**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: *Draft 21 – June 10, 2015***

**ISSUE TITLE:** *Interconnect Modeling Using IBIS-ISS*

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**DATE SUBMITTED:**

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**STATEMENT OF THE ISSUE:**

This BIRD enhances IBIS with interconnect modeling features to support broadband and coupled package and on-die interconnect using IBIS-ISS and Touchstone data.

The BIRD also adds a keyword for buffer rail mapping, to link to the new Terminal definitions defined for buffers.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

Definitions:

Enhanced interconnect descriptions in IBIS, called hereinafter “IBIS Interconnect Models”, rely on several assumptions:

1. IBIS Interconnect Models can be described either using IBIS-ISS subcircuit files or Touchstone files. Interconnect Model definitions may be included inside an IBIS file, but neither IBIS-ISS nor Touchstone data may be included inside an IBIS file.
2. If two points in an IBIS Interconnect Model are “Linked”, then there is either a low resistance DC electrical path between the two points, or a small insertion loss at the Nyquist frequency between the two points. For the purposes of IBIS Interconnect Models, “point” and “node” refer to identical locations.
3. IBIS Components, and therefore IBIS Interconnect Models, contain terminals consisting of Pins, Die Pads, Buffer I/O Terminals, and Buffer Supply Terminals. Pins are defined under the [Pin] keyword, and may be I/O, POWER, GND, or NC.
4. For each I/O Pin, there is a single, associated Die Pad and single, associated Buffer I/O Terminal. All of these shall be considered “Linked”.
5. Under [Pin], for each Signal\_name associated with Model\_name POWER or GND, all Pins, Die Pads and Buffer Supply Terminals that use that Signal\_name are “Linked”
6. IBIS assumes that each I/O [Pin] is connected to one Die Pad and one Buffer I/O Terminal. Two differential I/O pins shall be connected to two differential die pads and either two single-ended Buffer I/O Terminals or a single true differential Buffer I/O Terminal.
7. If multiple Buffer Terminals (Supply or I/O) are connected to a single pin, EMD shall be used for the interconnect description.
8. An Interconnect Model may describe the relationship between a single Pin and Buffer Terminal (Supply or I/O), a signle Pin and linked Die Pad, or between a single Die Pad and a Buffer Terminal (Supply or I/O). An Interconnect Model may also describe connections between multiple Pins and multiple Buffer Terminals (Supply and I/O), multiple Pins and multiple Die Pads, or multiple Die Pads and multiple Buffer Terminals (Supply and I/O).

**ANY OTHER BACKGROUND INFORMATION:**

Parameter is shorted to Param (.param is legal in IBIS-ISS) to differentiate it further from Parameters in the multi-lingual syntax (Parameter has several meanings in IBIS and the Algorithmic Modeling Interface.)

File\_names are not quoted to be consistent with Corner in the multi-lingual syntax.

For File\_TS, all columns typ, min, and max are entered (or NA for either or both min and max) to follow the corner syntax convention used for most IBIS keywords and subparameters. The typ entry is required, and the typ entry value is used by the EDA tool for any NA entry. The same typ, min, max convention is used for the subparameter Param.

Entries for strings in Param are surrounded by double quotes to be consistent with string\_literal Parameters in the multi-lingual syntax (or where the AMI string\_literal parameter surrounded by double quotes is passed into the multi-lingual Parameters reference). The EDA tool needs to convert string\_literals into the parameter string syntax in IBIS-ISS.

Interaction of Param entries was not discussed. For example, for a transmission line, TD and Z0 could each have max and min entries, but the EDA tool could make available combinations of min/min, min/max, max/min or max/max for any corner . Due to parameter interactions, some mixing of corner combinations might not be realistic. (E.g., Z0min or Z0max might not correlate with TDmin or TDmax values, where TDmin=sqrt(LminCmin), Z0min=sqrt(Lmin/Cmax), etc.).

How corners of File\_IBIS-ISS and Params are processed might be based on vendor supplied documentation. For example some, but not all, combinations are shown below:

1. One file\_name for all corners, one .subckt name, and all corner settings controlled by Param settings
2. One file\_name, three .subckts (with internal default .param settings), additional corner settings controlled by Param settings or Param is not used
3. Three file\_names with the same .subckt name, but with distinct default .param settings, additional settings controlled by Param settings or Param is not used
4. Three file\_names with three distinct .subckt name and with distinct default .param settings, additional corner settings controlled by Param settings or Param is not used

No interpretation is given for Param typ, min, and max values. It is possible to independently use typ, min, or max values for any of the Param names that have been defined (e.g., the max value of one parameter may be used with the min value of another parameter).

The following keywords should be added as their own Chapter. The current Chapter 7 should be modified with the existing text placed in a sub-section called “[PACKAGE MODEL]”.

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**7 PACKAGE MODELING**

Several types of package modeling formats are available in IBIS. These include:

1. Lumped [Component]-level models for the entire [Component], using the [Package] keyword
2. Lumped [Component]-level modeling per-pin, using the [Pin] keyword
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Selector] and the keywords associated with it

The lumped formats are described in the [Package] and [Pin] keyword defintions above. The [Package Model] format is described in this chapter, while Interconnect Model Selectors are described in Chapter 13.

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**13 INTERCONNECT MODEL SELECTORS**

This chapter defines an advanced format for interconnect descriptions that may be used for packages as well as other types of interconnect between buffer models and pins, for signal and power path modeling purposes.

*Keyword:* [Interconnect Model Selector]

*Required:* No

*Description:* Used to list available interconnect models for the component.

*Usage Rules:* Interconnect Models are described by IBIS-ISS or Touchstone files that are between the Pins, Die Pads and Buffer Terminals (Supply and I/O) of a Component.

A component may have none, one or more than one Interconnect Model associated with it. If any Interconnect Models exist for the Component, they shall be listed in this section. An Interconnect Model Selector is required even if only a single Interconnect Model is associated with the Component.

The section under the [Interconnect Model Selector] keyword shall have two fields per line, with each line defining the Interconnect Models associated with the Component. The fields shall be separated by at least one white space. The first field lists the Interconnect Model name (up to 40 characters long). The second field is the name of the file containing the Interconnect Model. If the Interconnect Model is in this IBIS file, then the second field shall be “\*”.

The file containing the Interconnect Model shall be located in the same directory as the .ibs file. The file name shall follow the rules for file names given in Section 3, "GENERAL SYNTAX RULES AND GUIDELINES".

The first entry under the [Interconnect Model Selector] keyword shall be considered the default by the EDA tool. Each Interconnect Model name may only appear once under the [Interconnect Model Selector] keyword for a given Component.

*Example:*

[Interconnect Model Selector]

 QS-SMT-cer-8-pin-pkgs\_iss \*

 QS-SMT-cer-8-pin-pkgs\_sNp QS-SMT-cer-8-pin-pkgs\_sNp.ipkg

[End Interconnect Model Selector]

*Keyword:* [Begin Interconnect Model]

*Required:* No

*Description:* Marks the beginning of an interconnect model description.

*Usage Rules:* [Begin Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed.

*Example:*

[Begin Interconnect Model] QS-SMT-cer-8-pin-pkgs\_iss

The following subparameters are defined:

Manufacturer

Description

Param

File\_TS

File\_IBIS-ISS

Unused\_Terminal\_Termination

Number\_of\_Terminals

Terminal

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Manufacturer rules:

This optional subparameter specifies the name of the interconnect’s manufacturer. The length of the manufacturer’s name shall not exceed 40 characters. Blank characters are permitted.

Description rules:

This optional subparameter provides a concise yet easily human-readable description of what the Interconnect Model represents. The description shall be fewer than 60 characters in length, shall fit on a single line, and may contain spaces.

Unused\_Terminal\_Termination rules:

This optional subparameter defines the termination that is to be applied by the EDA tool during simulation to the Terminals of any IBIS-ISS subcircuit or Touchstone networks that are not being used in the [Begin Interconnect Model]/[End Interconnect Model] group. The subparameter name is followed by a single integer argument greater than zero on the same line, separated from the subparameter name by the “=” character and optionally whitespace.

If this subparameter is present, the EDA should connect the unused Terminals to GND through a resistorwith the value of resistance in ohms provided in the argument.

If this parameter is not defined and if Language is IBIS-ISS, then the EDA tool should connect the unused Terminals to GND through a 1 megaohm resistor. If Language is Touchstone, then the EDA tool should connect the unused Terminals to GND through a resistor with the Touchstone File reference resistance of the Terminal.

Only one Unused\_Terminal\_Termination subparameter may appear for a given [Begin Interconnect Model] keyword.

Number\_of\_Terminals rules:

The Number\_of\_Terminals subparameter is required and defines the number of terminals associated with the Interconnect Model. The subparameter name is followed by a single integer argument greater than zero on the same line, separated from the subparameter name by the “=” character and optionally whitespace. Only one Number\_of\_Terminals subparameter may appear for a given [Begin Interconnect Model] keyword. The Number\_of\_Terminals subparameter shall appear before the Terminal subparameter for a given Interconnect Model.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS.

The numerical value rules follow the scaling conventions in Section 3, GENERAL SYNTAX RULES AND GUIDELINES. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to The Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ\_s2p" | file name string passed

 | into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_IBIS-TS (documented next) is required for a [Begin Interconnect Model]/[End Interconnect Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_name, and circuit\_name (.subckt name) for an IBIS-ISS file. . The referenced file under file\_name shall be located in the same directory as the .ibs file.

*Example:*

| file\_type file\_name circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [Begin Interconnect Model]/[End Interconnect Model] group.File\_TS is followed by one unquoted string argument, which is the file name for a Touchstone file. The Touchstone file under file\_name shall be located in the same directory as the .ibs file.

*Example:*

| file\_type file\_name

File\_TS typ.s8p

Terminal rules:

One or more Terminal subparameters may appear under a given [Begin Interconnect Model] keyword. At least one Terminal subparameter is required. Each Terminal line contains information on a terminal of an IBIS-ISS subckt (or Touchstone file).

The Terminal subparameter is followed by at least three arguments: Terminal\_number, Terminal\_ID and Terminal\_Location. An unlimited number of Qualifiers may optionally follow each of these three required arguments.

Terminal\_number

Terminal\_number is an identifier for a specific terminal. Terminal\_number shall be a positive non-zero integer less than or equal to the value of the Number\_of\_Terminals argument. The same Terminal\_number shall not appear more than once for a given Interconnect Model. If any Terminals are not present for a given Interconnect Model, then those terminals are unused, and shall be terminated according to the Unused\_Terminal\_Termination rules.

Terminal\_ID

Terminal\_ID is a string, which shall match one of the following:

a [Pin] name

a signal\_name

a model\_name

“Default”

Terminal\_ID entries shall conform to restrictions imposed by Terminal\_Location values (see below).

Terminal\_Location

Terminal\_Location is a string, and shall have one of the values:

Pin\_A\_signal

Pad\_A\_signal

A\_signal

Pin\_Signal\_name

Pad\_Signal\_name

A\_Signal\_name

A\_puref

A\_pdref

A\_pcref

A\_gcref

A\_extref

Terminal\_Location Rules

* Pin\_A\_signal indicates this terminal is the buffer’s A\_signal\_terminal and is connected to a specific pin. Terminal\_ID shall be a Pin\_name, Model\_name or Default.
* Pad\_A\_signal indicates this terminal is the buffer’s A\_signal\_terminal and is connected to a specific die pad. Terminal\_ID shall be a Pin\_name, Model\_name or Default.
* A\_signal indicates this terminal is the buffer’s A\_signal terminal. Terminal\_ID shall be a Pin\_name, Model\_name or Default.
* Pin\_Signal\_name indicates that this terminal is connected to all pins that have Signal\_name Terminal\_ID. Terminal\_ID shall be a Signal\_name on a Pin that has Model\_name Power or GND. All pins that have Signal\_name Terminal\_ID are considered shorted together at the pin side of the package model.
* Pad\_Signal\_name indicates that this terminal is connected to all die pads that have Signal\_name Terminal\_ID. Terminal\_ID shall be a Signal\_name on a Pin that has Model\_name Power or GND. All die pads that have Signal\_name Terminal\_IDs are considered shorted together at the die pad side of the package model.
* A\_Signal\_name indicates that this terminal is connected to all buffer model terminals Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference or External Reference (A\_puref, A\_pdref, A\_pcref, A\_gcref or A\_extref) that have an Terminal\_ID containing a Signal\_name Terminal\_ID shall be a Signal\_name on a Pin that has Model\_name Power or GND. All Buffer Terminals that have Signal\_name Terminal\_ID are considered shorted together at the buffer side of the package model.
* A\_puref indicates this terminal is connected to a specific buffer model pullup reference. Terminal\_ID shall be a Pin\_name, Model\_name or Default.
* A\_pdref indicates this terminal is connected to a specific buffer model pulldown reference. Terminal\_ID shall be a Pin\_name, Model\_name or Default.
* A\_pcref indicates this terminal is connected to a specific buffer model power clamp reference. Terminal\_ID shall be a Pin\_name, Model\_name or Default.
* A\_gcref indicates this terminal is connected to a specific buffer model ground clamp reference. Terminal\_ID shall be a Pin\_name, Model\_name or Default.
* A\_extref indicates this terminal connected to a specific buffer model external reference. Terminal\_ID shall be a Pin\_name, Model\_name or Default.

Qualifiers

Qualifiers are strings, which are limited to the specific values:

“Aggressor”

“Model\_name”

“Default”

“Inverting”

“Non-Inverting”

Connection(n), where the string “Connection” is followed by an integer value, n.

Qualifiers are optional. There may be zero, one, or several qualifiers for each Terminal line. Qualifiers may appear in any order.

Qualifier Rules

* Aggressor: A Terminal may be either a “Victim” or an “Aggressor”. An Aggressor terminal does not have coupling from other sources. Connections are Victims by default.
* Model\_name: using the Model\_name qualifier identifies the Terminal\_ID on this terminal as a Model\_name.
* Default: using the Default qualifier identifies the associated Terminal\_ID on this terminal as Default. A Terminal shall not use both Default and Model\_name qualifiers.
* All terminals that have the identical Connection(n) qualifiers are electrically connected. A single-ended connection will have two terminals with Connection(n). A differential connection will have four terminals with Connection(n). Connection(n) qualifiers are required if there are two or more Pre-Layout connections (see below) within a single Interconnect Model.
	+ There shall be only one terminal for each Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference and External Reference on a true differential [External Model]. These can be referenced by either the Non-Inverting or Inverting signal Pin\_name.
	+ There shall be only one terminal for each Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference and External Reference for each side of a legacy differential model that consists of two independent single-ended models. These can be referenced by either the Non-Inverting or Inverting signal Pin\_name.
	+ There may be two terminals for each Pullup Reference, Power Reference, Power Clamp Reference, Ground Clamp Reference and External Reference for each side of a legacy differential model that consists of two independent single-ended models.

Pre-layout Terminals

* If a terminal uses either Default or Model\_name qualifiers, then the terminal is considered a “Pre-Layout” terminal. If a “Pre-Layout” terminal is connected to a differential model, then the terminal shall use only the following Terminal Locations:
	+ - Pin\_A\_signal\_pos
		- Pad\_A\_signal\_pos
		- A\_signal\_pos
		- Pin\_A\_signal\_neg
		- Pad\_A\_signal\_neg
		- A\_ signal\_neg

*Other Notes:*

More than one Interconnect Model may be available for a specific simulation. The EDA tool may choose any of the available models but, in general, should prefer a model that matches by Pin\_name, then Model\_name and finally Default.

For an Interconnect Model using File\_TS with N ports, N is determined from the [Number of Ports] field in a Touchstone 2 file. The [Number of Terminals] in the Interconnect Model shall be N+1. Terminal rules are described below:

* The EDA tool shall use the Pin\_name or Signal\_name specified for the associated Terminal “N+1” entry as the reference node for each of the N ports.
* Terminal/Port Mapping
	+ Terminal              Port
	+ 1                              1
	+ 2                              2
	+ …
	+ N                             N
	+ N+1 reference
* If a Port is not connected, then it shall be terminated by the EDA tool with a resistor to the node on Terminal N+1. The resistance shall be the Port Reference Impedance.
* It shall be an error if Terminal N+1 is not specified to be connected to a Pin, a Pad, or a Buffer that is not part of a connection to a Signal\_name that is POWER or GND

*Examples:*

IBIS File

[Pin] signal\_name model\_name R\_pin L\_pin C\_pin

A1 DQ1 DQ

A2 DQ2 DQ

A3 DQ3 DQ

D1 DQS DQS

D2 DQS DQS

P1 VDD POWER

P2 VDD POWER

P3 VDD POWER

P4 VDD POWER

P5 VDD POWER

G1 VSS GND

G2 VSS GND

G3 VSS GND

G4 VSS GND

[Diff Pin] inv\_pin vdiff tdelay\_typ tdelay\_min tdelay\_max

D1 D2 NA NA NA NA

[Die Supply Pads]

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Buffer Rail Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1 VSS VDD NC NC NC

A2 VSS VDD NC NC NC

A3 VSS VDD NC NC NC

D1 VSS VDD NC NC NC

D2 VSS VDD NC NC NC

| Single DQ (A1)

Terminal 1 Pin\_A\_signal A1

Terminal 2 A\_signal A1

| Single DQS | There is a [Diff Pin] entry “D1 D2 …”

Terminal 1 Pin\_A\_signal D1

Terminal 2 Pin\_A\_signal D2

Terminal 3 A\_signal D1

Terminal 4 A\_signal D2

| One DQ (A2) victim, two DQ (A1 and A3) aggressors

Terminal 1 Pin\_A\_signal A1 Aggressor

Terminal 2 A\_signal A1 Aggressor

Terminal 3 Pin\_A\_signal A2

Terminal 4 A\_signal A2

Terminal 5 Pin\_A\_signal A3 Aggressor

Terminal 6 A\_signal A3 Aggressor

|Single DQ (A1) Pin to Die Pad

Terminal 1 Pin\_A\_signal A1

Terminal 2 Pad\_A\_signal A1

| Single-ended model that can be used for all I/O pins

Terminal 1 Pin\_A\_signal Default Default

Terminal 2 A\_signal Default Default

| Model that can connect all Pins with Signal\_name VDD to all Buffer supply terminals that are connected to

| Signal\_name VDD as described in Pin\_mapping. All Pins with Signal\_name VDD are shorted together.

| All Buffer supply terminals that are connected to Signal\_name VDD are shorted together

Terminal 1 Pin\_Signal\_name VDD

Terminal 2 A\_Signal\_name VDD

| VDD: Pins connected to board “bed spring” model, all buffer terminals connected to VDD shorted

Terminal 1 Pin\_A\_signal P1

Terminal 2 Pin\_A\_signal P2

Terminal 3 Pin\_A\_signal P3

Terminal 4 Pin\_A\_signal P4

Terminal 5 Pin\_A\_signal P5

Terminal 6 A\_Signal\_name VDD

| VDD: Interconnect between VDD Pins and individual buffer Pullup Reference.

Terminal 1 Pin\_A\_signal P1

Terminal 2 Pin\_A\_signal P2

Terminal 3 Pin\_A\_signal P3

Terminal 4 Pin\_A\_signal P4

Terminal 5 Pin\_A\_signal P5

Terminal 6 A\_puref A1

Terminal 7 A\_puref A2

Terminal 8 A\_puref A3

Terminal 9 A\_puref D1

| VDD: Interconnect between VDD Pins and die VDD pads.

Terminal 1 Pin\_A\_signal P1

Terminal 2 Pin\_A\_signal P2

Terminal 3 Pin\_A\_signal P3

Terminal 4 Pin\_A\_signal P4

Terminal 5 Pin\_A\_signal P5

Terminal 6 Pad\_Signal\_name VDD1

Terminal 7 Pad\_Signal\_name VDD2

Terminal 8 Pad\_Signal\_name VDD3

| VDD: Interconnect between die VDD pads and individual buffer Pullup Reference.

Terminal 1 Pad\_Signal\_name VDD1

Terminal 2 Pad\_Signal\_name VDD2

Terminal 3 Pad\_Signal\_name VDD3

Terminal 4 A\_puref A1

Terminal 5 A\_puref A2

Terminal 6 A\_puref A3

Terminal 7 A\_puref D1

| Single DQ

Terminal 1 Pin\_A\_signal DQ Model\_name

Terminal 2 A\_signal DQ Model\_name

| Single DQS

Terminal 1 Pin\_A\_signal\_pos DQS Model\_name

Terminal 2 Pin\_A\_signal\_neg DQS Model\_name

Terminal 3 A\_signal\_pos DQS Model\_name

Terminal 4 A\_signal\_neg DQS Model\_name

| Single DQ victim, two DQ aggressors

Terminal 1 Pin\_A\_signal DQ Model\_name Aggressor Connection(1)

Terminal 2 A\_signal DQ Model\_name Aggressor Connection(1)

Terminal 3 Pin\_A\_signal DQ Model\_name Connection(2)

Terminal 4 A\_signal DQ Model\_name Connection(2)

Terminal 5 Pin\_A\_signal DQ Model\_name Aggressor Connection(3)

Terminal 6 A\_signal DQ Model\_name Aggressor Connection(3)

| One DQ victim, two DQ aggressors, one DQS aggressor

Terminal 1 Pin\_A\_signal DQ Model\_name Aggressor Connection(1)

Terminal 2 A\_signal DQ Model\_name Aggressor Connection(1)

Terminal 3 Pin\_A\_signal A2

Terminal 4 A\_signal A2

Terminal 5 Pin\_A\_signal DQ Model\_name Aggressor Connection(2)

Terminal 6 A\_signal DQ Model\_name Aggressor Connection(2)

Terminal 7 Pin\_A\_signal\_pos DQS Model\_name Aggressor Connection(3)

Terminal 8 A\_signal\_pos DQS Model\_name Aggressor Connection(3)

Terminal 9 Pin\_A\_signal\_neg DQS Model\_name Aggressor Connection(3)

Terminal 10 A\_signal\_neg DQS Model\_name Aggressor Connection(3)

| One single-ended victim, two single-ended aggressors, one differential aggressor

Terminal 1 Pin\_A\_signal Default Default Aggressor Connection(1)

Terminal 2 A\_signal Default Default Aggressor Connection(1)

Terminal 3 Pin\_A\_signal Default Default

Terminal 4 A\_signal Default Default

Terminal 5 Pin\_A\_signal Default Default Aggressor Connection(2)

Terminal 6 A\_signal Default Default Aggressor Connection(2)

Terminal 7 Pin\_A\_signal\_pos Default Default Aggressor Connection(3)

Terminal 8 A\_signal\_pos Default Default Aggressor Connection(3)

Terminal 9 Pin\_A\_signal\_neg Default Default Aggressor Connection(3)

Terminal 10 A\_signal\_neg Default Model\_name Aggressor Connection(3)

| DQ: (A1) (Post-Layout)

Terminal 1 Pin\_A\_signal A1

Terminal 2 A\_signal A1

| DQS: (Post-Layout) There is a [Diff Pin] entry “D1 D2 …”

Terminal 1 Pin\_A\_signal D1

Terminal 2 Pin\_A\_signal D2

Terminal 3 A\_signal D1

Terminal 4 A\_signal D2

| DQS: (Pre-Layout)

Terminal 1 Pin\_A\_signal\_pos DQS Model\_name

Terminal 2 Pin\_A\_signal\_neg DQS Model\_name

Terminal 3 A\_signal\_pos DQS Model\_name

Terminal 4 A\_signal\_neg DQS Model\_name

| VDD: Pins connected to board “bed spring” model, all buffer terminals connected to VDD shorted

Terminal 1 Pin\_A\_signal P1

Terminal 2 Pin\_A\_signal P2

Terminal 3 Pin\_A\_signal P3

Terminal 4 Pin\_A\_signal P4

Terminal 5 Pin\_A\_signal P5

Terminal 6 A\_Signal\_name VDD

| VDD: Interconnect between VDD Pins and individual buffer Pullup Reference

Terminal 1 Pin\_A\_signal P1

Terminal 2 Pin\_A\_signal P2

Terminal 3 Pin\_A\_signal P3

Terminal 4 Pin\_A\_signal P4

Terminal 5 Pin\_A\_signal P5

Terminal 6 A\_puref A1

Terminal 7 A\_puref A2

Terminal 8 A\_puref A3

Terminal 9 A\_puref D1

*Keyword:* [**End Interconnect Model**]

*Required:* Yes, for each instance of the [Begin Interconnect Model] keyword

*Description:* Indicates the end of the Interconnect Model data.

*Other Notes:* Between the [Begin Interconnect Model] and [End Interconnect Model] keywords is the package model data itself. The data describes any number of interfaces to either IBIS-ISS models or Touchstone files.

*Example:*

[End Interconnect Model]

*Keyword:* **[Die Supply Pads]**

*Required:* No

*Description:* This begins a section in [Component] that contains one line of data assigning die pads as supply nodes. IBIS assumes that for I/O pins (pins that have a Model\_name that is not POWER, GND or NC), there is a one-to-one correspondence between a Pin, a Die Pad and the Buffer I/O connection point. There are no such assumptions for POWER and GND pins. A POWER or GND Signal\_name may have a different number of Pin nodes, die pad nodes and buffer nodes. If the model maker chooses to make separate package and on-die power distribution networks (PDN), then he shall supply a list of nodes (and their associated Signal\_name) that can be used to mate the package and on-die PDN models.

*Sub-Params:* None

*Usage Rules:*  Arguments under the [Die Supply Pads] keyword consist of two strings per line, where the strings define a die pad node name and a corresponding Signal\_name, in that order. Signal\_names may appear multiple times, but die pad node names may appear only once each under the [Die Supply Pads] keyword.

*Other Notes:* The data in this section consists of a list of die pad node names and their corresponding Signal\_names that can be used to mate package and on-die PDN networks.

*Example:*

[Die Supply Pads]

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

*Keyword:* **[End Die Supply Pads]**

*Required:* Yes

*Description:* Indicates the end of the [Die Supply Pads] data.

*Other Notes:*

*Example:*

[End Die Supply Pads]

*Examples*

[Define Package Model]

[Begin Interconnect Model] IOA3

| file\_name typ min max

File\_TS ioA3.s2p NA NA

Number\_of\_Terminals = 2

Terminal 1 Pin\_A\_signal Pin\_name A3

Terminal 2 A\_signal Pin\_name A3

Terminal 3 Pin\_Signal\_name VSS

[End Interconnect Model]

[Begin Interconnect Model] IOA7

| This model uses I/O pin A7

| file\_name typ min max

File\_TS ioA7.s2p NA NA

Number\_of\_Terminals = 2

Terminal 1 Pin\_A\_signal A7

Terminal 2 A\_signal A7

Terminal 3 Pin\_Signal\_name VSS

[End Interconnect Model]

[Begin Interconnect Model] IOB3C3

| file\_name typ min max

File\_TS ioB3C3.s4p NA NA

Number\_of\_Terminals = 4

Terminal 1 Pin\_A\_signal Pin\_name B3

Terminal 2 A\_Signal Pin\_name B3

Terminal 3 Pin\_A\_signal Pin\_name C3

Terminal 4 A\_Signal Pin\_name C3

Terminal 5 Pin\_Signal\_name VSS

[End Interconnect Model]

[Begin Interconnect Model] IOA3

| file\_type corner\_name file\_name circuit\_name (.subckt name)

File\_IBIS-ISS Typ io.iss io

Parameter Length Value 10. | 10mm

Number\_of\_Terminals = 2

Terminal 1 Pin\_A\_signal Pin\_name A3

Terminal 2 A\_signal Pin\_name A3

Terminal 3 Pin\_Signal\_name VSS

[End Interconnect Model]

[Begin Interconnect Model] DQS

| file\_name typ min max

File\_TS DQS.s4p NA NA

Number\_of\_Terminals = 4

Terminal 1 Pin\_A\_signal Model\_name DQS Diff\_pos

Terminal 2 A\_signal Model\_name DQS Diff\_pos

Terminal 3 Pin\_A\_signal Model\_name DQS Diff\_neg

Terminal 4 A\_signal Model\_name DQS Diff\_neg

Terminal 5 Pin\_Signal\_name VSS

[End Interconnect Model]

[Begin Interconnect Model] VDDQ

| file\_type corner\_name file\_name circuit\_name (.subckt name)

File\_IBIS-ISS Typ vddq.iss vddq

Number\_of\_Terminals = 2

Terminal 1 Pin\_A\_signal Signal\_name VDDQ

Terminal 2 A\_signal Signal\_name VDDQ

Terminal 3 Pin\_Signal\_name VSS

[End Interconnect Model]

[Begin Interconnect Model] VDDQ\_A3

| file\_type corner\_name file\_name circuit\_name (.subckt name)

File\_IBIS-ISS Typ vddq\_a3.iss vddq\_A3

Number\_of\_Terminals = 2

Terminal 1 Pin\_A\_signal Signal\_name VDDQ

Terminal 2 A\_signal Pin\_name A3 Pullup\_Reference

Terminal 3 Pin\_Signal\_name VSS

[End Interconnect Model]

[Begin Interconnect Model] IOA3

| file\_name typ min max

File\_TS ioA3.s10p NA NA

Number\_of\_Terminals = 10

Terminal 1 Pin\_A\_signal Pin\_name A3

Terminal 2 A\_signal Pin\_name A3

Terminal 3 Pin\_A\_signal Model\_name DQ NA 1 Aggressor

Terminal 4 A\_signal Model\_name DQ NA 1 Aggressor

Terminal 5 Pin\_A\_signal Model\_name DQ NA 2 Aggressor

Terminal 6 A\_signal Model\_name DQ NA 2 Aggressor

Terminal 7 Pin\_A\_signal Model\_name DQS Diff\_pos 3 Aggressor

Terminal 8 A\_signal Model\_name DQS Diff\_pos 3 Aggressor

Terminal 9 Pin\_A\_signal Model\_name DQS Diff\_neg 3 Aggressor

Terminal 10 A\_signal Model\_name DQS Diff\_neg 3 Aggressor

Terminal 11 Pin\_Signal\_name VSS

[End Interconnect Model]

[End Interconnect Model Data]

[End Package Model]

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

The following section should be included in Chapter 5, Component Modeling.

*Keyword:* [Buffer Rail Mapping]

*Required:* No

*Description:* Used to indicate the signal\_name to which a given driver, receiver or terminator is connected.

*Sub-Params:* pulldown\_ref, pullup\_ref, gnd\_clamp\_ref, power\_clamp\_ref, ext\_ref

*Usage Rules:* The [Buffer Rail Mapping] defines the connections between POWER and/or GND pins and buffer and/or terminator voltage supply references using signal\_name. When [Buffer Rail Mapping] is present, then the signal\_name field (second column of [Pin]) shall indicate that all POWER and GND pins with the same signal\_name are connected.

Each line shall contain either three, five or six entries. Use the reserved word NC for columns where a connection is not made.

The first column contains a pin name. Each pin name shall match one of the pin names declared in the [Pin] section of the [Component] as a buffer or terminator.

The remaining columns correspond to the voltage supply references for the named pin. Each [Model] supply reference is connected to a signal\_name in the corresponding column.

The second column, pulldown\_ref, designates the ground (GND) signal\_name for the buffer or termination associated with that pin. The signal\_name under pulldown\_ref is associated with the [Pulldown] I-V table for non-ECL [Model]s. This is also the signal\_name associated with the [GND Clamp] I-V table and the [Rgnd] model unless overridden by a label in the gnd\_clamp\_ref column.

The third column, pullup\_ref, designates the power (POWER) signal\_name for the buffer or termination. The signal\_name under pullup\_ref is associated with the [Pullup] table for non-ECL [Model]s (for ECL models, this bus is associated with the [Pulldown] table). This is also the signal\_name associated with the [POWER Clamp] I-V table and the [Rpower] model unless overridden by a label in the power\_clamp\_ref column.

The fourth and fifth columns, gnd\_clamp\_ref and power\_clamp\_ref, contain entries, if needed, to specify additional ground signal\_name and power signal\_name connections for clamps. Finally, the sixth column, ext\_ref, contains entries to specify external reference supply signal\_name connections.

There shall be no entries for pins listed under the [Pin] keyword with model\_name GND, POWER and NC.

If the [Buffer Rail Mapping] keyword is present, then the supply reference connections for every pin listed under the [Pin] keyword (except POWER, GND and NC pins) shall be given.

The column length limits are:

[Buffer Rail Mapping] 5 characters max

pulldown\_ref 40 characters max

pullup\_ref 40 characters max

gnd\_clamp\_ref 40 characters max

power\_clamp\_ref 40 characters max

ext\_ref 40 characters max

*Example:*

[Buffer Rail Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

|

1 VSS1 VCC1 | Signal pins and their associated

2 VSS2 VCC2 | ground, power and external

| | reference connections

3 VSS1 VCC1 VSSCLAMP VCCCLAMP

4 VSS2 VCC2 VSSCLAMP VCCCLAMP

5 VSS2 VCC2 NC VCCCLAMP V\_EXTREF1

6 VSS2 VCC2 NC VCCCLAMP

7 VSS2 VCC2 NC VCCCLAMP V\_EXTREF2

8 VSSCLAMP VCCCLAMP | Note that normal Input, Output and I/O

| buffers will need only three columns

| | Some possible clamping

| | connections are shown above

| | for illustration purposes

|

| The following [Pin] list corresponds to the [Buffer Rail Mapping] shown above.

|

[Pin] signal\_name model\_name R\_pin L\_pin C\_pin

|

1 OUT1 output\_buffer1 | Output buffers

2 OUT2 output\_buffer2 |

3 IO3 io\_buffer1 | Input/output buffers

4 IO4 io\_buffer2 |

5 SPECIAL1 ref\_buffer1 | Buffers with POWER CLAMP but no

6 SPECIAL2 io\_buffer\_term1 | GND CLAMP I-V tables; two use

7 SPECIAL3 ref\_buffer2 | external reference voltages

8 IN1 input\_buffer

11 VSS1 GND

12 VSS1 GND

13 VSS1 GND

21 VSS2 GND

22 VSS2 GND

23 VSS2 GND

31 VCC1 POWER

32 VCC1 POWER

33 VCC1 POWER

41 VCC2 POWER

42 VCC2 POWER

43 VCC2 POWER

51 VSSCLAMP GND | Power connections for clamps

52 VCCCLAMP POWER |

71 V\_EXTREF1 POWER | External reference voltage pins

72 V\_EXTREF2 POWER |

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The following section should be appended to the end of the IBIS document.

**12 RULES OF PRECEDENCE**

The sections below detail the rules of precedence to be assumed by EDA tools and model makers where multiple keywords may support similar functions.

**12.1 PACKAGES**

The order of precedence for package model data to be used by EDA tools in simulation is defined below, in ascending order. If a package data format at a numerically higher position on the list is available in an IBIS or related file, that data shall be used by the EDA tool for simulation; any data present in formats numerically lower on the list shall be ignored.

1. [Component]/[Package]
2. [Component]/[Pin]
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Selector]