**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER: *Draft 39 – August 24, 2016***

**ISSUE TITLE:** *Interconnect Modeling Using IBIS-ISS and Touchstone*

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**DATE ACCEPTED BY IBIS OPEN FORUM:**

**STATEMENT OF THE ISSUE:**

This BIRD enhances IBIS with interconnect modeling features to support broadband, coupled package, and on-die interconnect using IBIS-ISS and Touchstone data.

The BIRD also adds a keyword for buffer rail mapping, to link to new Terminal definitions defined for buffers.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

This BIRD has resulted from several years of discussion regarding the need for more flexible description of interconnects in IBIS. It was decided to avoid a keyword based approach, in favor of a circuit language approach. IBIS-ISS was developed for this purpose, and a means to instantiate IBIS-ISS models from IBIS became the logical next step.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. The model maker must be able to provide interconnect models representing die and package, using a combination of IBIS-ISS and Touchstone formats.
 | Might replace BIRD 125.1 |
| 1. Touchstone models without an IBIS-ISS wrapper circuit must be supported.
 | Might replace BIRD 158.1 |
| 1. An interconnect model may connect buffers to pins directly or separate models may be used for the buffer to pad and pad to pin connections (die and package portions).
 | Die is buffer to pad. Package is pad to pin. |
| 1. An interconnect model may connect one pin or any combination of pins on one [Component].
 | Coupled models are supported. |
| 1. The buffer I/O, pad, and pin terminals associated with I/O pins must be assignable to interconnect model terminals directly by pin name.
 |  |
| 1. The buffer supply, pad, and pin terminals associated with POWER and GND rail pins must be assignable to interconnect model terminals directly by pin name, or indirectly by [Pin] signal\_name or [Pin Mapping] bus\_label.
 |  |
| 1. The model maker must be able to provide alternative interconnect models for any given set of pins.
 | For example for a given pin pair it must be possible to provide both coupled and uncoupled models, high and low bandwidth models, or both IBIS-ISS and Touchstone models. |
| 1. The model maker may use new interconnect models for some pins and legacy package models for other pins.
 |  |
| 1. The model user must be able, given a pin or set of pins it must analyze, to locate all interconnect models that include the pin(s), if any.
 | Simulation netlisting begins with a list of pins that must be simulated. |
| 1. The model user must be able to determine all of the pins that a given interconnect model includes.
 | Once a model is chosen, it may add more pins to the simulation. |
| 1. The model user must be able to determine how to terminate any terminals of an interconnect model not necessary for a particular analysis.
 | May need to handle s-parameter and circuit models differently. |
| 1. For any pin having an interconnect model, models encompassing the full path from buffer to pin must be present and identifiable by the user.
 |  |
| 1. The model user must have useful information needed to make the choice between alternative interconnect models that differ only in characteristics other than the model format and the set of pins included.
 | For example: coupled/uncoupled, low/high bandwidth. This will be used to choose which alternative model set to use. |
| 1. The order of precedence for new interconnect models and legacy forms of package models must be specified.
 | Probably will take precedence over [Package Model], [Pin] RLC, and [Package]. |
| 1. The model user must not be required to use both new interconnect and legacy package models to model any single pin or coupled set of pins of a [Component].
 | For example can’t use [Pin] RLC for through path and IBIS-ISS for coupling. |
| 1. The model user must be informed which pins of an interconnect model have been modeled with coupling to other pins, sufficient for the former to represent the victim pins and the latter all of the aggressor pins in a crosstalk simulation.
 | Pins near one “end” of the model will be coupled to pins on one side but probably not enough pins on the other side. |

**BACKGROUND INFORMATION/HISTORY:**

Parameter is shortened to Param (.param is legal in IBIS-ISS) to differentiate it further from Parameters in the multi-lingual syntax (Parameter has several meanings in IBIS and the Algorithmic Modeling Interface.)

File\_names are not quoted, to be consistent with Corner in the multi-lingual syntax.

For File\_TS, all columns typ, min, and max are entered (or NA for either or both min and max) to follow the corner syntax convention used for most IBIS keywords and subparameters. The typ entry is required, and the typ entry value is used by the EDA tool for any NA entry. The same typ, min, max convention is used for the subparameter Param.

Entries for strings in Param are surrounded by double quotes to be consistent with string\_literal Parameters in the multi-lingual syntax (or where the AMI string\_literal parameter surrounded by double quotes is passed into the multi-lingual Parameters reference). The EDA tool needs to convert string\_literals into the parameter string syntax in IBIS-ISS.

Interaction of Param entries was not discussed. For example, for a transmission line, TD and Z0 could each have max and min entries, but the EDA tool could make available combinations of min/min, min/max, max/min or max/max for any corner. Due to parameter interactions, some mixing of corner combinations might not be realistic. (E.g., Z0min or Z0max might not correlate with TDmin or TDmax values, where TDmin=sqrt(LminCmin), Z0min=sqrt(Lmin/Cmax), etc.).

How corners of File\_IBIS-ISS and Params are processed might be based on vendor supplied documentation. For example some, but not all, combinations are shown below:

1. One file\_name for all corners, one .subckt name, and all corner settings controlled by Param settings
2. One file\_name, three .subckts (with internal default .param settings), additional corner settings controlled by Param settings or Param is not used
3. Three file\_names with the same .subckt name, but with distinct default .param settings, additional settings controlled by Param settings or Param is not used
4. Three file\_names with three distinct .subckt name and with distinct default .param settings, additional corner settings controlled by Param settings or Param is not used

No interpretation is given for Param typ, min, and max values. It is possible to independently use typ, min, or max values for any of the Param names that have been defined (e.g., the max value of one parameter may be used with the min value of another parameter).

**PROPOSED CHANGES:**

The following keyword should be added to Chapter 5, COMPONENT DESCRIPTION, after the [Alternate Package Models] keyword:

*Keyword:* [Interconnect Model Set Selector]

*Required:* No

*Description:* Used to list available Interconnect Models for the Component.

*Usage Rules:* Interconnect Models are described by IBIS-ISS subcircuits or Touchstone files that connect the Pins, Die Pads, and Buffer Terminals (Supply and I/O) of a Component.

A Component may have none, one, or more than one Interconnect Model Sets associated with it. If any Interconnect Models exist for the Component, they shall be listed in this section. An Interconnect Model Set Selector is required even if only a single Interconnect Model is associated with the Component. [Interconnect Model Set Selector] is hierarchically within the scope of the [Component] keyword.

The section under the [Interconnect Model Set Selector] keyword shall have two entries per line, with each line defining the list of Interconnect Model Sets associated with the Component. The entries shall be separated by at least one white space. The first entry lists the Interconnect Model Set name (up to 40 characters long). The second entry is the name of the file containing the Interconnect Model Set, with the extension “.ims”. If the Interconnect Model Set is in this IBIS file, then the second entry shall be “\*.ibs”.

The files containing the Interconnect Model Sets shall be located in the same directory as the .ibs file. The file names shall follow the rules for .ibs file names given in Section 3, ’GENERAL SYNTAX RULES AND GUIDELINES’. The file names and extensions shall be lower case. An [Interconnect Model Set] with matching name shall be found in the stated location for each Interconnect Model Set named in the [Interconnect Model Set Selector].

The first entry under the [Interconnect Model Set Selector] keyword shall be considered the default by the EDA tool. Each Interconnect Model Set name may only appear once under the [Interconnect Model Set Selector] keyword for a given Component.

*Example:*

[Interconnect Model Set Selector]

QS-SMT-cer-8-pin-pkgs\_iss \*.ibs | In this file, a full model is present

QS-SMT-cer-8-pin-pkgs\_sNp qs-smt-cer-8-pin-pkgs\_s16p.ict | A separate file

|
|
A1\_I/O\_and\_Rails           \*.ibs | I/O with PU, PD rails
A1\_I/O\_iss                 \*.ibs | I/Os without Rails
A2\_I/O\_iss                 \*.ibs
A3\_I/O\_iss                 \*.ibs
|
A1\_PU\_PD\_Rails\_iss         \*.ibs | PU, PD Rails separate from I/O path
I/O\_PU\_Rails\_iss           \*.ibs | One or many PU, PD buffer rails
I/O\_PD\_Rails\_iss           \*.ibs | (Assumes PC and GC rails
                                 |   are not needed)
|
A1\_A5\_I/Os\_and\_Rails\_iss   \*.ibs | Direct Buf\_Pin and Rails for A1-A5
|
A1\_A5\_I/Os\_Buf\_Pad\_iss     \*.ibs | Buf-Pad for A1-A5 I/Os
A1\_A5\_I/Os\_Pad\_Pin\_iss     \*.ibs | Pad-Pin for A1-A5 I/Os
20\_Rail\_Bed\_Spring\_iss     \*.ibs | Not all Power, Grounds Used
                                 |   or Connected for A1-A5 I/Os
                                 | Rails ca be Buf\_Pin while the I/Os
                                 |   are Buf\_Pad, Pad\_Pin; or visa-versa
|

[End Interconnect Model Set Selector]

*Keyword:* [**End Interconnect Model Set Selector**]

*Required:* Yes, for each instance of the [Interconnect Model Set Selector] keyword

*Description:* Indicates the end of the data for one [Interconnect Model Set Selector].

*Example:*

[End Interconnect Model Set Selector]

ssection 5, COMPONENT DESCRIPTION, after

*Keyword:* **[Die Supply Pads]**

*Required:* No

*Description:* Associates signal\_names and bus\_labels to die supply pads.

*Sub-Params:* signal name, bus\_label

*Usage Rules:*  Only die pads with signal\_names that occur on POWER or GND pins are allowed. Each line shall contain either two or three columns. The first column shall contain the die supply pad name. The second column, signal\_name, gives the data book name for the signal. The third column is optional. If it exists, it is a bus\_label. If the third column does not exist, then the bus\_label shall be the signal\_name.

*Other Notes:* The data in this section consists of a list of die pad node names and their corresponding signal\_names or bus\_labels that can be used to mate package and on-die power delivery networks.

*Example:*

[Die Supply Pads] signal\_name bus\_label

VDDQ VDDQ

VDD1 VDD VDDa

VDD2 VDD VDDa

VDD3 VDD VDDb

VSS1 VSS

VSS2 VSS

The following text should be added at the beginning of Chapter 7, PACKAGE MODELING, after the chapter head line.

Several types of package modeling formats are available in IBIS. These include:

1. Lumped [Component]-level models for the entire [Component], using the [Package] keyword.
2. Lumped [Component]-level modeling per-pin, using the [Pin] keyword.
3. [Package Model] (including [Alternate Package Models] and [Define Package Model]).
4. [Interconnect Model Set Selector] and the keywords associated with it.

The lumped formats are described in the [Package] and [Pin] keyword definitions above. Keywords for use with the [Package Model] format are described in this chapter, while keywords for use with [Interconnect Model Set Selector] are described in Chapter 12.

**KEYWORDS FOR USE WITH [Package Model]**

The following new Chapter 12 should be added after Chapter 11.

**12 INTERCONNECT MODELING**

, called “IBIS Interconnect Models” or simply “Interconnect Models”. Interconnect Models are gathered into Interconnect Model Sets that

Interconnect Models rely on several assumptions:

1. IBIS Interconnect Models may be described either using IBIS-ISS files or Touchstone files. Interconnect Model definitions may be included inside an IBIS file, but neither IBIS-ISS nor Touchstone data shall be included inside an IBIS file.
2. IBIS Components, and therefore IBIS Interconnect Models, contain terminals consisting of Pins, Die Pads, Buffer I/O Terminals, and Buffer Supply Terminals. Pins are defined under the [Pin] keyword, and may be I/O, POWER, GND, or NC.
3. Under [Pin], for each signal\_name associated with Model\_name POWER or GND, all Pins, Die Pads and Buffer Supply Terminals that use that signal\_name are “linked”
4. If two points in an Interconnect Model are “linked”, then there is either a low resistance DC electrical path between the two points, or a small impedance at the frequencies of interest between the two points. For the purposes of Interconnect Models, “point” and “node” refer to identical locations.
5. IBIS assumes that each I/O [Pin] is connected to one Die Pad and one Buffer I/O Terminal. Two differential I/O pins shall be connected to two differential die pads and either two single-ended Buffer I/O Terminals or a single true differential Buffer I/O Terminal.
6. An Interconnect Model may describe the relationship between a single Pin and Buffer Terminal (Supply or I/O), between a single Pin and Die Pad, or between a single Die Pad and a Buffer Terminal (Supply or I/O). An Interconnect Model may also describe connections between multiple Pins and multiple Buffer Terminals (Supply and I/O), between multiple Pins and multiple Die Pads, or between multiple Die Pads and multiple Buffer Terminals (Supply and I/O).

The specification permits .ibs files to contain the following additional list of Interconnect Model keywords and subparameters. Note that the actual Interconnect Models may be in a separate < filename>.ict file or may exist in a .ibs file between the [Interconnect Model] ... [End Interconnect Model] keywords for each Interconnect Model defined. For reference, these keywords and subparameters are listed in Table XX.

Table XX – Interconnect Modeling Keywords and Subparameters

| **Keyword or Subparameter** | **Notes** |
| --- | --- |
| [Interconnect Model Set] |  |
| [Interconnect Model] |  |
| Manufacturer |  |
| Description |  |
| Param |  |
| File\_TS | (note 1) |
| File\_IBIS-ISS | (note 1) |
| Unused\_terminal\_termination | (note 2) |
| Number\_of\_terminals | (note 3) |
| <terminal line> | (note 4) |
| [End Interconnect Model] | (note 5) |
| [End Interconnect Model Set] | (note 6) |
| Note 1 One of either the File\_TS or File\_IBIS-ISS subparameters is required.Note 2 The subparameter token shall be followed by the “=” character and a numeric value (integers and reals are acceptable), with both optionally surrounded by whitespace.Note 3 The subparameter token shall be followed by the “=” character and an integer value, with both optionally surrounded by whitespace.Note 4 No token or other reserved word is defined to identify terminal lines.Note 5 Required when the [Interconnect Model] keyword is usedNote 6 Required when the [Interconnect Model Set] keyword is used |

When Interconnect Model definitions occur within a .ibs file, their scope is “local”— they are known only within that .ibs file and no other. In addition, within that .ibs file, they override any interconnect package models defined using the [Package], [Pin], or [Define Package Model] keywords.

Usage Rules for the .ict File:

Package models are stored in a file whose name uses the format:

<filename>.ict.

The <filename> provided shall adhere to the rules given in Section 3, “GENERAL SYNTAX RULES AND GUIDELINES“. Use the “.ict” extension to identify files containing Interconnect Models. The .ict file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All of these keywords and associated subparameters follow the same rules as those for a normal .ibs file.

Note that the [Component] and [Model] keywords are not allowed in the .ict file. The .ict file is for Interconnect Models only.

*Keyword:* [Interconnect Model]

*Required:* No

*Description:* Marks the beginning of an Interconnect Model description.

*Sub-Params:* Manufacturer, Description, Unused\_terminal\_termination, Number\_of\_terminals, Param, File\_TS, File\_IBIS-ISS

*Usage Rules:* [Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model]/[End Interconnect Model] keyword pair is hierarchically equivalent in scope to [Component] and [Model].

The [Interconnect Model]/[End Interconnect Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an Interconnect Model, as well as defining the terminals and terminal usage for the Interconnect Model in the context of the given [Component].

An [Interconnect Model] shall contain for each signal, pin and buffer terminals (full package model), pin and die pad terminals (package only model) or die pad and buffer terminals (on-die package model). An [Interconnect Model] may not contain pin, buffer and die pad terminals for any signal.

*Other Notes:* If a full package model contains an I/O pin terminal for a pin\_name then it shall also contain an I/O buffer terminal for the same pin\_name. If a package only model contains an I/O pin terminal for a pin\_name then it shall also contain an I/O die pad terminal for the same pin\_name. If an on-die model contains an I/O buffer terminal for a pin\_name then it shall also contain an I/O die pad terminal for the same pin\_name.

A package model may just contain terminals to I/O buffer power rail buffer terminals.

A package model may contain terminals to one or more than one buffer I/O terminals.

A package model may contain terminals to both I/O buffer power rail buffer terminals and one or more than one buffer I/O terminals.

Each terminal of a package model passes current to the simulation node it is connected to and has a “voltage”. This, as stated, is imprecise. Voltage, by definition, is a potential difference between two points. It is common to probe and plot the potential difference between simulator nodes at a terminal and the simulator ideal Node 0. This is valid for non-power aware simulations when the local ground (or return path) node is forced to Node 0 by the simulator, or for “ground referenced” power aware simulations that lump the effect of the ground interconnect into the power rails. However, this is not valid when the voltages of the ground nodes are “floating”. In this case it is important that the actual rail node that is the reference node for measurements at the I/O buffer is included as a terminal in interconnect models. If this is not done, then the interconnect model will not correctly account for all return currents, particularly from capacitive elements. If an interconnect model does not contain a reference terminal, then the user of these models should be aware that using these models in non-ground referenced power aware simulations will introduce potential errors in simulations.

The following subparameters are defined:

Manufacturer

Description

Unused\_terminal\_termination = <value>

Param

File\_IBIS-ISS

File\_TS

Number\_of\_terminals = <value>

In addition to these subparameters, the [Interconnect Model]/[End Interconnect Model] section may contain lines describing terminals and their connections. No specific subparameter name, token, or other string is used to identify terminal lines.

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Manufacturer rules:

This optional subparameter specifies the name of the interconnect’s manufacturer. The length of the manufacturer’s name shall not exceed 40 characters. Blank characters are permitted.

Description rules:

This optional subparameter provides a concise yet easily human-readable description of what the Interconnect Model represents. The description shall be fewer than 60 characters in length, shall fit on a single line, and may contain spaces.

Unused\_terminal\_termination rules:

This optional subparameter defines the termination that is to be applied by the EDA tool during simulation to the Terminals of any IBIS-ISS subcircuit or Touchstone network that is not being used in the [Interconnect Model]/[End Interconnect Model] group. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace.

If this subparameter is present, the EDA tool should connect the unused Terminals to GND through a resistorwith the value of resistance in ohms provided in the argument.

If this parameter is not defined and File\_IBIS-ISS is present, the EDA tool may connect terminals to terminations as needed to prevent numerical instability in simulation (EDA tools are recommended to alert users when this occurs and document the termination value used). If File\_TS is present, then the EDA tool should connect the unused Terminals to GND through a resistor with the Touchstone file’s reference resistance for the corresponding Terminal.

Only one Unused\_terminal\_termination subparameter may appear for a given [Interconnect Model] keyword.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3, “GENERAL SYNTAX RULES AND GUIDELINES”. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to The Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ\_s2p" | file name string passed

 | into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_IBIS-TS is required for a [Interconnect Model]/[End Interconnect Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_name, and circuit\_name (.subckt name) for an IBIS-ISS file. The referenced file under file\_name shall be located in the same directory as the .ibs file.

*Example:*

| file\_type file\_name circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [Interconnect Model]/[End Interconnect Model] group.File\_TS is followed by one unquoted string argument, which is the file name for a Touchstone file. The Touchstone file under file\_name shall be located in the same directory as the referencing.ibs file or .ict file.

*Example:*

| file\_type file\_name

File\_TS typ.s8p

Number\_of\_terminals rules:

The Number\_of\_terminals subparameter is required and defines the number of Terminals associated with the Interconnect Model. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace. Only one Number\_of\_terminals subparameter may appear for a given [Interconnect Model] keyword. The Number\_of\_terminals subparameter shall appear before any Terminal lines and after all other subparameters for a given Interconnect Model.

Terminal line rules:

Terminal lines shall appear after the Number\_of\_terminals subparameter and before the [End Interconnect Model] keyword. No token or reserved word identifies terminal lines.

Each Terminal line contains information on a terminal of an IBIS-ISS subcircuit (or Touchstone file).

Terminal lines are of the form

<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier><Qualifier\_entry>[Aggressor]

Terminal\_number

Terminal\_number is an identifier for a specific terminal. Terminal\_number shall be a positive non-zero integer less than or equal to the value of the Number\_of\_terminals argument, and which also matches the number of terminals used in a corresponding IBIS-ISS subcircuit, or the number of ports plus 1 used in a corresponding Touchstone file. The same Terminal\_number shall not appear more than once for a given Interconnect Model. If any Terminals are not present for a given Interconnect Model, then those terminals are unused, and shall be terminated according to the Unused\_terminal\_termination rules.

The Terminal\_number entry shall match the IBIS\_ISS terminal (node) position or the Touchstone file terminal (line) position, plus an undeclared reference line. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries.

Terminal\_type
Terminal\_type shall be one of the following: Buf\_I/O, Buf\_PU\_Ref, Buf\_PD\_Ref, Buf\_PC\_Ref, Buf\_GC\_Ref, Buf\_Ext\_Ref, Buf\_Rail, Pad\_I/O, Pad\_Rail, Pin\_I/O, or Pin\_Rail. Buf\_I/O, Buf\_PU\_Ref, Buf\_PD\_Ref, Buf\_PC\_Ref, Buf\_GC\_Ref, Buf\_Ext\_Ref and Buf\_Rail are terminals of an Interconnect Model that connect directly to I/O buffers. Pad\_I/O and Pad\_Rail are terminals that are at the Die/Package interface. Pin\_I/O and Pin\_Rail are terminals that are at the Component PCB interface.

Terminal\_type\_qualifier
The Terminal\_type\_qualifier for Terminal\_types Buf\_I/O, Buf\_PU\_Ref, Buf\_PD\_Ref, Buf\_PC\_Ref, Buf\_GC\_Ref and Buf\_Ext\_Ref shall be pin\_name. The Terminal\_type\_qualifier for Terminal\_type Buf\_Rail may be signal\_name or bus\_label.

The Terminal\_type\_qualifier for Terminal\_type Pad\_I/O shall be pin\_name.

The Terminal\_type\_qualifier for Terminal\_type Pad\_Rail shall be one of pad\_name, signal\_name, or bus\_label.

The Terminal\_type\_qualifier for Terminal\_type Pin\_I/O shall be pin\_name.

The Terminal\_type\_qualifier for Terminal\_type Pin\_Rail shall be one of pin\_name, signal\_name, or bus\_label.

Qualifier\_entry
The <Qualifier\_entry> is the name permitted and to be used for the following Terminal\_type\_qualifiers:

pin\_name <pin\_name\_entry>

pad\_name <pad\_name\_entry>

signal\_name <signal\_name\_entry>

bus\_label <bus\_label\_entry>

Aggressor
The optional Aggressor field is allowed on all terminals. If the terminal is an I/O terminal, then the interconnect to that I/O terminal may be missing coupling to interconnections that are not included in this interconnect model. If a terminal is an I/O terminal and is not an Aggressor, then the interconnect to that I/O terminal will include coupling to all aggressor interconnections deemed necessary for coupled signal analysis.

Touchstone Files

For an Interconnect Model using File\_TS with N ports, N shall match the number of ports present in the data of the associated Touchstone 1.x file, or the value associated with the [Number of Ports] keyword in the associated Touchstone 2 file. The Number\_of\_terminals entry in the Interconnect Model shall be an integer equal to N+1. Terminal rules are described below:

* The EDA tool shall use the pin\_name or signal\_name specified for the associated Terminal “N+1” entry as the reference node for each of the N ports. For an Interconnect Model with N ports, the Terminals and Ports are associated as follows:
	+ Terminal              Port
	+ 1                              1
	+ 2                              2
	+ …
	+ N                             N
	+ N+1 reference
* If a Terminal with number less than or equal to N is not connected, then it shall be terminated by the EDA tool with a resistor to the node on Terminal N+1. The value of this resistance shall be the value associated with the Port Reference Impedance subparameter.
* Terminal N+1 shall be connected to a Pin, Pad, or Buffer Terminal which is in turn connected to a Pin with a signal\_name of POWER or GND.

The Terminal\_types Buf\_I/O, Pad\_I/O and Pin\_I/O are used only for any single terminal of a buffer described by the [Model] keyword and for any Model\_type subparameter listed in Table XX.  The Model\_types Series and \*\_diff are used for two-terminal configurations, and their terminals are described by two separate Buf\_I/O, Pad\_I/O and Pin\_I/O Terminal\_type lines.

Table XX summarizes the rules described above.

Table XX – Allowed Terminal\_type Associations1

| **Terminal\_type** | **Terminal\_type\_qualifier** | **aggressor** |
| --- | --- | --- |
| **pin\_name** | **signal\_name** | **bus\_label** | **pad\_name** |
| Buf\_I/O | X |  |  |  | A |
| Buf\_PU\_Ref | X |  |  |  |  |
| Buf\_PD\_Ref | X |  |  |  |  |
| Buf\_PC\_Ref | X |  |  |  |  |
| Buf\_GC\_Ref | X |  |  |  |  |
| Buf\_Ext\_Ref | X |  |  |  |  |
| Buf\_Rail |  | Y | Y |  |  |
| Pad\_I/O | X |  |  |  | A |
| Pad\_Rail |  | Y | Y | Z |  |
| Pin\_I/O | X |  |  |  | A |
| Pin\_Rail | Y | Y | Y |  |  |

Notes

1. In the table, “X” refers to I/O pin names. “Y” and “Z” are POWER and GND names. The letter “A” designates the word "Aggressor"

Connecting Pins, Pads and Terminals

Three classes of pins are defined for a Component: Signal Pins, Supply Pins and No Connect Pins. Supply Pins have a model\_name of either POWER or GND. No Connect Pins have model\_name NC. All other pins are classified as Signal Pins. Package models defined in this section assume that there is one Buf\_I/O Terminal and one Die Pad for each Signal Pin. Pins are assumed to use the names listed under the first column of the [Pin] keyword (the pin\_name column).

The model of an I/O buffer has supply terminals in addition to the Buf\_I/O. These supply (or rail) terminals can be Buf\_PU\_Ref, Buf\_PD\_Ref, Buf\_PC\_Ref, Buf\_GC\_Ref and/or Buf\_Ext\_Ref. The Buf\_PU\_Ref, Buf\_PD\_Ref, Buf\_PC\_Ref, Buf\_GC\_Ref and/or Buf\_Ext\_Ref terminals of a buffer are associated either with a bus\_label under the [Pin Mapping] keyword or a signal\_name under the [Pin] keyword. These terminals can be connected to Interconnect Models one of two ways:

1. By specifying a unique interconnect terminal for each I/O buffer Buf\_PU\_Ref, Buf\_PD\_Ref, Buf\_PC\_Ref, Buf\_GC\_Ref and/or Buf\_Ext\_Ref terminal
2. By assuming that all I/O buffer supply terminals connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal (of Terminal\_type Buf\_Rail) for all I/O buffer terminals that are connected to a specific signal\_name or bus\_label on at least one Supply Pin.

Pads are the location of the interface between the die and the package. Interconnect Models can either be between the Pins of a component and the I/O buffers, or they can be split into models between the Pins of a component and the Pads of the die and models between the Pads of the die and the I/O buffers. There is exactly one Pad (of Terminal\_type Pad\_I/O) for each Signal Pin. There can be any number of Pads (of Terminal\_type Pad\_Rail) for each signal\_name or bus\_label on Supply Pins. If Interconnect Models of supply (rail) networks are split between Pin/Pad and Pad/Buffer models, then the interface of supply connections at the die package interface can be handled in one of two ways:

1. By defining a list of Die Supply Pads, and specifying terminals for some or all of the Die Supply Pads that are connected to a bus\_label or signal\_name on at least one Supply Pin.
2. By assuming that all supply Pads connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pad\_Rail) for all Pads that are connected to a specific signal\_name on at least one Supply Pin.

Pins may be terminals of the Interconnect Model that connect directly to a PCB board or other type of system connection to an IBIS component. Pins can be Signal Pins (Pin\_I/O), or Supply Pins (Pin\_Rail). An Interconnect Model can connect supply pins in one of two ways:

1. By specifying terminals for some or all of the Supply Pins.
2. By assuming that all supply Pins connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all Pins that are connected to a specific signal\_name on at least one Supply Pin.

The Terminals of an Interconnect Model may be located at Pins and Pads, Pins and Buffers, or Pads and Buffers. A single Interconnect Model shall not have Terminals at Pins, Pads and Buffers simultaneously.

Any one pin shall not be included in more than one Terminal of an Interconnect Model.

Any one die pad shall not be included in more than one Terminal of an Interconnect Model.

Any one buffer terminal shall not be included in more than one Terminal of an Interconnect Model.

*Examples:*

| All examples show a [Interconnect Model Set] under [Component] for

| complete grouping of the [Interconnect Model] descriptions

|

| Naming convention for [Interconnect Model Set] is below

| ([Interconnect Model] may show additional details)

|

| Full – Includes all IO pins

| A1 or A1\_A3 – Designated pin or pins

| TS - Touchstone representation

| ISS - IBIS-ISS representation

| PDN - Includes power delivery network, can also be PU and PD

| IO - Only if modified differently than PDN below for buf\_pad\_pin

| buf\_pad\_pin – Includes models for buf\_pad, pad\_pin; if missing, buf\_pad

| sn - Uses signal\_name; if missing assumes pin\_name

| bl - Uses bus\_label; if missing assumes pin\_name

| pn - Uses pad\_name; if missing assumes pin\_name

| XTALK - Cross talk analysis (coupled nets may include Aggressor)

| Examples 1 – 11 apply to the configuration below:

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

D1    DQS+        DQS

D2    DQS-        DQS

P1    VDD         POWER

P2    VDD         POWER

P3    VDD         POWER

P4    VDD         POWER

P5    VDD         POWER

G1    VSS         GND

G2    VSS         GND

G3    VSS         GND

G4    VSS         GND

[Diff Pin] inv\_pin  vdiff  tdelay\_typ tdelay\_min tdelay\_max

D1         D2       NA     NA         NA         NA

[Die Supply Pads]  signal\_name bus\_label

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1            VSS          VDD        NC            NC              NC

A2            VSS          VDD        NC            NC              NC

A3            VSS          VDD        NC            NC              NC

D1            VSS          VDD        NC            NC              NC

D2            VSS          VDD        NC            NC              NC

| ... Pins below can be deleted with [Pin Mapping] BIRD

P1 NC VDD

P2 NC VDD

P3 NC VDD

P4 NC VDD

P5 NC VDD

G1 VSS NC

G2 VSS NC

G3 VSS NC

G4 VSS NC

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 1: Terminals for full IBIS-ISS component with PDN, as depicted below.

[Interconnect Model Set] Ful1\_ISS\_PDN\_1

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_1

File\_IBIS-ISS full\_buf\_pin\_1.iss full\_buf\_pin\_typ

Number\_of\_terminals = 29

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O      pin\_name A3  |  DQ3         DQ

4  Pin\_I/O      pin\_name D1  |  DQS+        DQS

5  Pin\_I/O      pin\_name D2  |  DQS-        DQS

6  Pin\_Rail     pin\_name P1  |  VDD         POWER

7  Pin\_Rail     pin\_name P2  |  VDD         POWER

8  Pin\_Rail     pin\_name P3  |  VDD         POWER

9  Pin\_Rail     pin\_name P4  |  VDD         POWER

10 Pin\_Rail     pin\_name P5  |  VDD         POWER

11 Pin\_Rail    pin\_name G1  |  VSS         GND

12 Pin\_Rail     pin\_name G2  |  VSS         GND

13 Pin\_Rail     pin\_name G3  |  VSS         GND

14 Pin\_Rail     pin\_name G4  |  VSS         GND

15 Buf\_I/O  pin\_name A1  |  DQ1         DQ

16 Buf\_I/O  pin\_name A2  |  DQ2         DQ

17 Buf\_I/O  pin\_name A3  |  DQ3         DQ

18 Buf\_I/O  pin\_name D1  |  DQS+        DQS

19 Buf\_I/O  pin\_name D2  |  DQS-        DQS

20 Buf\_PU\_Ref pin\_name A1  |  DQ1         DQ

21 Buf\_PU\_Ref pin\_name A2  |  DQ2         DQ

22 Buf\_PU\_Ref pin\_name A3  |  DQ3         DQ

23 Buf\_PU\_Ref pin\_name D1  |  DQS+        DQS

24 Buf\_PU\_Ref pin\_name D2  |  DQS-        DQS

25 Buf\_PD\_Ref pin\_name A1  |  DQ1         DQ

26 Buf\_PD\_Ref pin\_name A2  |  DQ2         DQ

27 Buf\_PD\_Ref pin\_name A3  |  DQ3         DQ

28 Buf\_PD\_Ref pin\_name D1  |  DQS+        DQS

29 Buf\_PD\_Ref pin\_name D2 |  DQS+        DQS

[End Interconnect Model]

[End Interconnect Model Set]



Figure 1 – Electrical Connections for Full Buffer\_Pin Model with Power Routing



Figure 2 – Electrical Terminals for Full Buffer\_Pin Model with Power Routing

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 2: Same as Example 1 except the PDN networks are simplified with

| signal\_name qualifiers to create a pair of POWER terminals and a pair

| of GND terminals

[Interconnect Model Set] Full\_ISS\_PDN\_sn\_2

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_2

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_2\_typ

Number\_of\_terminals = 14

1  Pin\_I/O      pin\_name A1    |  DQ1         DQ

2  Pin\_I/O      pin\_name A2    |  DQ2         DQ

3  Pin\_I/O      pin\_name A3    |  DQ3         DQ

4  Pin\_I/O     pin\_name D1    |  DQS+        DQS

5  Pin\_I/O     pin\_name D2    |  DQS-        DQS

|

| POWER and GND terminals with signal\_names

|

6  Pin\_Rail    signal\_name  VDD   |  VDD         POWER

7  Pin\_Rail     signal\_name   VSS   |  VSS         GND

|

8  Buf\_I/O   pin\_name A1    |  DQ1         DQ

9  Buf\_I/O    pin\_name A2    |  DQ2         DQ

10 Buf\_I/O   pin\_name A3    |  DQ3         DQ

11 Buf\_I/O   pin\_name D1    |  DQS+        DQS

12 Buf\_I/O   pin\_name D2    |  DQS-        DQS

|

| POWER and GND terminals with by signal\_names

|

13 Buf\_Rail  signal\_name   VDD   |  VDD         POWER

14 Buf\_Rail  signal\_name   VSS   |  VSS         GND

|

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 3: Single IO Touchstone connection with one extra terminal for the

| N+1 .s2p reference connection terminal

[Interconnect Model Set] A1\_TS

|-----

[Interconnect Model] A1\_TS\_buf\_pin

File\_TS dq\_ts\_buf\_pin.s2p

Number\_of\_terminals = 3

1 Pin\_I/O      pin\_name A1

2 Buf\_I/O    pin\_name A1

3 Buf\_PD\_Ref pin\_name A1 | VSS reference for .s2p file

 | Rail connections to Buf\_I/O through

 | [Pin Mapping] or a [Model] reference

 | voltages used if no external rails

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 4: Single IO pin documenting both IBIS-ISS and Touchstone files and

| showing that the Touchstone N+1 reference connection is to the VSS rail

[Interconnect Model Set] A1\_IBIS\_ISS\_buf\_pad\_pin

|-----

[Interconnect Model] A1\_TS\_pad\_pin

File\_TS dq\_ts\_buf\_pad.s2p

Number\_of\_terminals = 3

1 Pin\_I/O     pin\_name A1

2 Pad\_I/O     pad\_name A1

3 Pin\_Rail signal\_name VSS | VSS reference for .s2p file

| | Requires Pin\_Rail VSS connection

[End Interconnect Model]

[Interconnect Model] A1\_ISS\_buf\_pad

File\_IBIS-ISS dq\_iss\_pad\_pin.iss DQ\_pad\_pin\_typ

Number\_of\_terminals = 3

1 Pad\_I/O      pin\_name A1

2 Buf\_I/O    pin\_name A1

3 Buf\_PD\_Ref pin\_name A1 | A reference terminal for capacitor

 | connection

 | If missing a node 0 might be used with

 | reduced accuracy

|

| [Pin Mapping] connections used to connect external rails, or default

| internal [Model] rails used if no external rails

|

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 5: Full IO IBIS-ISS configuration with PDN terminals

} under separate [Interconnect Model]s

[Interconnect Model Set] Full\_ISS\_PDN\_3

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number\_of\_terminals = 11

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O      pin\_name A3  |  DQ3         DQ

4  Pin\_I/O      pin\_name D1  |  DQS+        DQS

5  Pin\_I/O      pin\_name D2  |  DQS-        DQS

6 Buf\_I/O  pin\_name A1  |  DQ1         DQ

7 Buf\_I/O  pin\_name A2  |  DQ2         DQ

8 Buf\_I/O  pin\_name A3  |  DQ3         DQ

9 Buf\_I/O  pin\_name D1  |  DQS+        DQS

10 Buf\_I/O  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail signal\_name VSS | Reference at the Pin\_Rail

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_1

File\_IBIS-ISS full\_ISS\_buf\_pin\_pdn.iss full\_buf\_pin\_PDN\_typ

Number\_of\_terminals = 19

1  Pin\_Rail    pin\_name P1  |  VDD         POWER

2 Pin\_Rail    pin\_name P2  |  VDD         POWER

3  Pin\_Rail    pin\_name P3  |  VDD         POWER

4  Pin\_Rail    pin\_name P4  |  VDD         POWER

5 Pin\_Rail    pin\_name P5  |  VDD         POWER

6 Buf\_PU\_Ref  pin\_name A1  |  DQ1         DQ

7 Buf\_PU\_Ref  pin\_name A2  |  DQ2         DQ

8 Buf\_PU\_Ref  pin\_name A3  |  DQ3         DQ

9 Buf\_PU\_Ref  pin\_name D1  |  DQS+        DQS

10 Buf\_PU\_Ref  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail    pin\_name G1  |  VSS         GND

12 Pin\_Rail   pin\_name G2  |  VSS         GND

13 Pin\_Rail   pin\_name G3  |  VSS         GND

14 Pin\_Rail   pin\_name G4  |  VSS         GND

15 Buf\_PD\_Ref  pin\_name A1  |  DQ1         DQ

16 Buf\_PD\_Ref  pin\_name A2  |  DQ2         DQ

17 Buf\_PD\_Ref  pin\_name A3  |  DQ3         DQ

18 Buf\_PD\_Ref  pin\_name D1  |  DQS+        DQS

19 Buf\_PD\_Ref  pin\_name D2  |  DQS-        DQS

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 6: Full IBIS-ISS IOs and separate PDNs, all with buf\_pad and

| pad\_pin [Interconnect Model]s

[Interconnect Model Set] Full\_ISS\_buf\_pad\_pin\_PDN\_4

|-----

[Interconnect Model] Full\_ISS\_pad\_pin\_IO

File\_IBIS-ISS full\_pad\_pin\_io.iss full\_pad\_pin\_IO\_typ

Number\_of\_terminals = 11

1  Pin\_I/O      pin\_name A1  |  DQ1         DQ

2  Pin\_I/O     pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     pin\_name D1  |  DQS+        DQS

5  Pin\_I/O     pin\_name D2  |  DQS-        DQS

|

6 Pad\_I/O  pin\_name A1  |  DQ1         DQ

7 Pad\_I/O  pin\_name A2  |  DQ2         DQ

8 Pad\_I/O  pin\_name A3  |  DQ3         DQ

9 Pad\_I/O  pin\_name D1  |  DQS+        DQS

10 Pad\_I/O  pin\_name D2  |  DQS-        DQS

11 Buf\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_IO

File\_IBIS-ISS full\_buf\_pad\_io.iss full\_buf\_pad\_IO\_typ

Number\_of\_terminals = 11

1  Pad\_I/O      pin\_name A1  |  DQ1         DQ

2  Pad\_I/O      pin\_name A2  |  DQ2         DQ

3  Pad\_I/O      pin\_name A3  |  DQ3         DQ

4  Pad\_I/O     pin\_name D1  |  DQS+        DQS

5  Pad\_I/O      pin\_name D2  |  DQS-        DQS

|

6 Buf\_I/O  pin\_name A1  |  DQ1         DQ

7 Buf\_I/O  pin\_name A2  |  DQ2         DQ

8 Buf\_I/O  pin\_name A3  |  DQ3         DQ

9 Buf\_I/O  pin\_name D1  |  DQS+        DQS

10 Buf\_I/O  pin\_name D2  |  DQS-        DQS

11 Pin\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn.iss full\_iss\_pad\_pin\_PDN\_typ

Number\_of\_terminals = 14

1  Pin\_Rail pin\_name P1    |  VDD         POWER

2 Pin\_Rail pin\_name P2    |  VDD         POWER

3  Pin\_Rail pin\_name P3    |  VDD         POWER

4  Pin\_Rail pin\_name P4    |  VDD         POWER

5 Pin\_Rail pin\_name P5    |  VDD         POWER

|

6 Pad\_Rail pad\_name VDD1 |  VDD         POWER

7 Pad\_Rail pad\_name VDD2 |  VDD         POWER

8 Pad\_Rail pad\_name VDD3 |  VDD         POWER

|

9  Pin\_Rail pin\_name G1   |  VSS         GND

10 Pin\_Rail pin\_name G2   |  VSS         GND

11 Pin\_Rail pin\_name G3   |  VSS         GND

12 Pin\_Rail pin\_name G4   |  VSS         GND

|

13 Pad\_Rail pad\_name VSS1 |  VSS         GND

14 Pad\_Rail pad\_name VSS2 |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn.iss full\_iss\_buf\_pad\_PDN\_typ

Number\_of\_terminals = 15

1 Pad\_Rail pad\_name VDD1 |  VDD         POWER

2 Pad\_Rail pad\_name VDD2 |  VDD         POWER

3 Pad\_Rail pad\_name VDD3 |  VDD         POWER

|

4 Buf\_PU\_Ref  pin\_name A1   |  DQ1         DQ

5 Buf\_PU\_Ref  pin\_name A2   |  DQ2         DQ

6 Buf\_PU\_Ref  pin\_name A3   |  DQ3         DQ

7 Buf\_PU\_Ref  pin\_name D1   |  DQS+        DQS

8 Buf\_PU\_Ref  pin\_name D2   |  DQS-        DQS

|

9 Pad\_Rail pad\_name VSS1 |  VSS         GND

10 Pad\_Rail pad\_name VSS2 |  VSS         GND

|

11 Buf\_PD\_Ref  pin\_name A1   |  DQ1         DQ

12 Buf\_PD\_Ref  pin\_name A2   |  DQ2         DQ

13 Buf\_PD\_Ref  pin\_name A3   |  DQ3         DQ

14 Buf\_PD\_Ref  pin\_name D1    |  DQS+        DQS

15 Buf\_PD\_Ref  pin\_name D2    |  DQS-        DQS

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 7: Full IBIS-ISS model with IO only [Interconnect Model] and a | separate PDN [Interconnect Model] with signal\_name qualifiers

[Interconnect Model Set] Full\_ISS\_PDN\_sn\_5

|-----

[Begin Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number \_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

6 Buf\_I/O pin\_name A1 | DQ1 DQ

7 Buf\_I/O pin\_name A2 | DQ2 DQ

8 Buf\_I/O pin\_name A3 | DQ3 DQ

9 Buf\_I/O pin\_name D1 | DQS+ DQS

10 Buf\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS | Reference at the Pin\_Rail

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_2

File\_IBIS-ISS full\_iss\_buf\_pin\_pdn\_2.iss full\_iss\_buf\_pad\_PDN\_2

Number\_of\_terminals = 4

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Buf\_Rail  signal\_name VDD  | VDD         POWER

3  Pin\_Rail     signal\_name VSS  |  VSS         GND

4 Buf\_Rail  signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 8: Same full IBIS-ISS model with PDN as in Example 7, but with the

| [Interconnect Model]s describing buf\_pad and pad\_pin connections

| separately

[Interconnect Model Set] Full\_ISS\_buf\_pad\_pin\_PDN\_sn\_6

|-----

[Interconnect Model] Full\_ISS\_pad\_pin\_IO

File\_IBIS-ISS full\_pad\_pin\_io.iss full\_pad\_pin\_IO\_typ

Number \_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

|

6 Pad\_I/O pin\_name A1 | DQ1 DQ

7 Pad\_I/O pin\_name A2 | DQ2 DQ

8 Pad\_I/O pin\_name A3 | DQ3 DQ

9 Pad\_I/O pin\_name D1 | DQS+ DQS

10 Pad\_I/O pin\_name D2 | DQS- DQS

11 Buf\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Begin Interconnect Model] Full\_ISS\_buf\_pad\_IO

File\_IBIS-ISS full\_buf\_pad\_io.iss full\_buf\_pad\_IO\_typ

Number\_of\_terminals = 11

1 Pad\_I/O pin\_name A1 | DQ1 DQ

2 Pad\_I/O pin\_name A2 | DQ2 DQ

3 Pad\_I/O pin\_name A3 | DQ3 DQ

4 Pad\_I/O pin\_name D1 | DQS+ DQS

5 Pad\_I/O pin\_name D2 | DQS- DQS

|

6 Buf\_I/O pin\_name A1 | DQ1 DQ

7 Buf\_I/O pin\_name A2 | DQ2 DQ

8 Buf\_I/O pin\_name A3 | DQ3 DQ

9 Buf\_I/O pin\_name D1 | DQS+ DQS

10 Buf\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN\_3

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn\_3.iss full\_iss\_pad\_pin\_pdn\_3

Number\_of\_terminals = 4

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Pad\_Rail     signal\_name VDD  |  VDD         POWER

3  Pin\_Rail     signal\_name VSS  |  VSS         GND

4 Pad\_Rail     signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN\_3

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn\_3 full\_iss\_buf\_pad\_pdn\_3

Number\_of\_terminals = 4

1  Buf\_Rail     signal\_name VDD  |  VDD         POWER

2 Pad\_Rail     signal\_name VDD  |  VDD         POWER

3  Buf\_Rail     signal\_name VSS  |  VSS         GND

4 Pad\_Rail     signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 9: Same full IBIS-ISS configuration with PDN as in Example 8, except

| that IO connections are direct from buf\_pin while the PDN connections are

| from buf\_pad and pad\_pin using the signal\_name qualifier – since there are | no terminal conflicts with this set, this should work

[Interconnect Model Set] Full\_ISS\_IO\_buf\_pad\_pin\_PDN\_sn\_7

|-----

[Begin Interconnect Model] Full\_ISS\_buf\_pin\_IO

File\_IBIS-ISS full\_buf\_pin.iss full\_buf\_pin\_typ

Number \_of\_terminals = 11

1 Pin\_I/O pin\_name A1 | DQ1 DQ

2 Pin\_I/O pin\_name A2 | DQ2 DQ

3 Pin\_I/O pin\_name A3 | DQ3 DQ

4 Pin\_I/O pin\_name D1 | DQS+ DQS

5 Pin\_I/O pin\_name D2 | DQS- DQS

6 Buf\_I/O pin\_name A1 | DQ1 DQ

7 Buf\_I/O pin\_name A2 | DQ2 DQ

8 Buf\_I/O pin\_name A3 | DQ3 DQ

9 Buf\_I/O pin\_name D1 | DQS+ DQS

10 Buf\_I/O pin\_name D2 | DQS- DQS

11 Pin\_Rail signal\_name VSS | Reference at the Pin\_Rail

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_pad\_pin\_PDN\_3

File\_IBIS-ISS full\_iss\_pad\_pin\_pdn\_3.iss full\_iss\_pad\_pin\_pdn\_3

Number\_of\_terminals = 4

1 Pin\_Rail signal\_name VDD | VDD POWER

2 Pad\_Rail signal\_name VDD | VDD POWER

3 Pin\_Rail signal\_name VSS | VSS GND

4 Pad\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_buf\_pad\_PDN\_3

File\_IBIS-ISS full\_iss\_buf\_pad\_pdn\_3 full\_iss\_buf\_pad\_pdn\_3

Number\_of\_terminals = 4

1 Buf\_Rail signal\_name VDD | VDD POWER

2 Pad\_Rail signal\_name VDD | VDD POWER

3 Buf\_Rail signal\_name VSS | VSS GND

4 Pad\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 10: Terminals A1\_A3 set up for and IBIS-ISS connections with coupling

| for cross-talk analysis – Aggressor terminals at the Buffer are designated

[Interconnect Model Set] A1\_A3\_DQ\_TS\_XTALK

|-----

[Interconnect Model] A1\_A3\_DQ\_TS\_buf\_pin\_XTALK

File\_IBIS-ISS dq\_iss\_buf\_pin\_xtalk.s6p

Number\_of\_terminals = 6

1 Pin\_I/O     pin\_name A1 Aggressor

2 Buf\_I/O  pin\_name A1 Aggressor

3 Pin\_I/O     pin\_name A2

4 Buf\_I/O  pin\_name A2

5 Pin\_I/O     pin\_name A3 Aggressor

6 Buf\_I/O  pin\_name A3 Aggressor

7 Buf\_PD\_Ref pin\_name A1 | Reference Node

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 11: Same as Example 10, but with a PDN network added

[Interconnect Model Set] A1\_A3\_DQ\_TS\_XTALK\_ISS\_PDN

|-----

[Interconnect Model] A1\_A3\_DQ\_TS\_buf\_pin\_XTALK

File\_IBIS-ISS dq\_iss\_buf\_pin\_xtalk.s6p

Number\_of\_terminals = 6

1 Pin\_I/O pin\_name A1 Aggressor

2 Buf\_I/O pin\_name A1 Aggressor

3 Pin\_I/O pin\_name A2

4 Buf\_I/O pin\_name A2

5 Pin\_I/O pin\_name A3 Aggressor

6 Buf\_I/O pin\_name A3 Aggressor

7 Buf\_PD\_Ref pin\_name A1 | Reference Node

[End Interconnect Model]

[Begin Interconnect Model] Full\_ISS\_buf\_pin\_PDN\_2

File\_IBIS-ISS full\_iss\_buf\_pin\_pdn\_2.iss full\_iss\_buf\_pad\_PDN\_2

Number\_of\_terminals = 4

1 Pin\_Rail signal\_name VDD | VDD POWER

2 Buf\_Rail signal\_name VDD | VDD POWER

3 Pin\_Rail signal\_name VSS | VSS GND

4 Buf\_Rail signal\_name VSS | VSS GND

[End Interconnect Model]

[End Interconnect Model Set]

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 12 applies to the configuration below

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

A4    DQ4         DQ

P1    VDD         POWER

P2    VDD         POWER

G1    VSS         GND

G2    VSS         GND

[Bus Label] signal\_name

VDD1 VDD

VDD2 VDD

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

A1            VSS           VDD1        NC            NC              NC

A2            VSS           VDD1        NC            NC              NC

A3            VSS           VDD2        NC            NC              NC

A4            VSS           VDD2        NC            NC              NC

| ... Entries below can be deleted and replaced with [Bus Label] per [Pin

| Mapping] BIRD

P1            NC           VDD1        NC            NC              NC

P2            NC           VDD2        NC            NC              NC

G1            VSS           NC         NC            NC              NC

G2            VSS           NC         NC            NC              NC

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

| Example 12: Full IBIS-ISS configuration with PDN described using both

| bus\_label and signal\_name qualifiers for the Rails

[Interconnect Model Set] Full\_ISS\_IO\_PDN\_bl\_sn\_6

|-----

[Interconnect Model] Full\_ISS\_buf\_pin\_IO\_4

File\_IBIS-ISS full\_iss\_buf\_pin\_io\_4.iss full\_iss\_buf\_pin\_IO\_4\_typ

Number\_of\_terminals = 9

1  Pin\_I/O     pin\_name A1  |  DQ1         DQ

2  Pin\_I/O      pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     pin\_name A4  |  DQ4         DQ

5 Buf\_I/O  pin\_name A1  |  DQ1         DQ

6 Buf\_I/O  pin\_name A2  |  DQ2         DQ

7 Buf\_I/O  pin\_name A3  |  DQ3         DQ

8 Buf\_I/O  pin\_name A4  |  DQ4         DQ

9 Pin\_Rail signal\_name VSS | Reference for I/Os

[End Interconnect Model]

[Interconnect Model] Full\_ISS\_PDN\_bl\_sn

File\_IBIS-ISS buf\_pin\_pdn.iss buf\_pin\_PDN\_typ

Number\_of\_terminals = 5

1  Pin\_Rail     signal\_name VDD  |  VDD         POWER

2  Pin\_Rail     signal\_name VSS  |  VSS         GND

|

3 Buf\_Rail  bus\_label VDD1  |  VDD         POWER

4 Buf\_Rail  bus\_label VDD2  |  VDD         POWER

5 Buf\_Rail  signal\_name VSS  |  VSS         GND

[End Interconnect Model]

[End Interconnect Model Set]

| The EDA tool connects the terminals and pins as follows:

|

| 1 Pins P1 and P2

| 2 Pins G1 and G2

| 3 Buf\_PU\_Ref of buffers A1 and A2

| 4 Buf\_PU\_Ref of buffers A3 and A4

| 5 Buf\_PD\_Ref of buffers A1, A2, A3 and A4

|\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

*Keyword:* [**End Interconnect Model**]

*Required:* Yes, for each instance of the [Interconnect Model] keyword

*Description:* Indicates the end of the Interconnect Model data.

*Other Notes:* Between the [Interconnect Model] and [End Interconnect Model] keywords is the package model data itself. The data describes any number of interfaces to either IBIS-ISS models or Touchstone files.

*Example:*

[End Interconnect Model]

The following text should be added to the list in section 3, GENERAL SYNTAX RULES AND GUIDELINES.

15. The underscore (‘\_’) character may be used interchangeably with a space in this document to refer to keywords, subparameters, column headers, etc. For example, “bus\_label” and “bus label” are synonymous.

The following sub-sections should be appended after 3.1, Keyword Hierarchy:

**3.2 RULES OF PRECEDENCE**

The sections below detail the rules of precedence to be assumed by EDA tools and model makers where multiple keywords may support similar functions.

**3.2.1 PACKAGES**

The order of precedence for package model data to be used by EDA tools in simulation is defined below, in ascending order. If a package data format at a numerically higher position on the list is available in an IBIS or related file, that data shall be used by the EDA tool for simulation.

1. [Component]/[Package]
2. [Component]/[Pin]
3. [Package Model] (including [Alternate Package Models] and [Define Package Model])
4. [Interconnect Model Set Selector]

Note that [External Circuit] and [Interconnect Model Set Selector] shall not be present within the same [Component]. [Package Model] and [Interconnect Model Set Selector] may both be present for the same [Component] but only if they either refer to completely independent pins (terminals), or if they refer to entirely overlapping groups of pins (terminals).