**Proposed New IBIS Terminal Syntax**

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Terminal rules:

Terminal records shall appear after the Number\_of\_Terminals subparameter and before the [End Interconnect Model] keyword.

Each Terminal line contains information on a terminal of an IBIS-ISS subckt (or Touchstone file).

Terminal records are of the form

<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> Aggressor

Terminal\_number

Terminal\_number is an identifier for a specific terminal. Terminal\_number shall be a positive non-zero integer less than or equal to the value of the Number\_of\_Terminals argument. The same Terminal\_number shall not appear more than once for a given Interconnect Model. If any Terminals are not present for a given Interconnect Model, then those terminals are unused, and shall be terminated according to the Unused\_Terminal\_Termination rules.

There are three classes of pins in a component, Signal Pins, Supply Pins and No Connect Pins. Supply Pins have model\_name POWER or GND. No Connect Pins have model\_name NC. All other pins are classified as Signal Pins. Package models defined in this section assume that there is one Buffer\_I/O Terminal and one Die Pad for each Signal Pin.

The model of an I/O Buffer has supply terminals in addition to the Buffer\_I/O. These supply (or rail) terminals can be PUref, PDref, PCref, GCref and/or EXTref. The association of the PUref, PDref, PCref, GCref and/or EXTref terminal of a buffer are associate with either bus\_label or signal\_name in the [Pin Mapping] section. These terminals can be connected to interconnect models one of two ways:

1. By specifying a unique interconnect terminal for each I/O Buffer PUref, PDref, PCref, GCref and/or EXTref
2. By assuming that all I/O Buffer supply terminals connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal for all I/O Buffer terminals that are connected to a specific signal\_name or bus\_label on at least one Supply Pin.

Pads are the location of the interface between the die and the package. Interconnect models can either be between the Pins of a component and the I/O Buffers, or they can be split into models between the Pins of a component and the Pads of the die, and model between the Pads of the die and the I/O Buffer models. There is exactly one Pad (Pad\_I/O) for each Signal Pin. There can be any number of Pads (Pad\_Rail) for each signal\_name or buf\_label on Supply Pins. If interconnect models of supply (rail) networks are split between Pin/Pad and Pad/Buffer models, then the interface of supply connections at the die package interface can be handled in one of two ways:

1. By defining a list of Die Supply Pads, and specifying terminals for some or all of the Die Supply Pads that are connected to a bus\_label or signal\_name on at least one Supply Pin.
2. By assuming that all supply Pads connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal for all Pads that are connected to a specific signal\_name on at least one Supply Pin.

Pins can be terminals of the interconnect model that connect directly to a PCB board or other type of system connection to an IBIS component. Pins can be Signal Pins (Pin\_I/O), or Supply Pins (Pin\_Rail). An interconnect model can connect supply pins in one of two ways:

1. By specifying terminals for some or all of the Supply Pins.
2. By assuming that all supply Pins connected to a supply signal\_name or bus\_label are shorted together. This is done by specifying a unique terminal for all Pins that are connected to a specific signal\_name on at least one Supply Pin.

Terminal\_type must be one of the following: Buffer\_I/O, PUref, PDref, PCref, GCref, EXTref, Buffer\_Rail, Pad\_I/O, Pad\_Rail, Pin\_I/O or Pin\_Rail. Buffer\_I/O, PUref, PDref, PCref, GCref, EXTref and Buffer\_Rail are terminals of an Interconnect Model that connect directly to I/O Buffers. Pin\_I/O and Pin\_Rail are terminals that are at the Die/Package interface. Pin\_I/O and Pin\_Rail are terminals that are at the Component PCB interface. The Terminal\_type\_qualifier for Terminal\_types Buffer\_I/O, PUref, PDref, PCref, GCref and EXTref must be pin\_name. The Terminal\_type\_qualifier for Terminal\_type Buffer\_Rail may be signal\_name or bus\_label.

The Terminal\_type\_qualifier for Terminal\_type Pad\_I/O must be pin\_name.

The Terminal\_type\_qualifier for Terminal\_type Pad\_Rail must be either pad\_name, signal\_name or bus\_label.

The Terminal\_type\_qualifier for Terminal\_type Pin\_I/O must be pin\_name.

The Terminal\_type\_qualifier for Terminal\_type Pin\_Rail must be either pin\_name, signal\_name or bus\_label.

The optional Aggressor field is only allowed allowed on Buffer\_I/O records. Connections to Buffer\_I/O terminals may be missing coupling to connects that are not included in this interconnect model.

The following table summarized the rules described above.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Terminal\_Type | pin\_name | signal\_name | bus\_label | pad\_name | Aggressor |
| Buffer\_I/O | X |  |  |  | A |
| Puref | X |  |  |  |  |
| Pdref | X |  |  |  |  |
| Pcref | X |  |  |  |  |
| Gcref | X |  |  |  |  |
| EXTref | X |  |  |  |  |
| Buffer\_rail |  | Y | Y |  |  |
| Pad\_I/O | X |  |  |  |  |
| Pad\_rail |  | Y | Y | Z |  |
| Pin\_I/O | X |  |  |  |  |
| Pin\_rail | Y | Y | Y |  |  |

For an Interconnect Model using File\_TS with N ports, N is determined from the [Number of Ports] field in a Touchstone 2 file. The [Number of Terminals] in the Interconnect Model shall be N+1. Terminal rules are described below:

* The EDA tool shall use the Pin\_name or Signal\_name specified for the associated Terminal “N+1” entry as the reference node for each of the N ports.
* Terminal/Port Mapping
  + Terminal              Port
  + 1                              1
  + 2                              2
  + …
  + N                             N
  + N+1 reference
* If a Port is not connected, then it shall be terminated by the EDA tool with a resistor to the node on Terminal N+1. The resistance shall be the Port Reference Impedance.
* It shall be an error if Terminal N+1 is not specified to be connected to a Pin, a Pad, or a Buffer that is not part of a connection to a Signal\_name that is POWER or GND

*Examples:*

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

D1    DQS+        DQS

D2    DQS-        DQS

P1    VDD         POWER

P2    VDD         POWER

P3    VDD         POWER

P4    VDD         POWER

P5    VDD         POWER

G1    VSS         GND

G2    VSS         GND

G3    VSS         GND

G4    VSS         GND

[Diff Pin] inv\_pin  vdiff  tdelay\_typ tdelay\_min tdelay\_max

D1          D2       NA     NA         NA         NA

[Die Supply Pads]  signal\_name

VDD1 VDD

VDD2 VDD

VDD3 VDD

VSS1 VSS

VSS2 VSS

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

Bus\_label\_signal\_name

A1            VSS          VDD        NC            NC              NC

A2            VSS          VDD        NC            NC              NC

A3            VSS          VDD        NC            NC              NC

D1            VSS          VDD        NC            NC              NC

D2            VSS          VDD        NC            NC              NC

| Full Package/Die Model Complex Power Distribution

Number\_of\_Terminals 29

1  Pin\_I/O     Pin\_name A1  |  DQ1         DQ

2  Pin\_I/O     Pin\_name A2  |  DQ2         DQ

3  Pin\_I/O     Pin\_name A3  |  DQ3         DQ

4  Pin\_I/O     Pin\_name D1  |  DQS+        DQS

5  Pin\_I/O     Pin\_name D2  |  DQS-        DQS

6  Pin\_I/O     Pin\_name P1  |  VDD         POWER

7  Pin\_I/O     Pin\_name P2  |  VDD         POWER

8  Pin\_I/O     Pin\_name P3  |  VDD         POWER

9  Pin\_I/O     Pin\_name P4  |  VDD         POWER

10 Pin\_Rail    Pin\_name P5  |  VDD         POWER

11 Pin\_Rail    Pin\_name G1  |  VSS         GND

12 Pin\_Rail    Pin\_name G2  |  VSS         GND

13 Pin\_Rail    Pin\_name G3  |  VSS         GND

14 Pin\_Rail    Pin\_name G4  |  VSS         GND

15 Buffer\_I/O  Pin\_name A1  |  DQ1         DQ

16 Buffer\_I/O  Pin\_name A2  |  DQ2         DQ

17 Buffer\_I/O  Pin\_name A3  |  DQ3         DQ

18 Buffer\_I/O  Pin\_name D1  |  DQS+        DQS

19 Buffer\_I/O  Pin\_name D2  |  DQS-        DQS

20 PUref   Pin\_name A1  |  DQ1         DQ

21 PUref   Pin\_name A2  |  DQ2         DQ

22 PUref   Pin\_name A3  |  DQ3         DQ

23 PUref   Pin\_name D1  |  DQS+        DQS

24 PUref   Pin\_name D2  |  DQS-        DQS

25 PDref   Pin\_name A1  |  DQ1         DQ

26 PDref   Pin\_name A2  |  DQ2         DQ

27 PDref   Pin\_name A3  |  DQ3         DQ

28 PDref   Pin\_name D1  |  DQS+        DQS

29 PDref   Pin\_name D1  |  DQS+        DQS

| Full Package/Die Model Simple Power Distribution

Number\_of\_Terminals 14

1  Pin\_I/O     Pin\_name A1         |  DQ1         DQ

2  Pin\_I/O     Pin\_name A2         |  DQ2         DQ

3  Pin\_I/O     Pin\_name A3         |  DQ3         DQ

4  Pin\_I/O     Pin\_name D1         |  DQS+        DQS

5  Pin\_I/O     Pin\_name D2         |  DQS-        DQS

6  Pin\_Rail    signal\_name   VDD   |  VDD         POWER

7  Pin\_Rail    signal\_name   VSS   |  VSS         GND

8  Buffer\_I/O  Pin\_name A1         |  DQ1         DQ

9  Buffer\_I/O  Pin\_name A2         |  DQ2         DQ

10 Buffer\_I/O  Pin\_name A3         |  DQ3         DQ

11 Buffer\_I/O  Pin\_name D1         |  DQS+        DQS

12 Buffer\_I/O  Pin\_name D2         |  DQS-        DQS

13 Buffer\_Rail signal\_name   VDD   |  VDD         POWER

14 Buffer\_Rail signal\_name   VSS   |  VSS         GND

| Single DQ (A1)

Number\_of\_Terminals 2

1 Pin\_I/O     Pin\_name A1

2 Buffer\_I/O  Pin\_name A1

| Single DQ (A1) , Split into package and on-die models

Number\_of\_Terminals 2

1 Pin\_I/O     Pin\_name A1

2 Pad\_I/O     Pin\_name A1

Number\_of\_Terminals 2

1 Pad\_I/O     Pin\_name A1

2 Buffer\_I/O  Pin\_name A1

Full VDD Power Supply Model

Number\_of\_Terminals 9

1 Pin\_Rail   Pin\_name P1  |  VDD         POWER

2 Pin\_Rail   Pin\_name P2  |  VDD         POWER

3 Pin\_Rail   Pin\_name P3  |  VDD         POWER

4 Pin\_Rail   Pin\_name P4  |  VDD         POWER

5 Pin\_Rail   Pin\_name P5  |  VDD         POWER

6 PDref Pin\_name A1  |  DQ1         DQ

7 PDref Pin\_name A2  |  DQ2         DQ

8 PDref Pin\_name A3  |  DQ3         DQ

9 PDref Pin\_name D1  |  DQS+        DQS

Full VDD Power Supply Model split into package and on-die

Number\_of\_Terminals 8

1 Pin\_Rail Pin\_name P1   |  VDD         POWER

2 Pin\_Rail Pin\_name P2   |  VDD         POWER

3 Pin\_Rail Pin\_name P3   |  VDD         POWER

4 Pin\_Rail Pin\_name P4   |  VDD         POWER

5 Pin\_Rail Pin\_name P5   |  VDD         POWER

6 Pad\_Rail Pad\_name VDD1 |  VDD         POWER

7 Pad\_Rail Pad\_name VDD2 |  VDD         POWER

8 Pad\_Rail Pad\_name VDD3 |  VDD         POWER

Number\_of\_Terminals 7

1 Pad\_Rail Pad\_name VDD1 |  VDD         POWER

2 Pad\_Rail Pad\_name VDD2 |  VDD         POWER

3 Pad\_Rail Pad\_name VDD3 |  VDD         POWER

4 PDref  Pin\_name A1   |  DQ1         DQ

5 PDref  Pin\_name A2   |  DQ2         DQ

6 PDref  Pin\_name A3   |  DQ3         DQ

7 PDref  Pin\_name D1   |  DQS+        DQS

Power supply model assuming pins shorted, pads shorted, and buffer rail shorted

Number\_of\_Terminals 2

1 Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Buffer\_Rail  signal\_name VDD  |  VDD         POWER

Power supply model assuming pins shorted, pads shorted, and buffer rail shorted, split between package and die

Number\_of\_Terminals 2

1 Pin\_Rail      signal\_name VDD  |  VDD         POWER

2 Pad\_Rail      signal\_name VDD  |  VDD         POWER

Number\_of\_Terminals 2

1 Pad\_Rail      signal\_name VDD  |  VDD         POWER

2 Buffer\_Rail   signal\_name VDD  |  VDD         POWER

| Single DQ Crosstalk Model

Number\_of\_Terminals 6

1 Pin\_I/O     Pin\_name A1

2 Buffer\_I/O  Pin\_name A1 Aggressor

3 Pin\_I/O     Pin\_name A2

4 Buffer\_I/O  Pin\_name A2

5 Pin\_I/O     Pin\_name A3

6 Buffer\_I/O  Pin\_name A3 Aggressor

Example with signal\_name split into bus\_labels

*Examples:*

[Pin] signal\_name model\_name      R\_pin   L\_pin   C\_pin

A1    DQ1         DQ

A2    DQ2         DQ

A3    DQ3         DQ

A4    DQ4         DQ

P1    VDD         POWER

P2    VDD         POWER

G1    VSS         GND

G2    VSS         GND

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref ext\_ref

Bus\_label\_signal\_name

A1            VSS           VDD1        NC            NC              NC

A2            VSS           VDD1        NC            NC              NC

A3            VSS           VDD2        NC            NC              NC

A4            VSS           VDD2        NC            NC              NC

P1            NC           VDD1        NC            NC              NC

P2            NC           VDD2        NC            NC              NC

G1            VSS           NC         NC            NC              NC

G2            VSS           NC         NC            NC              NC

Power supply model assuming pins shorted, pads shorted, and buffer rail shorted

Number\_of\_Terminals 2

1 Pin\_Rail     signal\_name VDD  |  VDD         POWER

2 Pin\_Rail     signal\_name VSS  |  VSS         GND

3 Buffer\_Rail  bus\_label VDD1 |  VDD         POWER

4 Buffer\_Rail  bus\_label VDD2 |  VDD         POWER

5 Buffer\_Rail  signal\_name VSS  |  VDD         POWER

EDA tool hooks up the following terminals to …

1 Pins P1 and P2

2 Pins G1 and G2

3 PUref of buffers A1 and A2

4 PUref of buffers A3 and A4

5 PDref of buffers A1, A2, A3 and A4