**TOUCHSTONE ISSUE RESOLUTION DOCUMENT (TSIRD)**

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**ISSUE TITLE:** Standardized Port Mapping

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**DEFINITION OF THE ISSUE:**

When using Touchstone models, it is essential to know how their ports should be connected in a design. This implies that the “port ordering” or “port mapping” information must be supplied along with or inside the Touchstone file. Currently, this is information is sometimes provided in a separate file, but increasingly more often it is included in the Touchstone file as a commented “header” section.

When a Touchstone file contains many ports, connecting its ports manually becomes a tedious and error-prone job. Consequently automation is highly desired. EDA vendors developed several different formats throughout the years, but the problem is that they are all different with various degrees of features and capabilities, making it difficult to parse them with software. Additionally, in most cases this information is provided as a commented header section in the Touchstone file, and strictly speaking, comments are non-parsable, arbitrary text.

The goal of this proposal is to provide a standardized port mapping format for Touchstone files so that all relevant information could be included in it, and all EDA tools could parse them reliably.

**SOLUTION REQUIREMENTS:**

Port Mapping data must be able to support:

1. Reliably, hooking up a Touchstone File in a simulation.
2. Automate creating a schematic symbol.
3. Automate generating/verifying [Interconnect Model]s in .ibs files.
4. Automate generating/verifying [EMD Model]s in .emd files.
5. Automate generating/verifying [C Comp Model]s in .ibs files.
6. Enable Touchstone File viewers to generate mixed-mode S-parameters for differential ports.
7. Sij Status (Measured | Simulated | TBD | Placeholder)
8. Automatic generation of test probe locations for test equipment.
9. Swathing
10. Ability to add new user defined parameters

The Touchstone specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Define two new keywords | [Begin Port Map] / [End Port Map] |
|  |  |
|  |  |
|  |  |

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table 2: Touchstone Keywords Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
|  |  |  |

**PROPOSED CHANGES:**

**Add the following keywords to the Touchstone specification in the appropriate location:**

*Keyword:* **[Begin Port Map] / [End Port Map]**

*Required:* Optional; illegal prior to Version 3.0.

*Description:* Identifies and associates physical, schematic, and optionally measurement locations with the port numbers specified in a Touchstone file

*Sub-Params:* IBIS\_file, EMD\_file, C\_comp\_model\_file, Ts4file, Source, Swathing, Group, Symbol\_leftside, Symbol\_topside, Symbol\_rightside, Symbol\_bottomside, Sij\_status, User\_defined, Port

*Usage rules:* If present in the file, the [Begin Port Map] / [End Port Map] keyword pair shall immediately follow the [Number of Ports] keyword and its associated data. Each subparameter shall start on a new line.

The following optional subparameters identify what the Touchstone file port map is describing; only one of these subparameters is permitted per [Begin Port Map]/[End Port Map] keyword pair.

The **IBIS\_file** subparameter is optional. It is followed by an IBIS file name and component. If present, this Touchstone file represents an [Interconnect Model] that is present in the named IBIS file.

The **EMD\_file** subparameter is optional. It is followed by an EMD file name. If present, this Touchstone file represents an [EMD Model] that is present in the named EMD file.

The **C\_comp\_model\_file** subparameter is optional. It is followed by a C Comp Model file name. If present, this Touchstone file represents an IBIS C Comp Model that is present in named model file.

The **Ts4file** subparameter is optional. It is followed by an IBIS

The **Source** subparameter is optional. It is followed by a file name identifying the original file where the Touchstone data was obtained or derived. The file name may be an ODB++ board data base, a schematic file, a simulation model, or any other data file. As the subparameter is purely informational, the data file is not required to be present on the computer system containing the associated Touchstone file.

The **Swathing** subparameter is optional. It is followed by a string, defining a Schema name. There are several ways that connector companies create Touchstone files for a slice (e.g., 3 wafers of a connector) of a connector that can be combined algorithmically to create a virtual Touchstone file that represents all the pins of the connector. Separately, both Reserved Schemas, and other, model-maker-defined Schema values will be supported.

The subparameter . string The rs, inclusive argument valueand

The **Group** subparameter is optional. Group may appear multiple times for a [Begin Port Map]/[End Port Map] pair, with each Group subparameter appearing on a separate line. These lines are placed after the last Port subparameter (see below) and the [End Port Map] keyword. The Group subparameter is followed by a white space and the name of the Group whose port is described by the line. This Group <name> is followed by a white space, a “(“, followed by a list of Physical names, and terminated by a “)”. Any Physical port names (see below) cannot be used as Group names. An EOL (end of line character) without a “)” will continue the list of Physical names on the next line.

The **Symbol\_leftside** subparameter is optional. These lines are placed after the last Port subparameter and the [End Port Map] keyword. The Symbol\_left subparameter string is followed by a list of Port numbers that can be terminals on the left side of a schematic symbol ordered top to bottom.

The **Symbol\_rightside** subparameter is optional. These lines are placed after the last Port Subparameter and the [End Port Map] keyword. The Symbol\_right subparameter string is followed by a list of Port numbers that can be terminals on the right side of a schematic symbol ordered top to bottom.

The **Symbol\_topside** subparameter is optional. These lines are placed after the last Port Subparameter and the [End Port Map] keyword. The Symbol\_top subparameter string is followed by a list of Port numbers that can be terminals on the top side of a schematic symbol ordered left to right.

The **Symbol\_bottomside** subparameter is optional. These lines are placed after the last Port Subparameter and the [End Port Map] keyword. The Symbol\_bottomside subparameter string is followed by a list of Port numbers that can be terminals on the bottom side of a schematic symbol ordered left to right.

If any Symbol\_leftside, Symbol\_rightside, Symbol\_topside or Symbol\_bottomside subparameters are present then any Port number shall appear once and only once in these subparameters.

The User\_defined subparameter is optional. It shall be followed by one or more strings within the same pair of parentheses. These subparameters are effectively ignored by the parser and EDA tools, but may be used by recipients to track whether physical measurements have been conducted on a Port, and/or how the Port data was measured.

Examples:

(Status Measured)

(Probe\_Angle 15)

The **Port** subparameter is required. The [Begin Port Map] keyword shall be followed by as many Port subparameter lines as the number of ports defined by the [Number of Ports] keyword. The entire content of each Port subparameter shall be on a single line.

The Port subparameter is followed by a white space and an integer number, indicating which port is described by the line. Note that the Port number shall be larger than zero and shall be smaller than or equal to the Number of Ports entry in the same Touchstone file. The integer port number is followed by a white space, then (<name> <value>) pairs enclosed in parentheses. Unless otherwise noted, all Port subparameter pairs are optional. Subparameter names are case-sensitive.

Several names are reserved and shall not be used as values or arguments to Port subparameters. These are listed below:

Diff\_Port

Logical

Net

Physical

Reference

Side

The Port subparameter and its value shall appear first, at the beginning of each line. All other name/value pairs may appear in any order thereafter.

Examples:

Port 1 (Physical U7.1)

Port 2 (Physical U7.3) (Logical DQ5+) (Diff\_Port 3)

Port 3 (Physical U7.4) (Logical DQ5-) (Diff\_Port 2)

**Port Subparameter Name Rules**

**Type**: The value is either S or P. S stands for Signal, P stands for Power (in other words, rail). If not specified, the Type default is S.

**Physical**: The value is a string that describes the physical location of the terminal used to generate the Port network data. This can be a pin on a component, a set of coordinates identifying the location of a probe, or a sheet and node location for a schematic. The string should clearly indicate to a human where, for instance, the probe used to measure the S-parameter data is placed, or how to connect to the described network element in a circuit simulator. For a printed circuit board (PCB), the argument to “Physical” should either be a reference designator (also called a “refdes”), followed by a dot and a pin number (e.g., U7.3), or an X,Y, Layer.. There are special rules that can be followed to automatically connect the element described by the Touchstone network data in IBIS and EMD [Interconnect Model]s and in IBIS [C\_comp\_Model]s. If the value is provided in the Bus\_Label:<name> format, then <name> shall be either defined in the IBIS or EMD file, or defined in the Bus\_Labels subparameter section.

Allowed Physical names for C Comp Models:

Buffer\_I/O

Buffer\_I

Pullup\_ref

Pulldown\_ref

Power\_clamp\_ref

Gnd\_clamp\_ref

Ext\_Ref

A\_gnd

Rules for [EMD Model]s:

For Type S Ports, the Physical name shall be either the EMD Pin\_name or a designator.pin\_name

For Type P Ports, the Physical name shall be either the EMD Pin\_name, a designator.pin\_name, a Bus\_Label.name or Group.name

Rules for IBIS [Interconnect Model]s:

For Type S Ports, the Physical name shall be either pin.<pin\_name>, pad.<pin\_name> or buf.<pin\_name>

For Type P Ports, the Physical name shall be either pin.pin\_name, pad.pin\_name The list of Bus\_Label pins can be determined from the associated .ibs file. Rail connections to the buffer shall be in one of the following formats:

Pullup\_ref.<pin\_name>

Pulldown\_ref.pin\_name

Power\_clamp\_ref.pin\_name

Gnd\_clamp\_ref.pin\_name

Pullup\_ref.Bus\_label:<name>

Pulldown\_ref. Bus\_label:<name>

Power\_clamp\_ref. Bus\_label:<name>

Gnd\_clamp\_ref. Bus\_label:<name>

Pullup\_ref.Group:<name>

Pulldown\_ref.Group:<name>

Power\_clamp\_ref. Group:<name>

Gnd\_clamp\_ref. Group:<name>

ext\_ref?

**Logical**: The Logical value identifies a grouping of ports to be used in a schematic symbol for the Touchstone file.

**Net**: The Net value identifies a grouping for generation of simulation or schematic topologies. All ports that have the same Net value are part of the same signal path (this does not mean they share the same node, as in a short).

**Side**: The Side value identifies a grouping, for connecting elements described by Touchstone network data in larger structures across multiple components. A Touchstone-described interconnect file often has two sides (e.g., a connector between a mainboard and daughterboard). A memory DQ route may have a Controller Side, and separate Sides for each memory device connected to that route. A cable assembly for a car may have four Sides (e.g., CPU, Brake, Engine, and Camera).

**Diff\_Port:** The Diff\_Port value identifies the given Port as one-half of a differential pair, and states the Port number of the complementary port. Polarity is not directly indicated, since this will be established by how the port is used by the differential models in simulation. Each port declared as a Diff\_port shall have a corresponding (complementary) Diff\_port declaration.

**Reference**: The Reference value identifies the physical location of the reference terminals used for probing (measurement). If more than one reference is needed, the value shall be in the format Bus\_Label:<Bus\_Label name> or Group:<Group name>.

Example 1: 4 pin cable from CPU to Sensor.

[Begin Port Map]

Port 1 (Physical A.1) (Side CPU) (Net 1)

Port 2 (Physical A.2) (Side CPU) (Net 2)

Port 3 (Physical A.3) (Side CPU) (Net 3)

Port 4 (Physical A.4) (Side CPU) (Net 4)

Port 5 (Physical B.1) (Side Sensor) (Net 1)

Port 6 (Physical B.2) (Side Sensor) (Net 2)

Port 7 (Physical B.3) (Side Sensor) (Net 3)

Port 8 (Physical B.4) (Side Sensor) (Net 4)

Symbol\_left 1 2 3 4

Symbol\_right 5 6 7 8

(Add Short Cuts e.g., NFNF NNFF, Gonzalez, Bogatin, IEEE)

[End Port Map]

Example 2: Transistor

[Begin Port Map]

Port 1 (Logical Emitter)

Port 2 (Logical Base)

Port 3 (Logical Collector)

Symbol\_left 1

Symbol\_right 3

Symbol\_bottom 2

[End Port Map]

Example 3: A 8” coplanar wave guide. (probe has 3 connections: 1 signal and 2 references)

[Begin Port Map]

Port 1 (Physical 0.:0.:Top) (Side Left) (Net 1) (Reference Group:GND\_L)

Port 2 (Physical 8.:0.:Top) (Side Right) (Net 1) (Reference Group:GND\_R)

Group GND\_L (0.:.1:Top 0.:-.1:Top)

Group GND\_R (8.:.1:Top 8.:-.1:Top)

[End Port Map]

Example 4: Single ended IBIS package model between pin and pad on pin 7.

[Begin Port Map]

Port 1 (Physical pin.7) (Side Pin) (Net 7) (Logical DQ3pin)

Port 2 (Physical pad.7) (Side Pad) (Net 7) (Logical DQ3pad)

[End Port Map]

Example 5: Single ended IBIS package model between pin and buffer on pin 7, including VDD voltage port.

[Begin Port Map]

Port 1 (Physical pin.7) (Type S) (Side Pin) (Net 7) (Logical DQ3pin)

| Type S is redundant, as this is the default

Port 2 (Physical buffer.7) (Type S) (Side buffer) (Net 7) (Logical DQ3buffer)

| Type S is redundant, as this is the default

Port 3 (Physical Pin.Bus\_label:VDD) (Type P) (Side Pin) (Net VDD) (Logical VDDpin)

Port 4 (Physical Pullup\_ref.7) (Type P) (Side Buffer) (Net VDD) (Logical VDDbuffer)

[End Port Map]

Example 6: Single-ended connection between U1.7 and U3.5 for a PCB.

[Begin Port Map]

Port 1 (Physical U1.7) (Side U1) (Net DQ3) (Logical CPU)

Port 2 (Physical U3.5) (Side U3) (Net DQ3) (Logical SDRAM)

[End Port Map]

Example 7: EMD of a 4 bit DQ nibble in a 2 rank DIMM

[Begin Port Map]

Port 1 (Physical 20) (Side EMD) (Net DQ0) (Logical DQ0)

Port 2 (Physical 21) (Side EMD) (Net DQ1) (Logical DQ1)

Port 3 (Physical 22) (Side EMD) (Net DQ2) (Logical DQ2)

Port 4 (Physical 23) (Side EMD) (Net DQ3) (Logical DQ3)

Port 5 (Physical 25) (Side EMD) (Net DQS+) (Logical DQS+) (Diff\_port 6)

Port 6 (Physical 26) (Side EMD) (Net DQS-) (Logical DQS-) (Diff\_port 5)

Port 7 (Physical 27) (Side mem1) (Net DQ0) (Logical mem1\_DQ0)

Port 8 (Physical 28) (Side mem1) (Net DQ1) (Logical mem1\_DQ1)

Port 9 (Physical 29) (Side mem1) (Net DQ2) (Logical mem1\_DQ2)

Port 10 (Physical 30) (Side mem1) (Net DQ3) (Logical mem1\_DQ3)

Port 11 (Physical 31) (Side mem1) (Net DQS+) (Logical mem1\_DQS+) (Diff\_port 12)

Port 12 (Physical 32) (Side mem1) (Net DQS-) (Logical mem1\_DQS-) (Diff\_port 11)

Port 13 (Physical 33) (Side mem2) (Net DQ0) (Logical mem2\_DQ0)

Port 14 (Physical 34) (Side mem2) (Net DQ1) (Logical mem2\_DQ1)

Port 15 (Physical 35) (Side mem2) (Net DQ2) (Logical mem2\_DQ2)

Port 16 (Physical 36) (Side mem2) (Net DQ3) (Logical mem2\_DQ3)

Port 17 (Physical 37) (Side mem2) (Net DQS+) (Logical mem2\_DQS+) (Diff\_port 18)

Port 18 (Physical 38) (Side mem2) (Net DQS-) (Logical mem2\_DQS-) (Diff\_port 17)

[End Port Map]

**BACKGROUND INFORMATION/HISTORY:**

TBD