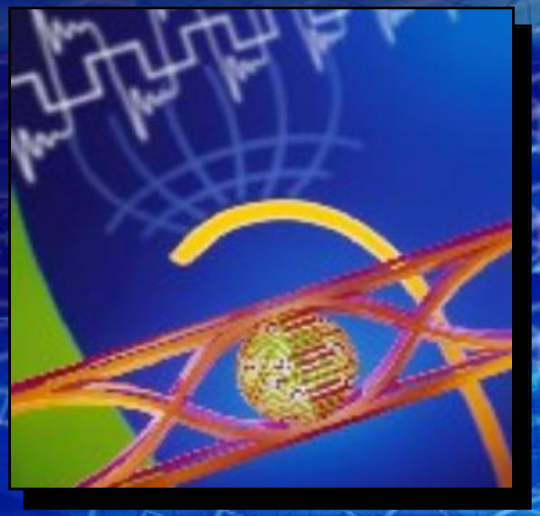
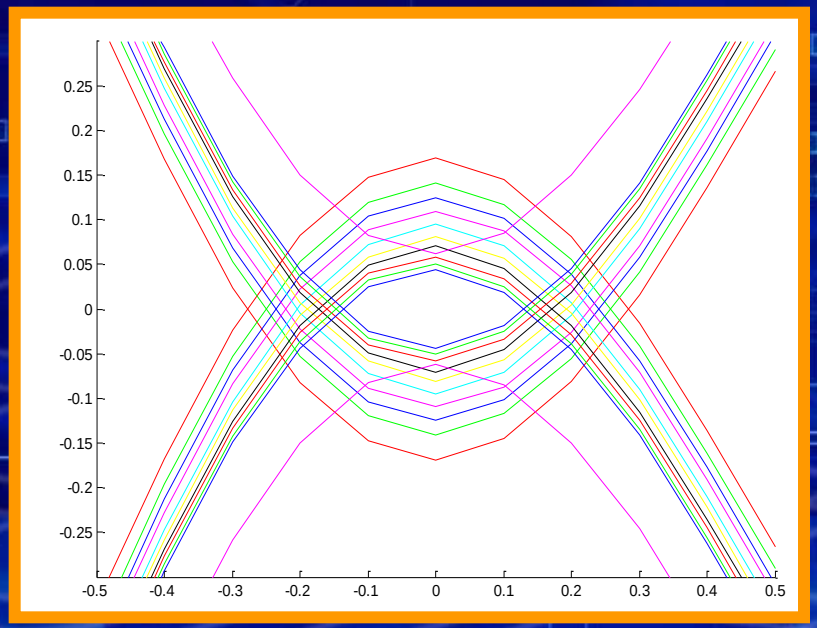
Package and On-die Interconnect Modeling in IBIS

IBIS ATM Teleconference
October 1, 2013





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Introduction

- **The following slides demonstrate how the various use cases described in SiSoft's presentation (discussed in the September 24, 2013 ATM meeting) can be implemented using the BIRD 125 concepts**
  http://www.vhdl.org/pub/ibis/macromodel_wip/archive/20130924/walterkatz/Package%20and%20On-Die%20Interconnect%20rev3/Package_On_Die_Interconnect_3.pdf

- **The examples below contain some deviations from BIRD 125.1, because since it was last updated (July 2011), the need for new features have been identified**
  http://www.eda.org/ibis/birds/bird125.1.txt
  - **BIRD 125.1 can be easily adopted to embrace these deviations**
  - **some syntax rules need to be finalized**

Package modeling

SiSoft's Slide 6

EMD Like Solution for IBIS Component Packaging – IBIS File

- The IBIS File
  - [Component] sdram
  - [IBIS_ISS_Package] sdram.pkg
  - [PIN] signal_name model_name R_pin L_pin C_pin
  - A1 VDD POWER
  - A2 VSS GND
  - B7 DQ1 DQ
  - C2 DQ0 DQ
  - D3 DQ2 DQ
  - D7 DQ3 DQ

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SiSoft's Slide 7

sdram.pkg 2 Terminal s2p or subckt for each Pin

```
(sdram
   (DQ0  | s2p for this specific pin (C2)
      (Tstonefile_File (Corner DQ0_typ.s2p DQ0_min.s2p DQ0_max.s2p))
      (Terminals
         (1 (Pin (Pin_Name C2)))
         (2 (Pad (Pad_Name C2)))
      )
   )
 (DQ1  | s2p for this specific pin (B7)
      (Tstonefile_File (Corner DQ1_typ.s2p DQ1_min.s2p DQ1_max.s2p))
      (Terminals (1 (Pin (Pin_Name B7)))(2 (Pad (Pad_Name B7))))
 (DQ2  | s2p for this specific pin (D3 )
      (Tstonefile_File (Corner DQ2_typ.s2p DQ2_min.s2p DQ2_max.s2p))
      (Terminals (1 (Pin (Pin_Name D3)))(2 (Pad (Pad_Name D3))))
 (DQ3  | 2 terminal subckt for this specific pin (B7)
      (IBIS_ISS_File (Value DQ3_typ.mod))
      (Subckt (Corner DQ3_typ DQ3_min DQ3_max))
      (Terminals (1 (Pin (Pin_Name D7)))(2 (Pad (Pad_Name D7))))
...
```

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Slide 6/7 implemented with BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

SDRAM_pkg.cir file:

```
************************************************************
.SUBCKT  S_pkg  P1  P2
+ TSFile="TouchstoneFileName.s2p"

Sdriver  P1  P2
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
************************************************************
.ends
```

IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        4
|
[Pin Numbers]  die_ports
B7   IDP_B7
C2   IDP_C2
D3   IDP_D3
D7   IDP_D7
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQ1_typ.s2p"
Ports  B7  IDP_B7
[End Package Circuit]
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQ0_typ.s2p"
Ports  C2  IDP_C2
[End Package Circuit]
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQ2_typ.s2p"
Ports  D3  IDP_D3
[End Package Circuit]
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQ3_typ.s2p"
Ports  D7  IDP_D7
[End Package Circuit]
|
[End Package Model]
```

SiSoft's Slide 8

sdram.pkg 2 Terminal s2p or subckt for each Pin, one parameterized subckt

```
...
 (DQ0   | parameterized subckt for this specific pin (C2)
      (IBIS_ISS_File (Value DQ.mod))
      (Subckt (Value DQ))
      (Parameters
           (Framis (Corner 0 -1 1))
           (Length (Value .02)))
       (Terminals
         (1 (Pin (Pin_Name C2)))
         (2 (Pad (Pad_Name C2)))))
 (DQ1   | parameterized subckt for this specific pin (C2)
      (IBIS_ISS_File (Value DQ.mod))
      (Subckt (Value DQ))
      (Parameters
           (Framis (Corner 0 -1 1))
           (Length (Value .01)))
       (Terminals
         (1 (Pin (Pin_Name B7)))
         (2 (Pad (Pad_Name B7)))))
...
```

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Slide 6/8 implemented with BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        4
|
[Pin Numbers]  die_ports
B7   IDP_B7
C2   IDP_C2
D3   IDP_D3
D7   IDP_D7
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  DQ.mod  DQ
Parameters  Framis = 0
Parameters  Length = 0.01
Ports  B7  IDP_B7
[End Package Circuit]
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  DQ.mod  DQ
Parameters  Framis = 0
Parameters  Length = 0.02
Ports  C2  IDP_C2
[End Package Circuit]
|
|…
|…
|…
[End Package Model]
```

DQ.mod file:

```
************************************************************
.SUBCKT  DQ  P1  P2
+ Framis=0  Length=1
…
…
…
************************************************************
.ends
```

SiSoft's Slide 9

S2p for each Model

```
 ...
(DQ   | s2p for this specific model (DQ)
  (Tstonefile_File (Corner DQ_typ.s2p DQ_min.s2p DQ_max.s2p))
  (Terminals
     (1 (Pin (Model_Name DQ)(Connection 1)))
     (2 (Pad (Model_Name DQ)(Connection 1))))
))
...
```

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Slide 6/9 implemented with (modified) BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        0   | Or we can make this required only
|                           | with the [Pin Numbers] keyword
|
[Model Names]   pin_names   pad_names   connections
DQ   SomeDQpin_1   SomeDQpad_1   1
|
| We could define a reserved node name for this type of connections
| so that the model maker shouldn't have to come up with bogus names.
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQ_typ.s2p"
Ports  SomeDQpin_1  SomeDQpad_1
[End Package Circuit]
|
|…
|…
|…
[End Package Model]
```

SDRAM_pkg.cir file:

```
*********************************************************
.SUBCKT  S_pkg  P1  P2
+ TSFile="TouchstoneFileName.s2p"

Sdriver  P1  P2
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
*********************************************************
.ends
```

SiSoft's Slide 10

s8p for full DQ bus

```
 ...
(DQall   | s8p for all DQ bus signal pins
  (Tstonefile_File (Corner DQall_typ.s8p DQall_min.s8p DQall_max.s8p))
  (Terminals
     (1 (Pin (Pin_Name C2)(Connection 1)))
     (2 (Pin (Pin_Name B7)(Connection 2)))
     (3 (Pin (Pin_Name D3)(Connection 3)))
     (4 (Pin (Pin_Name D7)(Connection 4)))
     (5 (Pad (Pad_Name C2)(Connection 1)))
     (6 (Pad (Pad_Name B7)(Connection 2)))
     (7 (Pad (Pad_Name D3)(Connection 3)))
     (8 (Pad (Pad_Name D7)(Connection 4)))
))
...
```

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Slide 6/10 implemented with BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        4
|
[Pin Numbers]  die_ports  connections
| Note that the "connection" column is really not needed here
| but it is shown for consistency with the SiSoft example
B7   IDP_B7   2
C2   IDP_C2   1
D3   IDP_D3   3
D7   IDP_D7   4
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQall_typ.s8p"
Ports  B7  IDP_B7
Ports  C2  IDP_C2
Ports  D3  IDP_D3
Ports  D7  IDP_D7
[End Package Circuit]
|
[End Package Model]
```

SDRAM_pkg.cir file:

```
*********************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4  P5  P6  P7  P8
+ TSFile="TouchstoneFileName.s8p"

Sdriver  P1  P2  P3  P4  P5  P6  P7  P8
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
*********************************************************
.ends
```

SiSoft's Slide 11

S10p for full DQ bus and Vdd

```
 ...
(DQvdd  | s10p for all DQ bus signal pins
  (Tstonefile_File (Corner DQvdd_typ.s10p DQvdd_min.s10p DQvdd_max.s10p))
  (Terminals
     (1 (Pin (Pin_Name C2)(Connection 1)))
     (2 (Pin (Pin_Name B7)(Connection 2)))
     (3 (Pin (Pin_Name D3)(Connection 3)))
     (4 (Pin (Pin_Name D7)(Connection 4)))
     (5 (Pad (Pad_Name C2)(Connection 1)))
     (6 (Pad (Pad_Name B7)(Connection 2)))
     (7 (Pad (Pad_Name D3)(Connection 3)))
     (8 (Pad (Pad_Name D7)(Connection 4)))
     (9 (Pin (Pin_Name A1)(Connection 5)))
     (10 (Pad (Pad_Name A1)(Connection 5)))
))
...
```


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Slide 6/11 implemented with BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        5
|
[Pin Numbers]  die_ports  connections
| Note that the "connection" column is really not needed here
| but it is shown for consistency with the SiSoft example
A1   IDP_A1   5
B7   IDP_B7   2
C2   IDP_C2   1
D3   IDP_D3   3
D7   IDP_D7   4
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQvdd_typ.s10p"
Ports  B7  IDP_B7
Ports  C2  IDP_C2
Ports  D3  IDP_D3
Ports  D7  IDP_D7
Ports  A1  IDP_A1
[End Package Circuit]
|
[End Package Model]
```

SDRAM_pkg.cir file:

```
**********************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4  P5  P6  P7  P8  P9  P10
+ TSFile="TouchstoneFileName.s10p"

Sdriver  P1  P2  P3  P4  P5  P6  P7  P8  P9  P10
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
**********************************************************
.ends
```

SiSoft's Slide 12

S10p for DQ0 and Vdd

```
 ...
(DQ0vdd  | s10p for DQ0 signal and vdd
  (Tstonefile_File (Corner DQvdd_typ.s10p DQvdd_min.s10p DQvdd_max.s10p))
  (Terminals
     (1 (Pin (Pin_Name C2)(Connection 1)))
     (5 (Pad (Pad_Name C2)(Connection 1)))
     (9 (Pin (Pin_Name A1)(Connection 2)))
     (10 (Pad (Pad_Name A1)(Connection 2)))
))
...
```

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Slide 6/12 implemented with BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        2
|
[Pin Numbers]  die_ports  connections
| Note that the "connection" column is really not needed here
| but it is shown for consistency with the SiSoft example
A1   IDP_A1   2
C2   IDP_C2   1
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQvdd_typ.s10p"
Ports  NC  NC           | "NC" stands for "no connect".  The IBIS
Ports  C2  IDP_C2       | specification will have to define the rules
Ports  NC  NC           | for the EDA tool and model maker to ensure
Ports  NC  NC           | that these types of models work properly.
Ports  A1  IDP_A1
[End Package Circuit]
|
[End Package Model]
```

SDRAM_pkg.cir file:

```
**********************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4  P5  P6  P7  P8  P9  P10
+ TSFile="TouchstoneFileName.s10p"

Sdriver  P1  P2  P3  P4  P5  P6  P7  P8  P9  P10
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
**********************************************************
.ends
```

SiSoft's Slide 13

s4p for any DQ and one aggressor

```
 ...
(DQ_1ag | s4p for any DQ signal and one worst case aggressor
  (Tstonefile_File (Corner DQ_1ag_typ.s4p DQ_1ag_min.s4p DQ_1ag_max.s4p))
  (Terminals
     (1 (Pin (Model_Name DQ)(Victim 1)))
     (2 (Pad (Model_Name DQ)(Victim 1)))
     (3 (Pin (Model_Name DQ)(Aggressor 2)))
     (4 (Pad (Model_Name DQ)(Aggressor 2)))
))
...
(DQ0_1ag | s4p for DQ0 signal and one worst case aggressor
 (Tstonefile_File (Corner DQ0_1ag_typ.s4p DQ0_1ag_min.s4p DQ0_1ag_max.s4p))
 (Terminals
     (1 (Pin (Pin_Name C2)(Victim 1)))
     (2 (Pad (Pad_Name C2)(Victim 1)))
     (3 (Pin (Model_Name DQ)(Aggressor 2)))
     (4 (Pad (Model_Name DQ)(Aggressor 2)))
))
...
```

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Slide 6/13a implemented with (modified) BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        0   | Or we can make this required only
|                           | when the [Pin Numbers] keyword exists
|
[Model Names]   pin_names   pad_names   vi/ag
DQ   SomeDQpin_1   SomeDQpad_1   victim_1
DQ   SomeDQpin_2   SomeDQpad_2   aggressor_2
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQ_lag_typ.s4p"
Ports  SomeDQpin_1  SomeDQpad_1
Ports  SomeDQpin_2  SomeDQpad_2
[End Package Circuit]
|
|…
|…
|…
[End Package Model]
```

SDRAM_pkg.cir file:

```
**********************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4
+ TSFile="TouchstoneFileName.s4p"

Sdriver  P1  P2  P3  P4
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
**********************************************************
.ends
```

Slide 6/13b implemented with (modified) BIRD 125

IBIS file:

```
[Component] SDRAM
|
[PIN]  signal_name  model_name  R_pin  L_pin  C_pin
|
A1   VDD   POWER
A2   VSS   GND
B7   DQ1   DQ
C2   DQ0   DQ
D3   DQ2   DQ
D7   DQ3   DQ
|
[Package Model] SDRAM_pkg
|
[Model]  DQ
|…
|…
|…
```

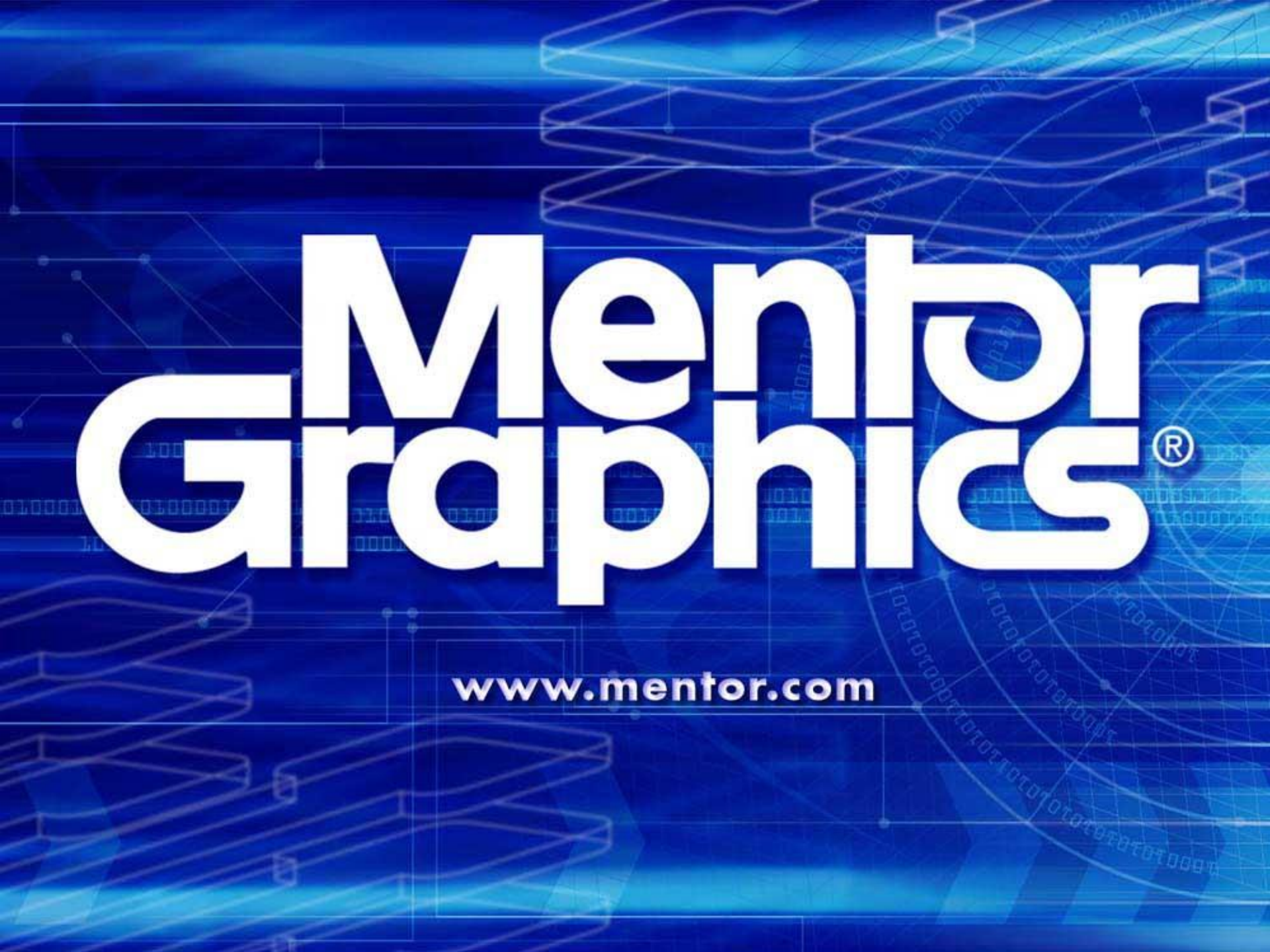
IBIS SDRAM.pkg file:

```
[Define Package Model]  SDRAM_pkg
[Manufacturer]          Some Company
[OEM]                   Some Company
[Description]           An SDRAM package model
[Number Of Pins]        1   | This refers only to the number of
|                           | pins listed under [Pin Numbers]
|
[Pin Numbers]  die_ports  vi/ag
C2   IDP_C2   victim_1

[Model Names]   pin_names   pad_names   vi/ag
DQ   SomeDQpin_2   SomeDQpad_2   aggressor_2
|
[Package Circuit]
Language IBIS-ISS
Corner  Typ  SDRAM_pkg.cir  S_pkg
Parameters  TSFile = "DQ_lag_typ.s4p"
Ports  C2           IDP_C2
Ports  SomeDQpin_2  SomeDQpad_2
[End Package Circuit]
|
|…
|…
|…
[End Package Model]
```

SDRAM_pkg.cir file:

```
************************************************************
.SUBCKT  S_pkg  P1  P2  P3  P4
+ TSFile="TouchstoneFileName.s4p"

Sdriver  P1  P2  P3  P4
+ MNAME=TSFile
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
************************************************************
.ends
```

On-die interconnect modeling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