Backchannel Co-Optimization Requirements

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Introduction

- Serial Link performance is affected by both TX and RX EQ settings

- Some EQ behavior can overlap (TX post-cursor and RX CTLE / DFE taps)

- Optimizing system performance involves balancing the contributions of TX & RX EQ (SiSoft calls this TX/RX co-optimization)

- System Designers perform multiple TX/RX co-optimization tasks before production release

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TX/RX Co-optimization: Design Tasks

1. Emulate H/W training protocol in a backchannel compliant system
   - Identify required starting settings to ensure successful system level training
2. Co-optimize TX/RX settings based on different performance criteria (eye height, area, etc.)
3. Verify system performance using fixed, partially fixed & completely adaptive EQ settings
4. Predict BER / Operating Margin
5. Identify SerDes settings

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TX/RX Co-optimization: Requirements

1. Support existing AMI simulation modes
2. Support cross-vendor optimization
3. Support high-throughput (Statistical) and detailed (Time-Domain) simulation flows
4. Identify optimized TX/RX settings in a standard way
5. Optimized results reflect actual hardware capabilities (tap extents, tap granularity)
6. Enable mapping between simulation results and H/W register settings
7. Use all possible combinations of model optimization, Statistical and Time Domain capabilities

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Flows "Backchannel" Should Support

- Statistical with no co-optimization
- Time Domain with no co-optimization
- Statistical co-optimization followed by
  - Statistical "Simulation"
  - Time Domain "Simulation"
- Time Domain co-optimization followed by
  - Statistical "Simulation"
  - Time Domain "Simulation"
- Statistical co-optimization followed by Time Domain co-optimization followed by
  - Statistical "Simulation"
  - Time Domain "Simulation"

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