BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)

BIRD NUMBER: ???
ISSUE TITLE: Power Pin Package Modeling
REQUESTOR: Arpad Muranyi, Mentor Graphics, Randy Wolff, Micron Technology, Inc.
DATE SUBMITTED: March 31, 2015
DATE REVISED: ???
DATE ACCEPTED BY IBIS OPEN FORUM: ???

STATEMENT OF THE ISSUE:

Under the [Package] keyword, the IBIS specification defines a set of rules on the hierarchy of the various package modeling options. It is clearly stated that when present, the package information under the [Pin] keyword will override the package information in the [Package] keyword, and if present the information in the [Package Model] and [Define Package Model] keywords will override the information in the [Pin] and [Package] keywords.

The rules for the [Pin Numbers] keyword in the [Define Package Model] keyword section do not prohibit a "partial package model", i.e. a model which only describes a subset of a Component's pins. The problem is that the IBIS specification does not define the hierarchy rules for the situation when the [Define Package Model] contains only a partial package model. In the absence of rules, model makers and EDA tool vendors may make different assumptions, which may lead to incorrect simulation results. For example, for missing package parasitics under the [Define Package Model] keyword one might assume that the package parasitics from the [Pin] or [Package] keyword should be used, but other assumptions might implement an open or short in such cases.

ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:

The IBIS specification requires that the R, L and C matrices should be the same size. This makes it nearly impossible to generate RLC data with a simulator and convert it into the IBIS matrix format. The C matrix will never have the same size as the R and L matrices unless there is never more than one pin connected to each power or ground path. The equivalent SPICE model would have only one C element but multiple RL elements. To generate a valid C matrix of the same size as the R and L matrices, model makers would have to post-process the RLC data that was generated by the field solver and create multiple C values from a single C value. All mutual C values would have to be created in a similar fashion as well.

Using the [Package]/[Pin] RLC data for ***signal pins*** not defined in [Define Package Model] is ***acceptable***, however, ***the same rule is difficult at best to apply to power and ground pins*** and it seems that it is better not to use RLC data from the [Package]/[Pin] keywords for power and ground pins not defined in [Define Package Model].

For data in the [Pin] keyword, representing the capacitance of a plane on multiple pins is an issue. In addition, there is no way to define critically important mutual inductances and capacitances.

For data in the [Package] keyword, the problem revolves around the min/max values. People use the min/max values based on the signal parasitics, which is useless for the power/ground corner cases.

It seems that the only way to provide valid RLC data for power integrity (PI) simulations is by placing it into the [Define Package Model] keyword, and by merging multiple power/ground pins into one pin while leaving the remaining pins in the group undefined or disconnected.

A simple update to the IBIS specification proposed in this BIRD describes the rules that when the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e. pads), the package parasitics of those power/ground pins should be merged into a single pin representation per group in the [Define Package Model] keyword and only one of the pin names for each of those groups should be present in the [Pin Numbers] keyword of the [Define Package Model] keyword.

Even though the new package/on-die interconnect specification proposal for IBIS is expected to resolve these problems, it might still be worth adding this change for the legacy package modeling syntax, since there may be numerous models which will never use the new package modeling syntax.

ANY OTHER BACKGROUND INFORMATION:

This issue was discussed in a series of emails with Randy Wolff and Aniello Viscardi of Micron Technology, Inc. during the weeks of March, 2015 and in the March 31, 2015 Advanced Technology Modeling Task Group. The proposal presented in this BIRD is based on these discussions.

On pg. 140 add a new subparameter name Merged_pins to the list of subparameters under the [Pin Numbers] keyword.

On pg. 140 change the following paragraph under the [Pin Numbers] keyword:

Usage Rules: Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as there are pins (as given by the preceding [Number Of Pins] keyword). Pin names cannot exceed 5 characters in length. The first pin name given is the "lowest" pin, and the last pin given is the "highest." If the [Number Of Sections] keyword is used then each pin name must be followed by one or more of the legal subparameter combinations listed below. If the [Number Of Sections] keyword is not present then subparameter usage is NOT allowed.

to:

Usage Rules: Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as the number of pins given by the preceding [Number Of Pins] keyword, but it is not required to include all of the pins listed under the [Pin] keyword. When an undefined pin in [Define Package Model] is a signal pin, the EDA tool shall first look for the package RLC values for that pin under the [Pin] keyword. If this information is not available there, the EDA tool shall make use of the package RLC values in the [Package] keyword.

When the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e. pads), the package parasitics of one or more groups of power/ground pins may be merged into one or more single pin representations. The Merged_pins subparameter identifies the pins under the [Pin Numbers] keyword which contain merged power/ground package information and provides a list of pins whose package parasitics have been merged into that pin. The EDA tool shall short the merged pins (not die pads) with each other and with the pin that contains their combined package effects with an ideal short. Also, the EDA tool shall use an open circuit between the merged pin and its corresponding die pads to eliminate any interference with the package parasitics defined by the pin that contains the merged package model data.

Note that power integrity (PI) analysis including the package parasitics on power and ground nets is not possible with Components which do not contain power/ground bus definitions using the [Pin Mapping] keyword together with the [Define Package Model] keyword, because key pieces of information on how power is distributed between the power and ground pins and the power terminals of buffer [Model]s are not available for the simulator.

Pin names cannot exceed 5 characters in length. The first pin name given is the "lowest" pin, and the last pin given is the "highest." If the [Number Of Sections] keyword is used then each pin name must be followed by one or more of the legal subparameter combinations listed below. If the [Number Of Sections] keyword is not present, only subparameter Merged_pins is allowed, otherwise only subparameters Len, L, R, C, Fork, Endfork are allowed.

On pg. 140 add a new subparameter description as follows:

The subparameter Merged_pins is optional. When used, it is placed after the pin name under the [Pin Numbers] keyword. Its purpose is to define the pin that it follows as a pin containing merged power or ground package data. The subparameter is only allowed after pin names which appear as Power or GND pins in the [Pin] keyword and are also included in a power or ground bus definition in the [Pin Mapping] keyword.

The subparameter name is followed by a list of pin names. The pin names must be separated by at least one white space. The list may span multiple lines if needed, but each new line must begin with the subparameter name Merged_pins. The list of pins is terminated by a new pin name at the beginning of a new line continuing the [Pin Numbers] keyword's pin list, or a new valid IBIS keyword.

Each pin name in this list must match the name of a Power or GND pin in the [Pin] keyword and must also be a member of the same power or ground bus of which the pin that is followed by this subparameter is a member. The Merged_pins subparameter may only list pin names which are not part of the pin list defined by the [Pin Numbers] keyword, i.e. pins for which the [Define Package Model] keyword does not define a package model. The Merged_pins subparameter must list the name of all those pins whose package parasitics have been merged into the pin that is followed by the subparameter.

On pg. 141 add the following example (or the relevant portion of it):

```
|*****************************************************************************
| COMPONENT: MT40A256M16HA (96-Ball FBGA, x16)
|*****************************************************************************
|
[Component]     MT40A256M16HA
[Package Model] z80a_96ball_pkg
[Manufacturer]  Micron Technology, Inc.
[Package]
|               typ          min           max
R_pkg           283.8m       190.8m        437.9m
L_pkg           1.564nH      0.808nH       2.677nH
C_pkg           0.396pF      0.302pF       0.559pF
|
[Pin]   signal_name          model_name     R_pin    L_pin    C_pin
A1      VDDQ                 POWER
A2      VSSQ                 GND
A8      VSSQ                 GND
A9      VDDQ                 POWER
B1      VPP                  POWER
B2      VSS                  GND
B3      VDD                  POWER
B9      VDD                  POWER
C1      VDDQ                 POWER
C9      VSSQ                 GND
D1      VDD                  POWER
D2      VSSQ                 GND
```

```
D8      VSSQ                GND
D9      VDDQ                POWER
E1      VSS                 GND
E3      VSSQ                GND
E8      VSSQ                GND
E9      VSS                 GND
F1      VSSQ                GND
F2      VDDQ                POWER
F8      VDDQ                POWER
G1      VDDQ                POWER
G7      VDD                 POWER
G8      VSS                 GND
G9      VDDQ                POWER
H1      VSSQ                GND
H9      VSSQ                GND
J1      VDD                 POWER
J2      VDDQ                POWER
J8      VDDQ                POWER
J9      VDD                 POWER
K1      VSS                 GND
K9      VSS                 GND
L1      VDD                 POWER
L9      VDD                 POWER
M1      VREFCA              POWER
M9      VSS                 GND
N1      VSS                 GND
R1      VDD                 POWER
R9      VPP                 POWER
T1      VSS                 GND
T9      VDD                 POWER
|
|************************PIN MAPPING*****************************************
|
[Pin Mapping]   pulldown_ref    pullup_ref      gnd_clamp_ref   power_clamp_ref
ext_ref
A1              NC              VDDQ
A2              VSS             NC
A8              VSS             NC
A9              NC              VDDQ
B1              NC              VPP
B2              VSS             NC
B3              NC              VDD
B9              NC              VDD
C1              NC              VDDQ
C9              VSS             NC
D1              NC              VDD
D2              VSS             NC
D8              VSS             NC
D9              NC              VDDQ
E1              VSS             NC
E3              VSS             NC
E8              VSS             NC
E9              VSS             NC
F1              VSS             NC
F2              NC              VDDQ
F8              NC              VDDQ
G1              NC              VDDQ
```

```
G7              NC              VDD
G8              VSS             NC
G9              NC              VDDQ
H1              VSS             NC
H9              VSS             NC
J1              NC              VDDL
J2              NC              VDDQ
J8              NC              VDDQ
J9              NC              VDD
K1              VSSL            NC
K9              VSS             NC
L1              NC              VDD
L9              NC              VDD
M1              NC              VREFCA
M9              VSS             NC
N1              VSS             NC
R1              NC              VDD
R9              NC              VPP
T1              VSS             NC
T9              NC              VDD
|
|*****************************************************************************
| Sparse Matrix Package Model for z80a_96ball_pkg (x16)
|*****************************************************************************
|
[Define Package Model]  z80a_96ball_pkg
[Manufacturer]  Micron Technology, Inc.
[OEM]   Micron Technology, Inc.
[Description]  z80a package model for 96-Ball FBGA
[Number of Pins]        91
[Pin Numbers]
A1 |VDDQ
A2 |VSSQ
A8 |VSSQ
A9 |VDDQ
B1 |VPP
B2 |VSS
B3 |VDD
B9 |VDD
C1 |VDDQ
C9 |VSSQ
D1 |VDD
D2 |VSSQ
D8 |VSSQ
D9 |VDDQ
E1 |VSS
E3 |VSSQ
E8 |VSSQ
| Merged VSS
E9 Merged_pins K9 M9 N1 T1
F1 |VSSQ
| Merged VDDQ
F2 Merged_pins G9
F8 |VSS
G1 |VDDQ
G7 |VDD
G8 |VSS
```

```
H1 |VSSQ
H9 |VSSQ
J1 |VDDL
J2 |VDDQ
J8 |VDDQ
J9 |VDD
K1 |VSSL
L1 |VDD
L9 |VDD
M1 |VREFCA
R1 |VDD
R9 |VPP
T9 |VDD
|
[Model Data]
[Inductance Matrix]     Sparse_Matrix
|...
```