BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)

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ISSUE TITLE: Power Pin Package Modeling
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STATEMENT OF THE ISSUE:

Under the [Package] keyword, the IBIS specification defines a set of rules on the hierarchy of the various package modeling options. It is clearly stated that when present, the package information under the [Pin] keyword will override the package information in the [Package] keyword, and if present the information in the [Package Model] and [Define Package Model] keywords will override the information in the [Pin] and [Package] keywords.

The rules for the [Pin Numbers] keyword in the [Define Package Model] keyword section do not prohibit a "partial package model", i.e., a model which only describes a subset of a Component's pins. The problem is that the IBIS specification does not define the hierarchy rules for the situation when the [Define Package Model] contains only a partial package model. In the absence of rules, model makers and EDA tool vendors may make different assumptions, which may lead to incorrect simulation results. For example, for missing package parasitics under the [Define Package Model] keyword one might assume that the package parasitics from the [Pin] or [Package] keyword should be used, but other assumptions might implement an open or short in such cases.

ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:

The IBIS specification requires that the R, L and C matrices should be the same size. This makes it nearly impossible to generate RLC data with a simulator and convert it into the IBIS matrix format. The C matrix will never have the same size as the R and L matrices unless there is never more than one pin connected to each power or ground path. The equivalent SPICE model would have only one C element but multiple RL elements. To generate a valid C matrix of the same size as the R and L matrices, model makers would have to post-process the RLC data that was generated by the field solver and create multiple C values from a single C value. All mutual C values would have to be created in a similar fashion as well.

Using the [Package]/[Pin] RLC data for ***signal pins*** not defined in [Define Package Model] is ***acceptable***, however, ***the same rule is difficult at best to apply to power and ground pins*** and it seems that it is better not to use RLC data from the [Package]/[Pin] keywords for power and ground pins not defined in [Define Package Model].

For data in the [Pin] keyword, representing the capacitance of a plane on multiple pins is an issue. In addition, there is no way to define critically important mutual inductances and capacitances.

For data in the [Package] keyword, the problem revolves around the min/max values. People use the min/max values based on the signal's package parasitics, which is useless for the power/ground corner cases.

It seems that the only way to provide valid RLC data for power integrity (PI) simulations is by placing it into the [Define Package Model] keyword, and by merging multiple power/ground pins into one pin while leaving the remaining pins in the group undefined or disconnected.

A simple update to the IBIS specification proposed in this BIRD describes the rules that when the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e., pads), the package parasitics of those power/ground pins should be merged into a single pin representation per group in the [Define Package Model] keyword and only one of the pin names for each of those groups should be present in the [Pin Numbers] keyword of the [Define Package Model] keyword.

Even though the new package/on-die interconnect specification proposal for IBIS is expected to resolve these problems, it might still be worth adding this change for the legacy package modeling syntax, since there may be numerous models which will never use the new package modeling syntax.

ANY OTHER BACKGROUND INFORMATION:

This issue was discussed in a series of emails with Randy Wolff and Aniello Viscardi of Micron Technology, Inc. during the weeks of March, 2015 and in the March 31 and April 7, 2015 Advanced Technology Modeling Task Group Teleconferences. The proposal presented in this BIRD is based on these discussions.

On pg. 137 add a new line to the table for the new proposed [Merged Pins] keyword as follows:

Table 1 – Package Modeling Keywords

Keyword	Notes
[Define Package Model]	Required if the [Package Model] keyword is used
[Manufacturer]	(note 1)
[OEM]	(note 1)
[Description]	(note 1)
[Number Of Sections]	(note 2)
[Number Of Pins]	(note 1)
[Pin Numbers]	(note 1)
[Merged Pins]	Optional when [Model Data] is used, otherwise illegal
[Model Data]	(note 2)
[Resistance Matrix]	Optional when [Model Data] is used
[Inductance Matrix]	(note 3)
[Capacitance Matrix]	(note 3)
[Bandwidth]	Required (for Banded_matrix matrices only)
[Row]	(note 3)
[End Model Data]	(note 2)
[End Package Model]	(note 1)

Note 1 Required when the [Define Package Model] keyword is used

Note 2 Either the [Number Of Sections] or the [Model Data]/[End Model Data] keywords are required. Note that [Number of Sections] and the [Model Data]/[End Model Data] keywords are mutually exclusive.

Note 3 Required when the [Define Package Model] keyword is used and the [Number Of Sections] keyword is not used.

On pg. 140 change the following paragraph under the [Pin Numbers] keyword:

Usage Rules: Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as there are pins (as given by the preceding [Number Of Pins] keyword). Pin names cannot exceed 5 characters in length. The first pin name given is the "lowest" pin, and the last pin given is the "highest." If the [Number Of Sections] keyword is used then each pin name must be followed by one or more of the legal subparameter combinations listed below. If the [Number Of Sections] keyword is not present then subparameter usage is NOT allowed.

to:

Usage Rules: Following the [Pin Numbers] keyword, the names of the pins are listed. There must be as many names listed as the number of pins given by the preceding [Number Of Pins] keyword, but it is not required to include all of the pins listed under the [Pin] keyword. Pin names cannot exceed 5 characters in length. The first pin name given is the "lowest" pin, and the last pin given is the "highest." If the [Number Of Sections] keyword is used then each pin name must be followed by one or more of the legal subparameter combinations listed below. If the [Number Of Sections] keyword is not present then subparameter usage is NOT allowed.

For pins that are not listed under the [Pin Numbers] keyword in the [Define Package Model] section, i.e., pins whose package model is not defined in the [Define Package Model] keyword, the EDA tool is expected to first look for the package RLC values under the [Pin] keyword. If this information is not available there, the EDA tool is expected to make use of the package RLC values in the [Package] keyword. However, the EDA tool is expected to use an open circuit between those pins and their corresponding pads that are not listed under the [Pin Numbers] keyword but are connected to a bus (defined by the [Pin Mapping] keyword) where the bus includes another pin that is listed under the [Pin Numbers] keyword.

On pg. 142 add a new keyword description before the [Model Data] keyword as follows:

Keyword: **[Merged Pins]**

Required: Optional when [Model Data] is used, otherwise illegal

Description: When the [Pin Mapping] keyword defines power/ground buses that span over multiple power/ground pins (i.e., pads), the package parasitics of one or more groups of power/ground pins may be merged into one or more single pin representations. The [Merged Pins] keyword declares the package model for the pin whose name follows the [Merged Pin] keyword as a merged package model and lists the names of the pins whose package parasitics have been merged into this merged package model.

Usage Rules: This keyword may optionally be used when the [Model Data] keyword is present in the [Define Package Model] section. When used, it must be placed after the end of the pin list defined by the [Pin Numbers] keyword and before the [Model Data] keyword. The keyword must be followed by one pin name on the same line on which the keyword appears, separated by at least one white space. This pin name must be listed under the [Pin Numbers] keyword, it must be listed as a POWER or GND pin under the [Pin] keyword and it must also be a member of a power or

ground bus defined by the [Pin Mapping] keyword. This is the pin whose package model contains the merged package model data for a group of power or ground pins.

The line on which the [Merged Pins] keyword appears must be followed by a new line providing a list of one or more pin names, which are separated by at least one white space. The list may be on a single line or span multiple lines and is terminated by either another [Merged Pins] keyword or the [Model Data] keyword.

Each pin name in the list must match the name of a POWER or GND pin in the [Pin] keyword and must also be a member of the same power or ground bus of which the pin that follows the [Merged Pins] keyword is a member, but pin names in this list may not be present in the pin list under the [Pin Numbers] keyword. In other words, the pins in the list should not have a package model defined under the [Define Package Model] keyword. The list must include the name of all those pins whose package parasitics have been merged into the pin that follows the [Merged Pins] keyword.

The EDA tool is expected to connect all of the pins (not die pads) named in the [Merged Pins] keyword together with an ideal short.

Other Notes: Note that power integrity (PI) analysis including the package parasitics on power and ground nets is not possible with Components which do not contain power/ground bus definitions using the [Pin Mapping] keyword together with the [Define Package Model] keyword, because key pieces of information on how power is distributed between the power and ground pins and the power terminals of buffer [Model]s are not available for the simulator. For PI analysis, at least one power/ground pin should be included in [Pin Numbers] from each power/ground bus defined in [Pin Mapping] for a given signal pin's buffer. If no power/ground pins are defined, ideal power/ground connections based on the [Voltage Range] and/or the [* Reference] keywords can be assumed. However, there is insufficient information for PI analysis.

Example:

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[Manufacturer]  ACME, Inc.
[OEM]  ACME, Inc.
[Description]  FBGA Package Model for x4 Data Pins and POWER/GND
[Number of Pins]  13
[Pin Numbers]
A1 |VDD
A2 |VSSQ
A8 |VSSQ
A9 |VSS
B2 |VDDQ
B3 |DQS_c
B7 |DQ1
C2 |DQ0
C3 |DQS_t
C7 |VDD
D3 |DQ2
D7 |DQ3
D9 |VSSQ
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[Merged Pins] A1
H1 M1 | Merged VDD

[Merged Pins] C7
F9 J9 N9 | Merged VDD (electrically in parallel with A1, shorted at the die)

[Merged Pins] A9
C8 E9 G1 H9 K1 K9 N1 | Merged VSS

[Merged Pins] A2
D1 | Merged VSSQ (electrically in parallel with A8 and D9, shorted at the die)

[Merged Pins] B2
B8 C1 C9 E2 E8 | Merged VDDQ
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