Buffer Rail Mapping
Ground in Legacy Package Models

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July 7, 2015

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[Buffer Rail Mapping]

- The [Buffer Rail Mapping] keyword names the connections between POWER and/or GND pins and buffer and/or terminator voltage supply references using Signal_name.
- What [Pin Mapping] should have been.
- Records similar to [Pin Mapping] records.
- Assume [Component] [Pin] Signal_name is Data Book Name
- All [Pin]s with Model_name POWER or GND that have the same Signal_name (Data Book Name) are connected.

[Buffer Rail Mapping] Example

```
[Buffer Rail Mapping] pulldown_ref pullup_ref gnd_clamp_ref power_clamp_ref ext_ref
|
1          VSS1      VCC1      | Signal pins and their associated
2          VSS2      VCC2      | ground, power and external
|                               | reference connections
3          VSS1      VCC1        VSSCLAMP      VCCCLAMP
4          VSS2      VCC2        VSSCLAMP      VCCCLAMP
5          VSS2      VCC2        NC            VCCCLAMP     V_EXTREF1
6          VSS2      VCC2        NC            VCCCLAMP
7          VSS2      VCC2        NC            VCCCLAMP     V_EXTREF2
8          VSSCLAMP  VCCCLAMP  | Note that normal Input, Output and I/O
|                              buffers will need only three columns
|                              Some possible clamping
|                              connections are shown above
|                              for illustration purposes
```

[Pin] list corresponds to the [Buffer Rail Mapping] shown above.

```
[Pin] signal_name model_name R_pin L_pin C_pin
|
1    OUT1        output_buffer1      | Output buffers
2    OUT2        output_buffer2      |
3    IO3         io_buffer1          | Input/output buffers
4    IO4         io_buffer2          |
5    SPECIAL1    ref_buffer1         | Buffers with POWER CLAMP but no
6    SPECIAL2    io_buffer_term1     | GND CLAMP I-V tables; two use
7    SPECIAL3    ref_buffer2         | external reference voltages
8    IN1         input_buffer
11   VSS1        GND
12   VSS1        GND
13   VSS1        GND
21   VSS2        GND
22   VSS2        GND
23   VSS2        GND
31   VCC1        POWER
32   VCC1        POWER
33   VCC1        POWER
41   VCC2        POWER
42   VCC2        POWER
43   VCC2        POWER
51   VSSCLAMP    GND             | Power connections for clamps
52   VCCCLAMP    POWER           |
71   V_EXTREF1   POWER           | External reference voltage pins
72   V_EXTREF2   POWER           |
```

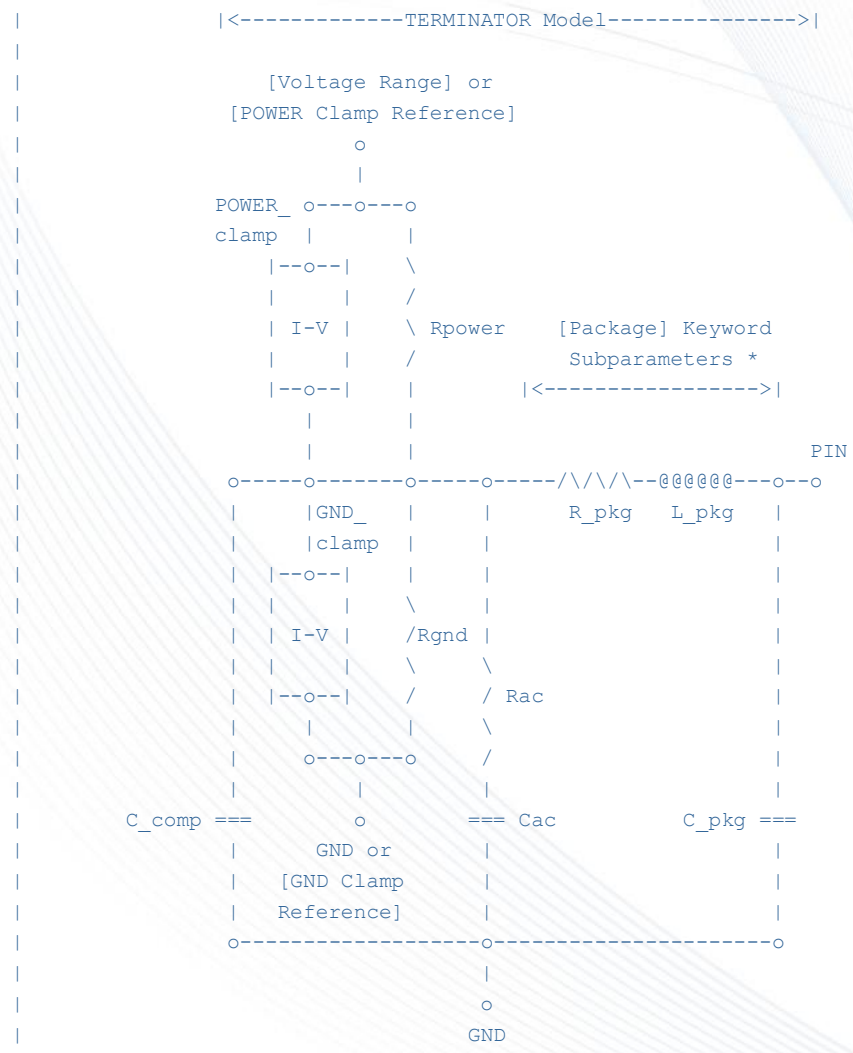
A [Model] Has A “Local Circuit Reference Node”

- A [Model] “Local Circuit Reference Node” is either the A_pdref or A_gcref using [External Model] terminal naming conventions.
- The [Buffer Rail Mapping] section defines the Signal_name (“I/O Buffer Model Reference Signal_name”) that should be connected to a [Model] A_pdref or A_gcref.
- Ground in package and on-die interconnect models for I/O Buffers should be connected to the “I/O Buffer Model Reference Signal_name”

How to Connect RLC Package to Ground

- IBIS is silent on which ground to connect the Capacitor.
- The Capacitor of an I/O Buffer [Pin] Package RLC should be connected to the “I/O Buffer Model Reference Signal_name”

One C_pkg Reference to Ground



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How to Connect “Define Package Model” with “Sections” to Ground

- IBIS is silent on which ground to connect the Capacitor or RLC section.
- The Capacitor of package stub sections of an I/O Buffer [Pin] should be connected to the “I/O Buffer Model Reference Signal_name”
- If the Len of an RLC section of an I/O Buffer [Pin] is not zero, the section can be replace with a transmission line that should be reference to “I/O Buffer Model Reference Signal_name”

How to Connect “Define Package Model” with “Matricies” to Ground

- If all of the Buffer I/O [Pins] in the matrix have the same “I/O Buffer Model Reference Signal_name” then one can use the same rules as for “Define Package Model” with “Sections”.
- If there are off diagonal matrix elements between Buffer I/O [Pins] that have different “I/O Buffer Model Reference Signal_names”, ?????

These Problems go Away with the New Interconnect Modeling

- The package model maker **CAN** make the IBIS-ISS package models with terminals that connect to “I/O Buffer Model Reference Signal_name(s)” that the interconnect within the subckt are required to reference.
- Is this necessary?
  - Should it be required?
  - What error is introduced by using Node 0 in IBIS package and on-die interconnect models?

Are We Gilding the Lilly?

- Simulations results are different by ~10mV transients: C_comp connected to A_pdref vs Node 0
- Certainly any resistors or capacitors to ground in power distribution systems, or pulldown resistors should go to the correct grounds.
- What about referencing signal interconnect w-lines to Node 0, vs the correct ground plane?
  - Can someone demonstrate a difference of any significance?