**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** TBD draft 1

**ISSUE TITLE:** *Electrical Descriptions of Modules*

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**DATE SUBMITTED:** July, 2017

**DATE REVISED:**

**DATE ACCEPTED:**

**STATEMENT OF THE ISSUE:**

There is a need to describe modules that consist of one or more ICs or module mounted on a PCB, MCM or substrate that connects them to a system thru a set of pins. The following BIRD proposes a new type of file called .emd (Electrical Module Description) that addresses this need. This proposal does not encompass an electrical description of connectors and other interconnect devices.

**ANALYSIS PATH/DATA THAT LED TO SPECIFICATION:**

This BIRD has resulted from several years of discussion regarding the need for more flexible description of module interconnects in IBIS. It was decided to avoid a keyword-based approach, in favor of a circuit language approach. IBIS-ISS was developed for this purpose, and a means to instantiate IBIS-ISS models from IBIS became the logical next step.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table : Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| * The model maker must be able to provide interconnect models representing modules, using a combination of IBIS-ISS and Touchstone formats. |  |
| * Touchstone models without an IBIS-ISS wrapper circuit must be supported. |  |
|  |  |
| * An interconnect model may connect one signal name or any combination of signal names on one [Begin Module Description]. | Coupled models are supported. |
| * The buffer I/O, pad, and pin terminals associated with I/O pins must be assignable to interconnect model terminals directly by pin name. |  |
| * The buffer supply, pad, and pin terminals associated with POWER and GND rail pins must be assignable to interconnect model terminals directly by pin name, or indirectly by [Pin] signal\_name. |  |
| * The model maker must be able to provide alternative interconnect models for any given set of pins. | For example for a given pin pair it must be possible to provide both coupled and uncoupled models, high and low bandwidth models, or both IBIS-ISS and Touchstone models. |
|  |  |
| * The model user must be able, given a pin or set of pins it must analyze, to locate all interconnect models that include the pin(s), if any. | Simulation netlisting begins with a list of pins that must be simulated. |
| * The model user must be able to determine all of the pins that a given interconnect model includes. | Once a model is chosen, it may add more pins to the simulation. |
| * The model user must be able to determine how to terminate any terminals of an interconnect model not necessary for a particular analysis. | May need to handle s-parameter and circuit models differently. |
|  |  |
| * The model user must have useful information needed to make the choice between alternative interconnect models that differ only in characteristics other than the model format and the set of pins included. | For example: coupled/uncoupled, low/high bandwidth. This will be used to choose which alternative model set to use. |
|  |  |
|  |  |
| * The model user must be informed which pins of an interconnect model have been modeled with coupling to other pins, sufficient for the former to represent the victim pins and the latter all of the aggressor pins in a crosstalk simulation. | Pins near one “end” of the model will be coupled to pins on one side but probably not enough pins on the other side. |

**BACKGROUND INFORMATION/HISTORY:**

STATEMENT OF THE RESOLVED SPECIFICATIONS: The following text is placed in the specification after the .pkg file description and before the

[End] keyword description.

**<# TBD> ELECTRICAL MODULE DESCRIPTION**

**INTRODUCTION**

A “module” is the generic term to be used to describe a printed circuit board (PCB), Multi Chip Module (MCM) or substrate which can contain components or even other boards or modules, and which can connect to another board or module through a set of user visible pins. The electrical connectivity of such a board or module level component is referred to as an “Electrical Module Description”. For the perposes of the rest of this section, module shall mean PCB, MCM, or substrate

For example, a SIMM module is a module level component that is used to attach several DRAM components on the PCB to another module through edge connector pins. An electrical module description file (a .emd file) is defined to describe the connections of a module level component between the module pins and its components on the module.

What is, and is not, included in an Electrical Module Description is defined by its boundaries. For the definition of the boundaries, see the Description section under the [Interconnect Model] Keyword.

Usage Rules:

A .emd file is intended to be a stand-alone file, not referenced by or included in any .ibs or .pkg file. Electrical Module Descriptions are stored in a file whose name looks like <filename>.emd, where <filename> must conform to the naming rules given in Section 3 of this specification. The .emd extension is mandatory.

Contents:

A .emd file is structured similar to a standard .ibs file. It must contain the following keywords, as defined in IBIS: [IBIS Ver], [File Name], [File Rev], and [End]. It may also contain the following optional keywords: [Comment Char], [Date], [Source], [Notes], [Disclaimer], and [Copyright]. The actual module description is contained between the keywords [Begin Module Description] and [End Module Description], and includes the keywords listed below:

[Begin Module Description]

[Manufacturer]

[Description]

[Number Of Pins]

[Pin List]

[Interconnect Model Set Selector]

[END Interconnect Model Set Selector]

[Interconnect Model Set]

[End Interconnect Model Set]

[Interconnect Model]

[End Interconnect Model]

[Reference Designator Map]

[End Module Description]

More than one [Begin Module Description]/[End Module Description] keyword pair is allowed in a .emd file.

**KEYWORD DEFINITIONS**

*Keyword:* [Begin Module Description]

*Required:* Yes

*Description:* Marks the beginning of an Electrical Module Description.

*Usage Rules:* The keyword is followed by the name of the module level component. If the .emd file contains more than one [Begin Module Description] keyword, then each name must be unique. The length of the component name must not exceed 40 characters in length, and blank characters are allowed. For every [Begin Module Description] keyword there must be a matching [End Module Description] keyword.

*Example:*

[Begin Module Description] 16Meg X 8 SIMM Module

*Keyword:* [Manufacturer]

*Required:* Yes

*Description:* Declares the manufacturer of the components(s) that use this .emd file.

*Usage Rules:* Following the keyword is the manufacturer’s name. It must not exceed 40 characters, and can include blank characters. Each manufacturer must use a consistent name in all .emd files.

*Example:*

[Manufacturer] Quality SIMM Corp.

*Keyword:* [Number Of Pins]

*Required:* Yes

*Description:* Tells the parser the number of pins to expect. Pins are any externally accessible electrical connection to the component.

*Usage Rules:* The field must be a positive decimal integer. Note: The EDA tool must not limit the Number Of Pins to any value less than 1,000. The [Number Of Pins] keyword must be positioned before the [Pin List] keyword.

*Example:*

[Number Of Pins] 128

*Keyword:* [Pin List]

*Required:* Yes

*Description:* Tells the parser the pin names of the user accessible pins. It also informs the parser which pins are connected to power and ground.

*Sub-Params:* signal\_name

*Usage Rules:* Following the [Pin List] keyword are two columns. The first column lists the pin name while the second lists the data book name of the signal connected to that pin. There must be as many pin\_name/signal\_name rows as there are pins given by the preceding [Number Of Pins] keyword. Pin names must be the alphanumeric external pin names of the part. The pin names cannot exceed eight characters in length. Any pin associated with a signal name that begins with “GND” or “POWER” will be interpreted as connecting to the modules ground or power plane. In addition, NC is a legal signal name and indicates that the Pin is a “no connect”. As per the IBIS standard “GND,” “POWER,” and “NC” are case insensitive.

*Example:*

| A SIMM Module Example:

|

[Pin List] signal\_name

A1 GND

A2 data1

A3 data2

A4 POWER5 | This pin connects to 5 V

A5 NC | a no connect pin

| .

| .

A22 POWER3.3 | This pin connects to 3.3 V

B1 casa

| .

| .

|etc.

*Keyword:* [Interconnect Model Set Selector]

*Required:* No

*Description:* Used to list by name the [Interconnect Model Set] keywords available for the [Begin Module Description].

*Usage Rules:* Interconnect Model Sets contain Interconnect Models used to describe pin connections to IBIS-ISS subcircuits or Touchstone files.

A [Begin Module Description] may have one, or more than one [Interconnect Model Set] keywords (identified by a name) associated with it. All Interconnect Model Sets exist for the component shall be listed in this section. An Interconnect Model Set Selector is required even if there is only one Interconnect Model Set. If there are no Interconnect Model Sets, the [Interconnect Model Set Selector] keyword is illegal. The [Interconnect Model Set Selector] is hierarchically within the scope of the [Begin Module Description] keyword.

The section under the [Interconnect Model Set Selector] keyword shall have two entries per line, with each line identifying one Interconnect Model Set associated with the component. The entries shall be separated by at least one white space. The first entry lists the Interconnect Model Set name (up to 40 characters long). The second entry is the file reference of the file containing the Interconnect Model Set and shall have the extension “ims”. This file reference shall conform to the rules given in Section 3, ‘GENERAL SYNTAX RULES AND GUIDELINES’. If the Interconnect Model Set is in the same IBIS file as [Begin Module Description], then the second entry shall be “NA”.

The files containing the Interconnect Model Sets with the ibs extension shall be located in the same directory as the .ibs file or in a specified directory under the .ibs file as determined by the directory path according to the file name rules given in Section 3, ’GENERAL SYNTAX RULES AND GUIDELINES’ (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs file is permitted). An [Interconnect Model Set] with matching name shall be found in the stated location for each Interconnect Model Set named in the [Interconnect Model Set Selector].

Each Interconnect Model Set name may only appear once under the [Interconnect Model Set Selector] keyword for a given component.

*Example:*

[Interconnect Model Set Selector]

| Interconnect Model Set file\_reference

All\_pins\_iss NA | An [Interconnect Model Set] is

| present in the .ibs file

All\_pins\_touchstone 8\_pin\_s16p.ims | The [Interconnect Model Set] is

| stored in a separate .ims file

[End Interconnect Model Set Selector]

*Keyword:* [**End Interconnect Model Set Selector**]

*Required:* Yes, for each instance of the [Interconnect Model Set Selector] keyword

*Description:* Indicates the end of the data for one [Interconnect Model Set Selector].

*Example:*

[End Interconnect Model Set Selector]

**12.2 GENERAL INTERCONNECT SYNTAX REQUIREMENTS**

Terminal lines under the [Interconnect Model] keyword describe connections.

Pin\_name in this context are either the pin\_name in the [Pin List], or reference\_designator.pin for ins that are pins of a component in [Reference Designator Map]

I/O terminals shall be connected using only the pin\_name qualifier:

Rail terminal connections have more options to support direct connections to terminals or to groups of terminals using signal\_name, or pin\_name. The rail terminal can connect to:

* a specific rail pin\_name
* all of the pins of a rail signal\_name within a component
* all of the pins of a rail signal\_name

One or more Interconnect Model Sets may be included in a separate Interconnect Model Set file, using a file name with the extension “ims”, or within the .emd file where [Interconnect Model Set Selector] is used. The [Interconnect Model Set] keyword can contain the optional [Manufacturer] and [Description] keywords and one or more [Interconnect Model] keywords and the [Interconnect Model] associated subparameters, as is listed in Table 40.

Table 40 – Interconnect Modeling Keywords and Subparameters

| **Keyword or Subparameter** | **Notes** |
| --- | --- |
| [Interconnect Model Set] |  |
| [Manufacturer] | (note 1) |
| [Description] | (note 1) |
| [Interconnect Model] | (note 2) |
| Param |  |
| File\_TS | (note 3) |
| File\_IBIS-ISS | (note 3) |
| Unused\_port\_termination | (note 4) |
| Number\_of\_terminals | (note 5) |
| <terminal line> | (note 6) |
| [End Interconnect Model] | (note 7) |
| [End Interconnect Model Set] | (note 8) |
| Note 1 [Manufacturer] and [Description] are each optional keywords within any [Interconnect Model Set].  Note 2 At least one [Interconnect Model] is required for each [Interconnect Model Set].  Note 3 One of either the File\_TS or File\_IBIS-ISS subparameters is required.  Note 4 This subparameter shall be followed by the “=” character and a numeric value (integers and reals are acceptable), with both optionally surrounded by whitespace.  Note 5 This subparameter shall be followed by the “=” character and an integer value, with both optionally surrounded by whitespace.  Note 6 See text below.  Note 7 Required when the [Interconnect Model] keyword is used  Note 8 Required when the [Interconnect Model Set] keyword is used | |

When Interconnect Model Set definitions occur within a .ibs file, their scope is “local”— they are known only within that .ibs file and no other .ibs file.

Usage Rules for the .ims file:

Interconnect models are stored in a file whose file name uses the format:

<stem>.ims

The <stem> provided shall adhere to the rules given for the [File Name] keyword. Use the “ims” extension to identify files containing Interconnect Models. The .ims file shall contain the [IBIS Ver], [File Name], [File Rev], and the [End] keywords. Optional elements include the [Date], [Source], [Notes], [Disclaimer], [Copyright], and [Comment Char] keywords. All of these keywords and associated subparameters follow the same rules as those for a normal .ibs file.

Note that the [Begin Module Description] and [Model] keywords are not allowed in the .ims file. The .ims file is for Interconnect Models only.

*Keyword:* [Interconnect Model Set]

*Required:* No

*Description:* Used to contain Interconnect Models

*Usage Rules:* [Interconnect Model Set] has a single argument, which is the name of the Interconnect Model Set. The length of the Interconnect Model Set name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model Set]/[End Interconnect Model Set] keyword pair is hierarchically equivalent in scope to [Begin Module Description] and [Model].

The section under the [Interconnect Model Set] keyword may contain a [Manufacturer] keyword section and [Description] keyword section and shall contain one or more Interconnect Models. See the section [Interconnect Model] for a description of the content of each Interconnect Model.

Model makers are recommended to ensure that each Interconnect Model Set contains a complete description, through Interconnect Models, needed for the path connecting the pins of the module to the pins of the modules (reference dsignator) that are in the [Reference Designator Map].

*Example:*

[Interconnect Model Set] Signal\_Integrity

[Manufacturer] Acme Packaging, Inc.

[Description] This set contains one model for each I/O pin

[Interconnect Model] DQ1

…

[End Interconnect Model]

[Interconnect Model] DQ2

…

[End Interconnect Model]

[Interconnect Model] DQS

…

[End Interconnect Model]

[End Interconnect Model Set]

*Keyword:* [Manufacturer]

*Required:* No

*Description:* Specifies the name of the [Interconnect Model Set] manufacturer.

*Usage Rules:* The length of the manufacturer’s name shall not exceed 40 characters (blank characters are allowed, e.g., Oklahoma Instruments).

*Example:*

[Manufacturer] NoName Corp.

*Keyword:* [Description]

*Required:* No

*Description:* Provides a concise yet easily human-readable description of what kind of interconnect the [Interconnect Model Set] represents.

*Usage Rules:* The description shall be less than 60 characters in length, shall fit on a single line, and may contain spaces.

*Example:*

[Description] 220-Pin Quad Ceramic Flat Pack

*Keyword:* [**End Interconnect Model Set**]

*Required:* Yes, for each instance of the [Interconnect Model Set] keyword.

*Descriptiofn:* Indicates the end of the Interconnect Model Set data.

*Example:*

[End Interconnect Model Set]

*Keyword:* [Interconnect Model]

*Required:* No

*Description:* Marks the beginning of an Interconnect Model description that is used to define the interfaces to IBIS-ISS subcircuit or Touchstone files.

*Sub-Params:* Unused\_port\_termination, Param, File\_TS, File\_IBIS-ISS, Number\_of\_terminals

*Usage Rules:* [Interconnect Model] has a single argument, which is the name of the associated Interconnect Model. The length of the Interconnect Model name shall not exceed 40 characters in length. Blank characters are not allowed. The [Interconnect Model]/[End Interconnect Model] keyword pair is hierarchically scoped by the [Interconnect Model Set]/[End Interconnect Model Set] keywords.

The [Interconnect Model]/[End Interconnect Model] section defines both the association between a Touchstone file or IBIS-ISS subcircuit and an Interconnect Model, as well as defining the terminals and terminal usage for the Interconnect Model in the context of the given [Begin Module Description].

Each terminal of an Interconnect Model passes current to the simulation node it is connected to and has a “voltage”. This, as stated, is imprecise. Voltage, by definition, is a potential difference between two points. It is common to probe and plot the potential difference between simulator nodes at a terminal and the simulator ideal Node 0. This is valid for non-power aware simulations when the local ground (or return path) node is forced to Node 0 by the simulator, or for “ground referenced” power aware simulations that lump the effect of the ground interconnect into the power rails. However, this is not valid when the voltages of the ground nodes are “floating”. In this case it is important that the actual rail node that is the reference node for measurements at the I/O pin is included as a terminal in the Interconnect Model. If this is not done, then the Interconnect Model will not correctly account for all return currents, particularly from capacitive elements. If an Interconnect Model does not contain a reference terminal, then the user of these models should be aware that using these models in non-ground referenced power aware simulations will introduce potential errors in simulations.

The following subparameters are defined:

Unused\_port\_termination = <value>

Param

File\_IBIS-ISS

File\_TS

Number\_of\_terminals = <value>

In addition to these subparameters, the [Interconnect Model]/[End Interconnect Model] section may contain lines describing terminals and their connections. No specific subparameter name, token, or other string is used to identify terminal lines.

Unless noted below, no Interconnect Model subparameter requires the presence of any other subparameter.

Unused\_port\_termination rules:

This optional subparameter defines the termination that is to be applied by the EDA tool during simulation to the terminals of any IBIS-ISS subcircuit or Touchstone network that is not being used in the [Interconnect Model]/[End Interconnect Model] group. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace.

If this subparameter is present, the EDA tool should connect the unused terminals to GND through a resistorwith the value of resistance in ohms provided in the argument.

If this parameter is not defined, the EDA tool may connect terminals to terminations as needed to prevent numerical instability in simulation (EDA tools are recommended to alert users when this occurs and document the termination value used). Note that the terminals remain technically open, and terminations connected by the EDA tool are intended to approximate open-circuit conditions.

Only one Unused\_port\_termination subparameter may appear for a given [Interconnect Model] keyword.

Param rules:

The subparameter Param is optional and only legal with the File\_IBIS-ISS subparameter documented below. Param is illegal with the File\_TS subparameter documented below. Param shall be followed by three arguments: an unquoted string argument giving the name of the parameter to be passed into the IBIS-ISS subcircuit, a reserved word for the parameter format, and one numerical value or one string value (surrounded by double quotes) for the parameter value to be passed into the IBIS-ISS subcircuit.

The numerical value rules follow the scaling conventions in Section 3.2, “SYNTAX RULES”. The EDA tool is responsible for translating IBIS specified parameters into IBIS-ISS parameters. For example, 1 megaohm, would be represented as 1M in Param value according to the Section 3 rules, but would be converted by the EDA tool to case-insensitive 1meg (1X is not recommended) or 1E6 for IBIS-ISS use. Quoted string parameters in IBIS are converted to the string parameter syntax in IBIS-ISS subcircuits. For example, the Param value "typ.s2p" would be converted to str('typ.s2p') in IBIS-ISS subcircuits.

*Examples:*

| Param name format value

Param abc Value 2m | 2E-3 in IBIS

Param def Value 4k | 4E3 in IBIS

Param ts\_file Value "typ.s2p" | file name string passed

| into IBIS-ISS

File\_IBIS-ISS rules:

Either File\_IBIS-ISS or File\_TS is required for a [Interconnect Model]/[End Interconnect Model] group*.* The File\_IBIS-ISS subparameter is followed by two unquoted string arguments consisting of the file\_reference and circuit\_name (.subckt name) for an IBIS-ISS file. The IBIS-ISS file under file\_reference shall be located in the same directory as the referencing .ibs file or .ims file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs or .ims file is permitted).

*Example:*

| file\_type file\_reference circuit\_name(.subckt name)

File\_IBIS-ISS net.iss netlist\_typ

File\_TS rules:

Either File\_TS or File\_IBIS-ISS is required for a [Interconnect Model]/[End Interconnect Model] group.File\_TS is followed by one unquoted string argument, which is the file reference for a Touchstone file. The Touchstone file under file\_reference shall be located in the same directory as the referencing .ibs file or .ims file or in a specified directory under the referencing file as determined by the directory path (i.e., a file reference containing a relative path to a directory below that of the referencing .ibs or .ims file is permitted).

*Example:*

| file\_type file\_reference

File\_TS typ.s8p

Number\_of\_terminals rules:

The Number\_of\_terminals subparameter is required and defines the number of terminals associated with the Interconnect Model. The subparameter name shall be followed by a single integer argument greater than zero on the same line. The argument shall be separated from the subparameter name by the “=” character. The subparameter name, “=” character, and argument may optionally be separated by whitespace. Only one Number\_of\_terminals subparameter may appear for a given [Interconnect Model] keyword. The Number\_of\_terminals subparameter shall appear before any terminal lines and after all other subparameters for a given Interconnect Model.

Terminal line rules:

Terminal lines shall appear after the Number\_of\_terminals subparameter and before the [End Interconnect Model] keyword. No token or reserved word identifies terminal lines.

Each terminal line contains information on a terminal of an IBIS-ISS subcircuit (or Touchstone file).

Terminal lines are of the following form, with each identifier separated by whitespace:

<Terminal\_number> <Terminal\_type> <Terminal\_type\_qualifier> <Qualifier\_entry> [Aggressor\_Only]

Terminal\_number

Terminal\_number is an identifier for a specific terminal. Terminal\_number shall be a positive non-zero integer less than or equal to the value of the Number\_of\_terminals argument. This value will also match the number of terminals used in an associated IBIS-ISS subcircuit, or the number of ports plus 1 (N+1) used in a corresponding associated Touchstone file. The same Terminal\_number shall not appear more than once for a given Interconnect Model. If any terminals are not present for a given Interconnect Model, then those terminals are unused, and shall be terminated according to the Unused\_port\_termination rules.

The Terminal\_number entry shall match the IBIS-ISS terminal (node) position or the Touchstone file terminal (line) position, plus an undeclared reference line. The Terminal\_number entries may be listed in any order as long as there are no duplicate entries.

Terminal\_type  
Terminal\_type is a string that identifies whether the terminal is a supply or I/O pin. Terminal\_type identifies to which specific pin rail the terminal is connected. Terminal\_type shall be one of the following:

* Pin\_I/O
* Pin\_Rail

Terminal\_type\_qualifier   
Terminal\_type\_qualifier is a string that identifies the association between a terminal and a specific pin\_name, signal\_name or component\_signal\_name

Qualifier\_entry   
The <Qualifier\_entry>, shown in angle brackets, is the name required for the following Terminal\_type\_qualifiers:

pin\_name <pin\_name\_entry>

signal\_name <signal\_name\_entry>

component\_signal\_name <reference\_designator.signal\_name\_entry>

Note that to short all rail pins in [Pin List] with the same signal\_name the reference\_designator shall be bland and the component\_signal\_name will be <.signal\_name\_entry>

Aggressor\_OnlyMulti-line models may describe only a subset of a coupled structure (e.g., a 64-line bus may be described by a four-line model). As a result, while the interconnects at the edges of the model may induce crosstalk onto other interconnects nearby, nearby, being on the edge of the model, they may not themselves experience the full crosstalk impact that the corresponding interconnect experiences in the real, full structure. The optional Aggressor\_Only column entry is allowed on all terminal locations for I/O terminals to indicate such incomplete coupling. Terminals that include the Aggressor\_Only entry may not be suitable to be simulated as victims, as they do not experience the full coupling present in the real physical structure. If an I/O terminal is not identified as Aggressor\_Only, then the interconnect to that I/O terminal includes coupling to all interconnections deemed necessary for coupled signal analysis. If a particular terminal is identified as Aggressor\_Only, then the entire path of the associated pin\_name is to be considered Aggressor\_Only.

Touchstone Files

For an Interconnect Model using File\_TS with N ports, N equals the number of ports present in the data of the associated Touchstone 1.x file, or the value associated with the [Number of Ports] keyword in the associated Touchstone 2 file. The Number\_of\_terminals entry in the Interconnect Model shall be an integer equal to N+1. Terminal rules are described below:

* The EDA tool shall use the pin\_name or signal\_name specified for the associated terminal “N+1” entry as the reference node for each of the N ports. For an Interconnect Model with N ports, the terminals and ports are associated as follows:
  + Terminal              Port
  + 1                              1
  + 2                              2
  + …
  + N                             N
  + N+1 reference
* Terminal N+1 shall be either directly connected to a pin with a signal\_name of POWER or GND.

Terminal lines describe the IBIS-ISS node or Touchstone port that each terminal should be connected to. The arrangement of the terminal line entries (columns) is described below.

* The first column, Terminal\_number, contains an integer between 1 and the Number\_of\_terminals that describes the ordinal (positional) number of the IBIS-ISS node in the [Interconnect Model] subcircuit or Touchstone file port. The second column is Terminal\_type, the third column is Terminal\_type\_qualifier, the fourth column is Qualifier\_entry and there is an optional fifth column “Aggressor\_Only”
* The second column, Terminal\_type is:
  + For I/O connections
    - Terminal\_type must be Pin\_I/O.
    - Terminal\_type\_qualifier shall be pin\_name.
    - Qualifier\_entry shall be the pin\_name of an I/O pin.
  + For rail connections
    - Terminal\_type shall be Pin\_Rail
    - Terminal\_type\_qualifier shall be one of the following
      * pin\_name
        + Qualifier\_entry shall be a rail pin\_name
      * signal\_name
        + Qualifier\_entry shall be a rail signal\_name
      * component\_signal\_name
        + Qualifier\_entry shall be a rail reference\_designator.signal\_name

Table 41 summarizes the rules described above.

Table 41 – Allowed Terminal\_type Associations1

| **Terminal\_type** | **Terminal\_type\_qualifier** | | | | **Aggressor\_Only** |
| --- | --- | --- | --- | --- | --- |
| **pin\_name** | **signal\_name** | **component\_signal\_name** |  |
| Pin\_I/O | X |  |  |  | A |
| Pin\_Rail | Y | Y | Z |  |  |

Notes

1. In the table, “X” refers to I/O pin names. “Y” are POWER and GND names. The letter “A” designates "Aggressor\_Only". The letter Z designates Reference Designator and POWER and GND names.

Three classes of pins are defined for a component: signal pins, supply pins and no-connect pins. Supply pins have a model\_name of either POWER or GND. No-connect pins have model\_name NC. All other pins are classified as signal pins. Pins are assumed to use the names listed under the first column of the [Pin List] keyword (the pin\_name column).

Pins may be terminals of the Interconnect Model that connect directly to a printed circuit board or other type of system connection to an IBIS component. Pins can be signal pins (Pin\_I/O), or supply pins (Pin\_Rail). An Interconnect Model can connect supply pins in one of two ways:

1. By specifying terminals for some or all of the supply pins.
2. By assuming that all supply pins connected to a supply signal\_name are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all pins that are connected to a specific signal\_name on at least one supply pin.
3. By assuming that all supply pins connected to a supply signal\_name on a specific component are shorted together. This is done by specifying a unique terminal (of Terminal\_type Pin\_Rail) for all pins on a component that are connected to a specific signal\_name on at least one supply pin.

Any one pin shall not be included in more than one terminal of an Interconnect Model.

*Keyword:* [Reference Designator Map]

*Required:* Yes, if any of the path descriptions use the Node subparameter

*Description:* Maps a reference designator to a component or electrical Module description contained in a .ibs or .emd file.

*Usage Rules:* The [Reference Designator Map] keyword must be followed by a list of all of the reference designators called out by the Node subparameters used in the various path descriptions. Each reference designator is followed by the name of the .ibs or .emd file containing the electrical description of the component or Module, then the name of the component itself as given by the .ibs or .emd file’s [Begin Module Description] or [Begin Module Description] keyword respectively. The reference designator, file name and component name terms are separated by white space. By default the .ibs or .emd files are assumed to exist in the same directory as the calling .emd file. It is legal for a reference designator to point to a component that is contained in the calling .emd file.

The reference designator is limited to ten characters.

*Example:*

[Reference Designator Map]

|

| External Part References:

|

| Ref Des File name Component name

u23 pp100.ibs Processor

u24 simm.emd 16Meg X 36 SIMM Module

u25 ls244.ibs NoName 74LS244a

u26 r10K.ibs My\_10K\_Pullup

*Keyword:* [End Module Description]

*Required:* Yes

*Description:* Marks the end of an Electrical Interconnect Description.

*Usage Rules:* This keyword must come at the end of each complete electrical interconnect model description.

Optionally, a comment may be added after the [End Electrical Description] keyword to clarify which Module model has ended.

*Example:*

[End Module Description] | End: 16Meg X 8 SIMM Module

Keyword: [End]

*Required:* Yes

*Description:* Defines the end of the emd file.

*Example:*

[End]