BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)

(See instructions starting on template page two)

BIRD NUMBER: BIRD_Figure29_draft1
ISSUE TITLE: Figure 29 corrections
REQUESTOR: Arpad Muranyi, Mentor Graphics, A Siemens Business

DATE SUBMITTED: TBD
DATE REVISED: TBD
DATE ACCEPTED: TBD

DEFINITION OF THE ISSUE:

Figure 29 and related examples in the IBIS v6.1 specification talk about “explicit pad connections” but there is also a note on pg. 131 which states that these types of connections are not supported by the specification:

> NOTE REGARDING THIS EXAMPLE:
> The pad_* to pin connections in Figure 29 and in the example lines with the comment, "explicit pad connection", are shown for reference. The connection syntax has not yet been defined. Therefore, the connections for pad_* to pin are not supported in this specification.

Since BIRD189 defines a new syntax for connecting package models between pins and pads, and/or connecting on-die interconnect models between pads and buffer terminals, this statement will no longer be true after BIRD189 becomes part of the IBIS specification.

In addition, Figure 29 shows examples for joins and splits in the package model which are not supported in IBIS v6.1 and will not be supported by BIRD189 either. These unsupported concepts need to be removed from the figure and corresponding examples.

For this reason, figure 29, the related text and examples need to be updated as described in this BIRD.

SOLUTION REQUIREMENTS:

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

Requirement	Notes
1. Remove any forward references to potential future package modeling syntax not supported by the specification	

2. Change figure 29 to be consistent with #1	
3. Chage the examples to be consistent with #1	
4. Make sure that Figure 29, the related text and examples are consistent with BIRD189	

(Enumerate each requirement in the table above, adding rows as needed.)

SUMMARY OF PROPOSED CHANGES:

For review purposes, the proposed changes are summarized as follows:

Table 2: IBIS Keywords, Subparameters, AMI Reserved_Parameters, and AMI functions Affected

Specification Item	New/Modified/Other	Notes

(List each affected specification item in the table above, adding rows as needed.)

PROPOSED CHANGES:

Note that while [Package], [Package Model] and R_pin, L_pin, C_pin under the [Pin] keyword may coexist with [Interconnect Model Group] in the same [Component], BIRD189 prohibits the use of [External Circuit] and [Node Declarations] (consequently [Circuit Call]) together with [Interconnect Model Group]. For that reason this BIRD does not need to mention anything about BIRD189, because this BIRD only contains syntax that is related to [Node Declarations] and [Circuit Call] (and a very small editorial change in the [Merged Pins] section). The changes described below will make the [Circuit Call] syntax compatible with BIRD189 without mentioning it.

On pg. 129/130, change the example from:

```
[Node Declarations]          | Must appear before any [Circuit Call] keyword
|
| Die nodes:
a b c d e                    | List of die nodes
f g h nd1
|
| Die pads:
pad_2a pad_2b pad_4 pad_11   | List of die pads
|
[End Node Declarations]
```

To:

```
[Node Declarations]          | Must appear before any [Circuit Call] keyword
|
| Die nodes:
a b c d e                    | List of die nodes
f g h nd1
|
[End Node Declarations]
```

On pg. 131, change:

Every occurrence of the Port_map subparameter must begin on a new line and must be followed by two arguments, the first being a port name, and the second being a die node, die pad, or a pin name.

To:

Every occurrence of the Port_map subparameter must begin on a new line and must be followed by two arguments, the first being a port name, and the second being a die node or a pin name.

On pg. 131, change:

“Please note that a pin name in the second argument does not mean that the connection is made directly to the pin. Since native IBIS does not have a mechanism to declare die pads explicitly, connections to die pads are made through their corresponding pin names (listed under the [Pin] keyword). This convention must only be used with native IBIS package models where a one-to-one path between the die pads and pins is assumed. When a package model other than native IBIS is used with a [Component], the second argument of Port_map must have a die pad or die node name. These names are matched to the corresponding port name of the non-native package model by name (not by position). In this case, the package model may have an arbitrary circuit topology between the die pads and the pins. A one-to-one mapping is not required.”

To:

“Please note that a pin name in the second argument does not mean that the connection is made directly to the pin. Since IBIS assumes a one-to-one path between the die pads and pins (i.e. each pin has one and only one corresponding die pad, and each die pad has one and only one corresponding pin), it does not have a mechanism to declare die pads. Consequently, when the second argument of Port_map contains a pin name, the connection is made to the die pad that is associated with that pin name.”

On pg. 131, delete the following text:

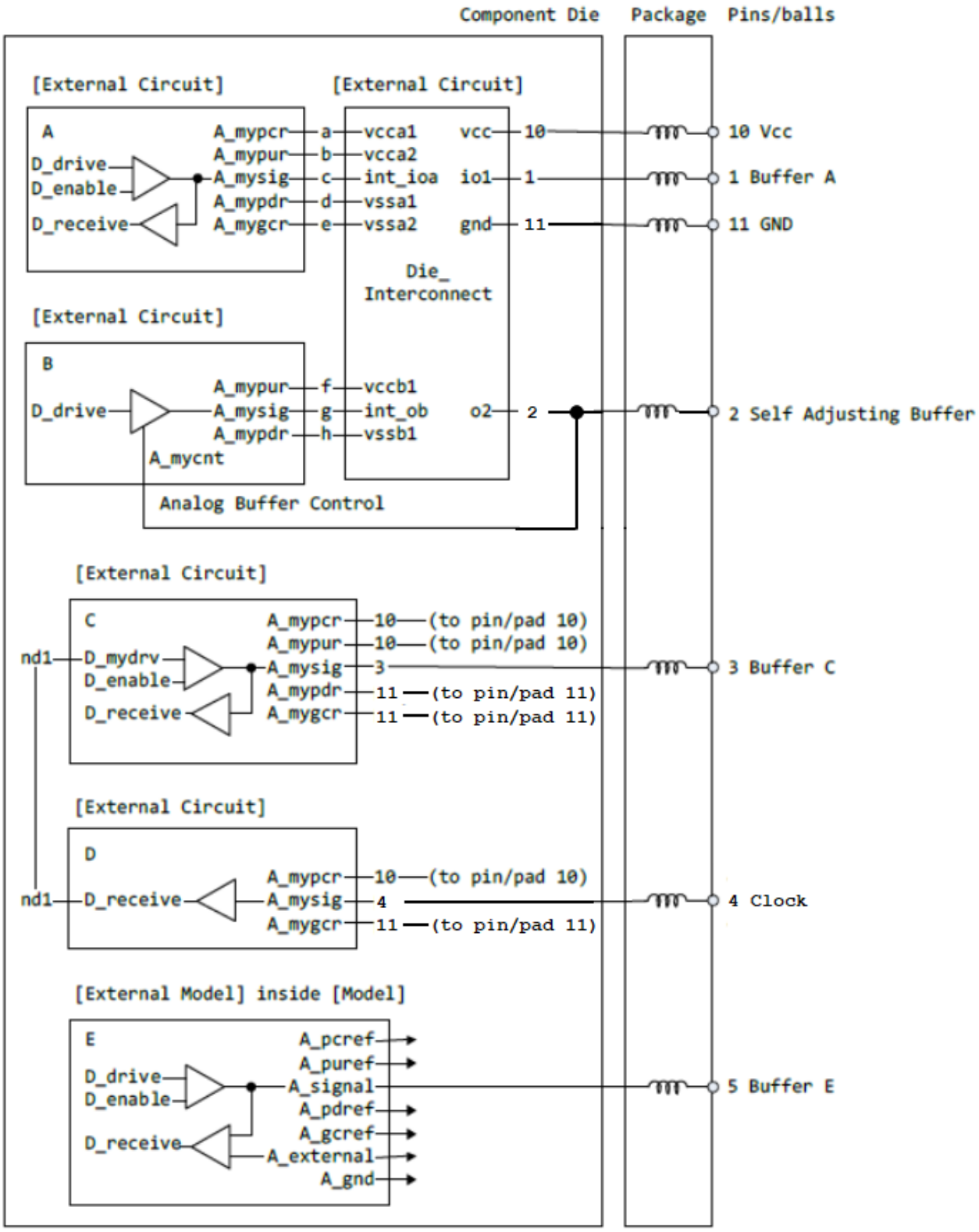
“The pad_* to pin connections in Figure 29 and in the example lines with the comment, "explicit pad connection", are shown for reference. The connection syntax has not yet been defined. Therefore, the connections for pad_* to pin are not supported in this specification.”

Page 132, Figure 29:

All “explicit pads” and joins/forks in the package model should be removed from the drawing as follows:

- change “pad_11” to “11”
- change “pad_2a” to “2”
- remove inductor between pin 2 and pad_2b
- remove “pad_2b”
- draw the “Analog Buffer Control” line to pad 2
- at [External Circuit] C change both “pad_11” to “11” (the same way as “10”)
- at [External Circuit] D change “pad_4” to “4” and “pad_11” to “11” (like “10”)
- rename pin “4a Clocka” to “4 Clock”
- remove pin “4b Clockb” and associated inductor in package model box
- remove Note 2 below the figure

After making these changes, the figure should look as follows:



Note:
The ports of the [External Model] E are automatically connected by the tool, taking the [Pin Mapping] keyword into consideration, if exists.

Pages 133-134, change the [Circuit Call] examples from:

```
[Circuit Call] A                | Instantiates [External Circuit] named "A"
|
Signal_pin 1
|
| mapping  port          pad/node
|
Port_map   A_mypcr       a        | Port to internal node connection
Port_map   A_mypur       b        | Port to internal node connection
Port_map   A_mysig       c        | Port to internal node connection
Port_map   A_mypdr       d        | Port to internal node connection
Port_map   A_mygcr       e        | Port to internal node connection
|
[End Circuit Call]
|
|
[Circuit Call] B                | Instantiates [External Circuit] named "B"
|
Signal_pin 2
|
| mapping  port          pad/node
|
Port_map   A_mypur       f        | Port to internal node connection
Port_map   A_mysig       g        | Port to internal node connection
Port_map   A_mypdr       h        | Port to internal node connection
Port_map   A_mycnt       pad_2b   | Port to explicit pad connection
|
[End Circuit Call]
|
|
[Circuit Call] C                | Instantiates [External Circuit] named "C"
|
Signal_pin 3
|
| mapping  port          pad/node
|
Port_map   A_mypcr       10       | Port to implicit pad connection
Port_map   A_mypur       10       | Port to implicit pad connection
Port_map   A_mysig       3        | Port to implicit pad connection
Port_map   A_mypdr       pad_11   | Port to explicit pad connection
Port_map   A_mygcr       pad_11   | Port to explicit pad connection
Port_map   D_mydrv       nd1      | Port to internal node connection
|
[End Circuit Call]
|
|
[Circuit Call] D                | Instantiates [External Circuit] named "D"
|
Signal_pin 4a
|
| mapping  port          pad/node
|
Port_map   A_my_pcref    10       | Port to implicit pad connection
```

```
Port_map   A_my_signal   pad_4     | Port to explicit pad connection
Port_map   A_my_gcref    pad_11    | Port to explicit pad connection
Port_map   D_receive     nd1       | Port to internal node connection
|
[End Circuit Call]
|
|
[Circuit Call] Die_Interconnect   | Instantiates [External Circuit] named
|                                   "Die_Interconnect"
|
| mapping  port          pad/node
|
Port_map   vcc           10        | Port to implicit pad connection
Port_map   gnd           pad_11    | Port to explicit pad connection
Port_map   io1           1         | Port to implicit pad connection
Port_map   o2            pad_2a    | Port to explicit pad connection
Port_map   vcca1         a         | Port to internal node connection
Port_map   vcca2         b         | Port to internal node connection
Port_map   int_ioa       c         | Port to internal node connection
Port_map   vssa1         d         | Port to internal node connection
Port_map   vssa2         e         | Port to internal node connection
Port_map   vccb1         f         | Port to internal node connection
Port_map   int_ob        g         | Port to internal node connection
Port_map   vssb1         h         | Port to internal node connection
|
[End Circuit Call]
```

To:

```
[Circuit Call] A                  | Instantiates [External Circuit] named "A"
|
Signal_pin 1
|
| mapping  port          pad/node
|
Port_map   A_mypcr       a         | Port to internal node connection
Port_map   A_mypur       b         | Port to internal node connection
Port_map   A_mysig       c         | Port to internal node connection
Port_map   A_mypdr       d         | Port to internal node connection
Port_map   A_mygcr       e         | Port to internal node connection
|
[End Circuit Call]
|
|
[Circuit Call] B                  | Instantiates [External Circuit] named "B"
|
Signal_pin 2
|
| mapping  port          pad/node
|
Port_map   A_mypur       f         | Port to internal node connection
Port_map   A_mysig       g         | Port to internal node connection
Port_map   A_mypdr       h         | Port to internal node connection
Port_map   A_mycnt       2         | Port to implicit pad connection
|
[End Circuit Call]
```

```
|
|
[Circuit Call] C                | Instantiates [External Circuit] named "C"
|
Signal_pin 3
|
| mapping  port          pad/node
|
Port_map   A_mypcr       10       | Port to implicit pad connection
Port_map   A_mypur       10       | Port to implicit pad connection
Port_map   A_mysig       3        | Port to implicit pad connection
Port_map   A_mypdr       11       | Port to implicit pad connection
Port_map   A_mygcr       11       | Port to implicit pad connection
Port_map   D_mydrv       nd1      | Port to internal node connection
|
[End Circuit Call]
|
|
[Circuit Call] D                | Instantiates [External Circuit] named "D"
|
Signal_pin 4
|
| mapping  port          pad/node
|
Port_map   A_my_pcref    10       | Port to implicit pad connection
Port_map   A_my_signal   4        | Port to implicit pad connection
Port_map   A_my_gcref    11       | Port to implicit pad connection
Port_map   D_receive     nd1      | Port to internal node connection
|
[End Circuit Call]
|
|
[Circuit Call] Die_Interconnect   | Instantiates [External Circuit] named
|                                   "Die_Interconnect"
|
| mapping  port          pad/node
|
Port_map   vcc           10       | Port to implicit pad connection
Port_map   gnd           11       | Port to implicit pad connection
Port_map   io1           1        | Port to implicit pad connection
Port_map   o2            2        | Port to implicit pad connection
Port_map   vcca1         a        | Port to internal node connection
Port_map   vcca2         b        | Port to internal node connection
Port_map   int_ioa       c        | Port to internal node connection
Port_map   vssa1         d        | Port to internal node connection
Port_map   vssa2         e        | Port to internal node connection
Port_map   vccb1         f        | Port to internal node connection
Port_map   int_ob        g        | Port to internal node connection
Port_map   vssb1         h        | Port to internal node connection
|
[End Circuit Call]
```

On pg. 142-143 change:

"Since the [Merged Pins] keyword (defined below) provides a mechanism to explicitly and unambiguously define the connectivity of merged pins with greater detail and freedom, the use of the [Merged Pins] keyword is strongly recommended for new models in which merged pin modeling exists."

To:

"Since the [Merged Pins] keyword (defined below) provides a mechanism to explicitly and unambiguously define the connectivity of merged pins with greater detail and freedom, the use of the [Merged Pins] keyword is strongly recommended for models in which merged pin modeling exists."

BACKGROUND INFORMATION/HISTORY:

(Relevant notes regarding history, discussions, and revisions go here.)