Micron IBIS-AMI Requirements for SE EQ

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IBIS-AMI Capability Requirements

- Must have
  - DC Offset/Common Mode Voltage
  - Clock Forwarding
  - Component Models
  - Vref

DC Offset/Common Mode Voltage

- EDA tool can detect Single-Ended by absence of [Diff Pin] entry
- Standard way of passing CM between Tx and Rx

Clock Forwarding

- External Timing Reference
  - Used as DFE trigger point for Rx GetWave
  - Clock vector in the AMI_GetWave function (‘clock_times’) as an input.
    - AMI model does not write to the vector.
    - EDA tool passes clock ticks to the model.
  - There needs to be a method to generate the clock ticks for every GetWave block.
    - This can be done by performing concurrent channel simulation of the strobe signal.
    - Another method may be to pass synthesized clock signal by imposing the jitter distribution on an ideal clock vector.
    - The clock vector passed in the AMI model would have the same properties of the traditional clock vector (edge timing).
- Reserved Parameter – External_Timing_Ref with values 0/1
  - When External_Timing_Ref = 0 – Model has CDR – behave like serial link
  - When External_Timing_Ref = 1 – Model has External Strobe/Clk Signal – use External Strobe/Clk Signal

Component Models

- Bus definition in .ibs
  - Declare bus and timing references under [Component] below [Diff Pin] sections
  - Used for common timing reference
  - Can define common Vref

```
[Bus Definition]    DQ
VoltageRef          Common
TimingRef           DQS_t / DQS_c
SignalName          DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7
[End Bus Definition]
```

Vref

- Vref
  - Depends on the channel, EDA tool detects Vref and adjusts final waveform at the Rx.
  - AMI models will still see a differential signal.
  - No change to the AMI API is expected in this regard.
  - The component level Vref (Vcent_DQ) is expected to be close to the signal Vref
  - Not passed to the AMI model to keep it simple.
- Could use [Standard] keyword or similar


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