GDDR6X Introduction + IBIS-AMI Simulation Results

IBIS ATM Task Group

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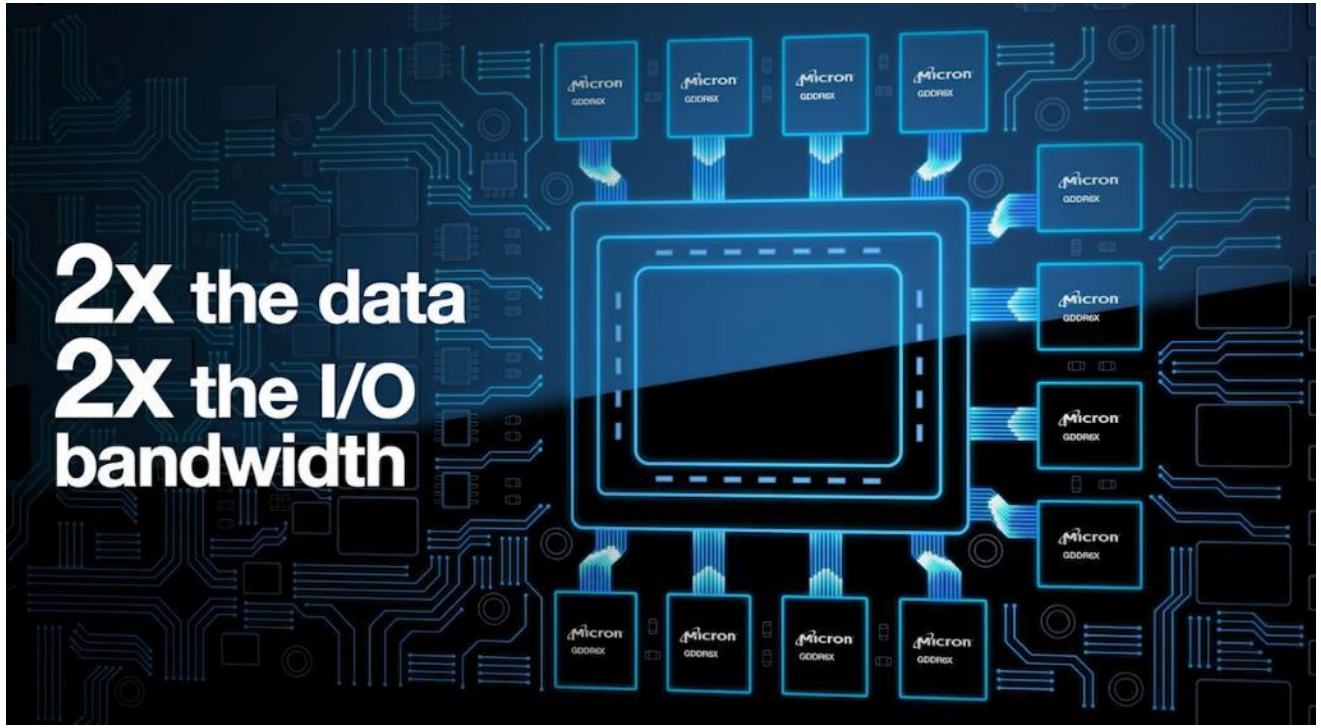
12/1/2020

What's New?

- Micron introduced new Graphics DDR memory – GDDR6X
  - https://www.micron.com/products/ultra-bandwidth-solutions/gddr6x
  - Micron Technical Brief
- First use of single-ended PAM4 I/O signaling
- Pushes single-ended I/O speeds beyond 16 Gb/s, targeting up to 32 Gb/s



PAM4 Benefit – Beyond 16 Gb/s

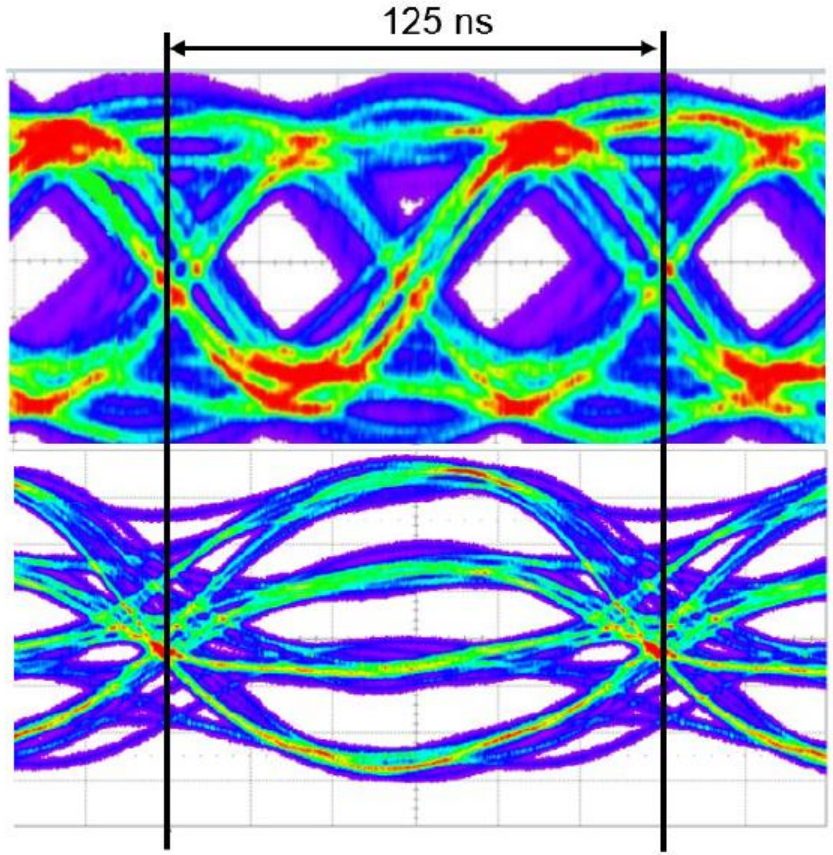
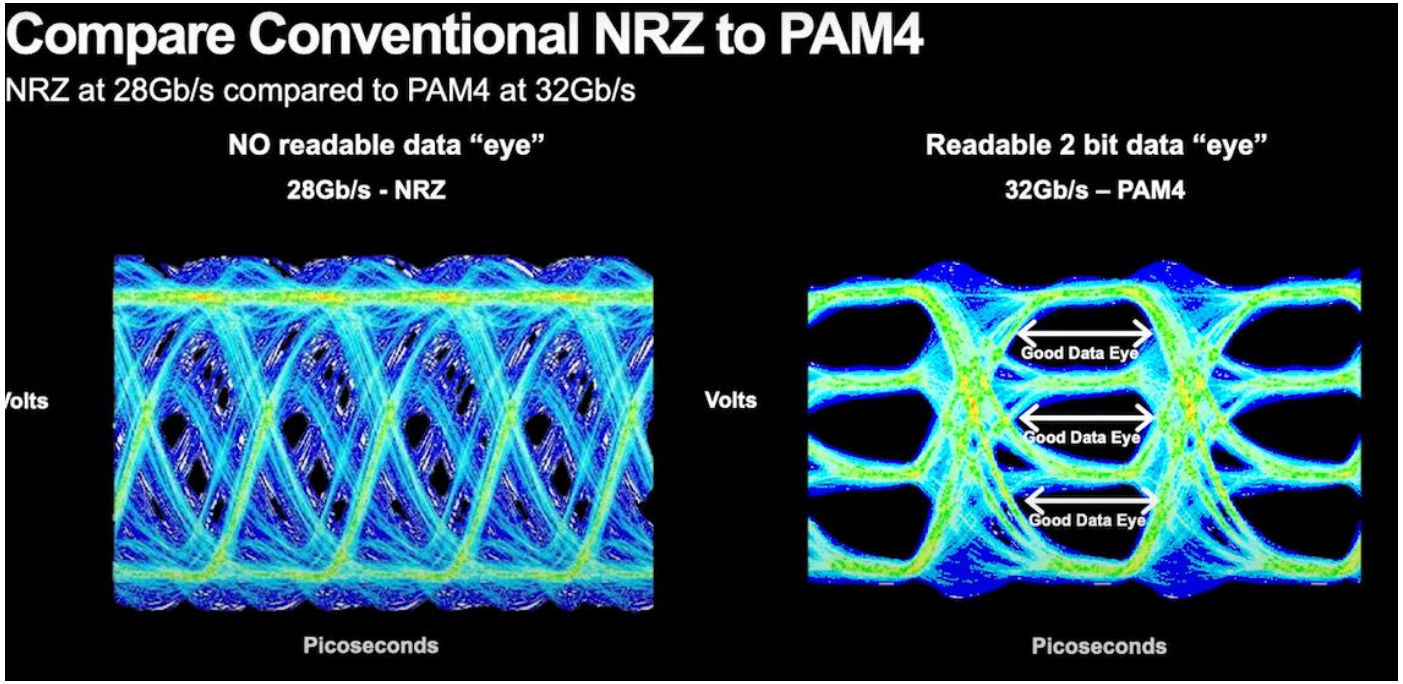


Figure 2: Data Eye Comparison Between GDDR6 (top) and GDDR6X (bottom) That Shows the Timing for a 2 Bits Data Transfer at 16Gb/s



Tx/Rx Specs

- Tx/Rx Equalization
- VDD/VDDQ @ 1.25V or 1.35V
- Datarate (today): 19Gb/s, 21 Gb/s, >21 Gb/s (per pin)
- Data is gray-coded
- V_{REFD} level internal per pin (64 steps), 3 sub-receivers per pin
- 40/48 Ohm ODT

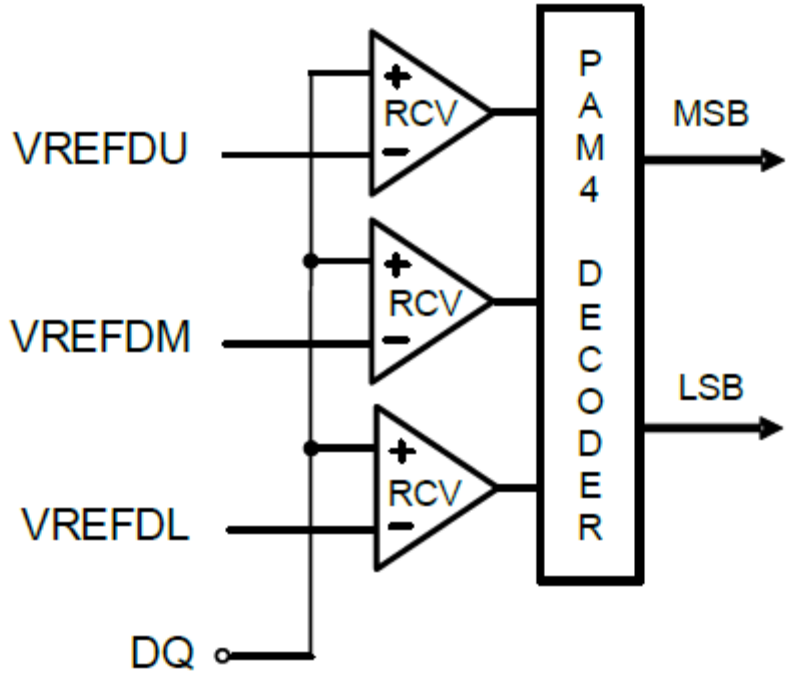


Figure 4: PAM4 Receiver

Tx Impedances

- Tx implemented with 60/120 Ohm PU/PD legs

Logical	Symbol	Physical
10	+3	
11	+1	
01	-1	
00	-3	

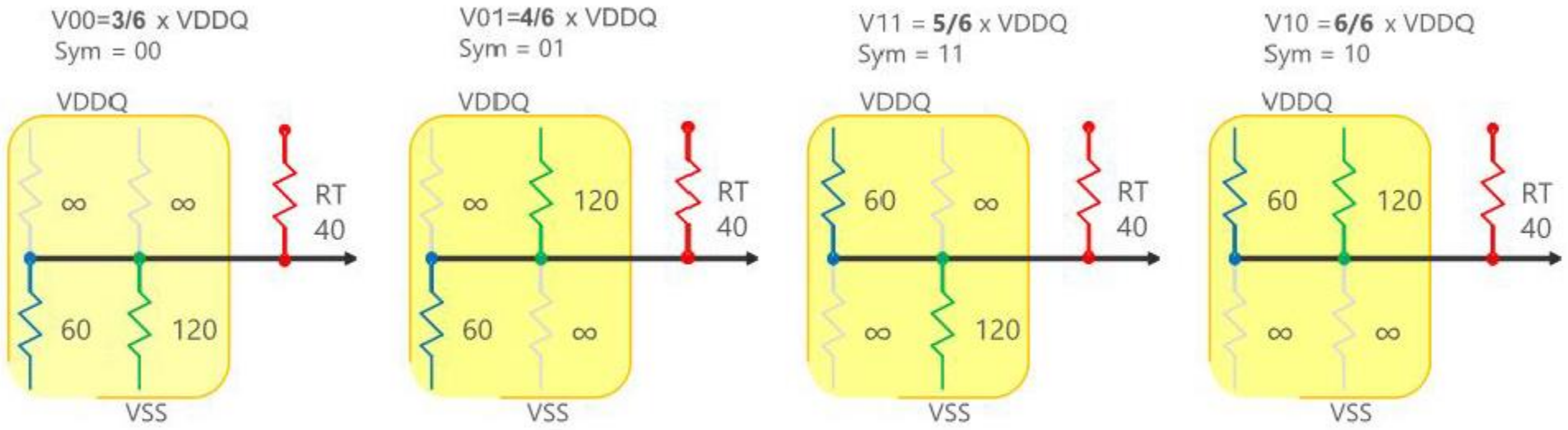
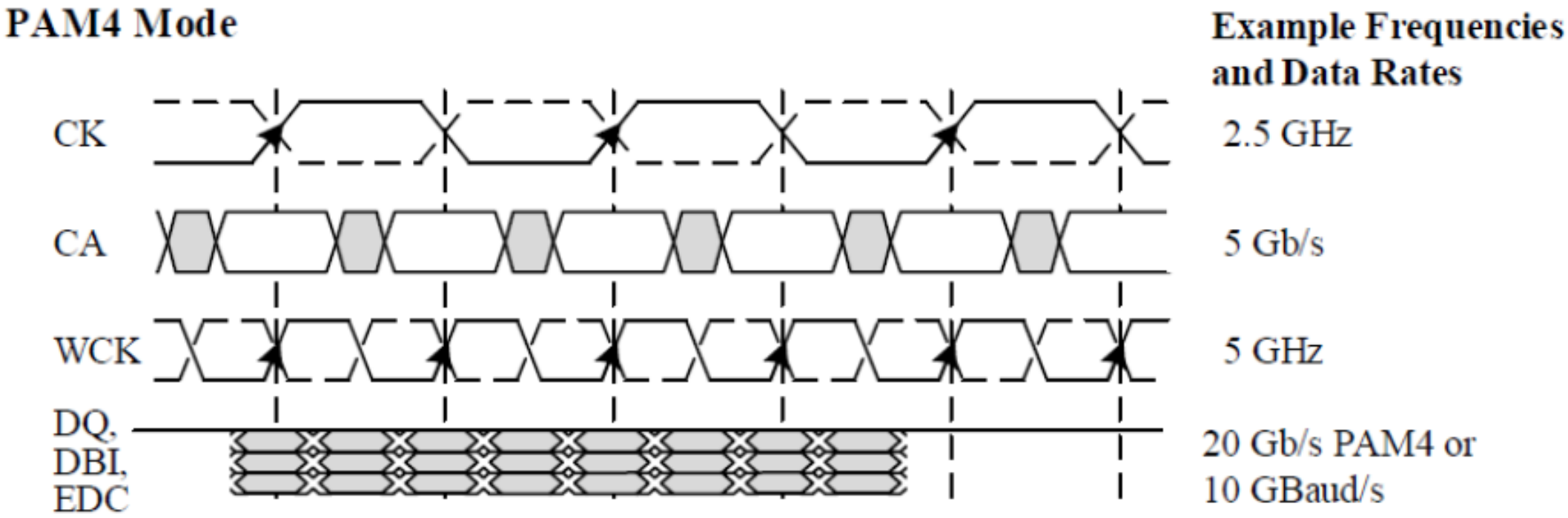


Figure 5: PAM4 Impedance Scheme

Clocking


PAM4 Mode
Example Frequencies and Data Rates
CK
2.5 GHz
CA
5 Gb/s
WCK
5 GHz
DQ, DBI, EDC
20 Gb/s PAM4 or 10 GBaud/s

What may be needed from IBIS?

- IBIS
  - New Model_Types (I/O_PAM4, Input_PAM4, Output_PAM4)
    - MSB/LSB input stimuli
    - Multiple Pullup/Pulldown curves
    - 6 sets of V-t waveforms
    - [Driver Schedule]-like architecture?

- IBIS-AMI
  - EDA tools will need to support new IBIS buffer model for time-domain channel characterization
    - Multiple edge responses (more than single rise/fall edges)
    - Multiple bit responses for superposition techniques
  - PAM4_*Threshold levels are V_{REFD} levels. How to set these?
  - Any special handling of DC_Offset?
  - Revamp of IBIS Section 10.7

IBIS-AMI Simulation Results
- Are new buffer models needed?

G6X Simulation Setup

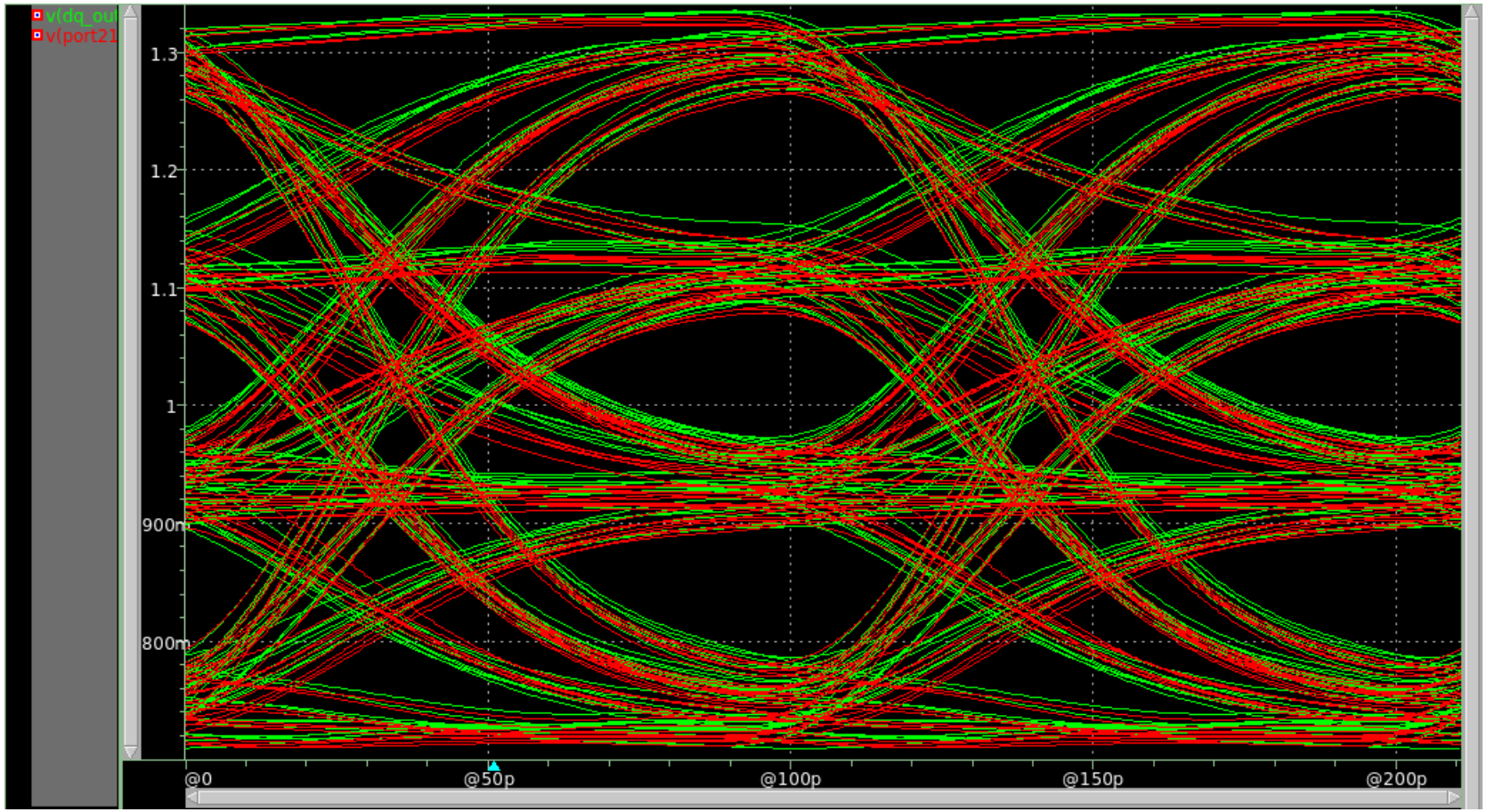
- G6X-specific channel model (S-parameter)
- Single DQ simulation
- Datarate: 19 Gb/s PAM4 (105.26ps UI)

- TX models compared
  - Transistor-level SPICE model
    - Used for transient sim
  - IBIS buffer full swing model (~40 ohms for 00-11 transition) with I-V and V-t data
    - Used for single and multi-edge IBIS-AMI sim
  - Ideal Tx with impedance and slew rate approximating pulldown characteristics of IBIS model
    - Used for single edge characterization IBIS-AMI sim
- Rx model
  - Ideal 40 ohm termination to VDDQ

SPICE vs. Single Edge IBIS-AMI sim with Ideal TX

SPICE=green, IBIS-AMI=red

Pullup and pulldown impedance, linearity, and slew rate differences not modeled



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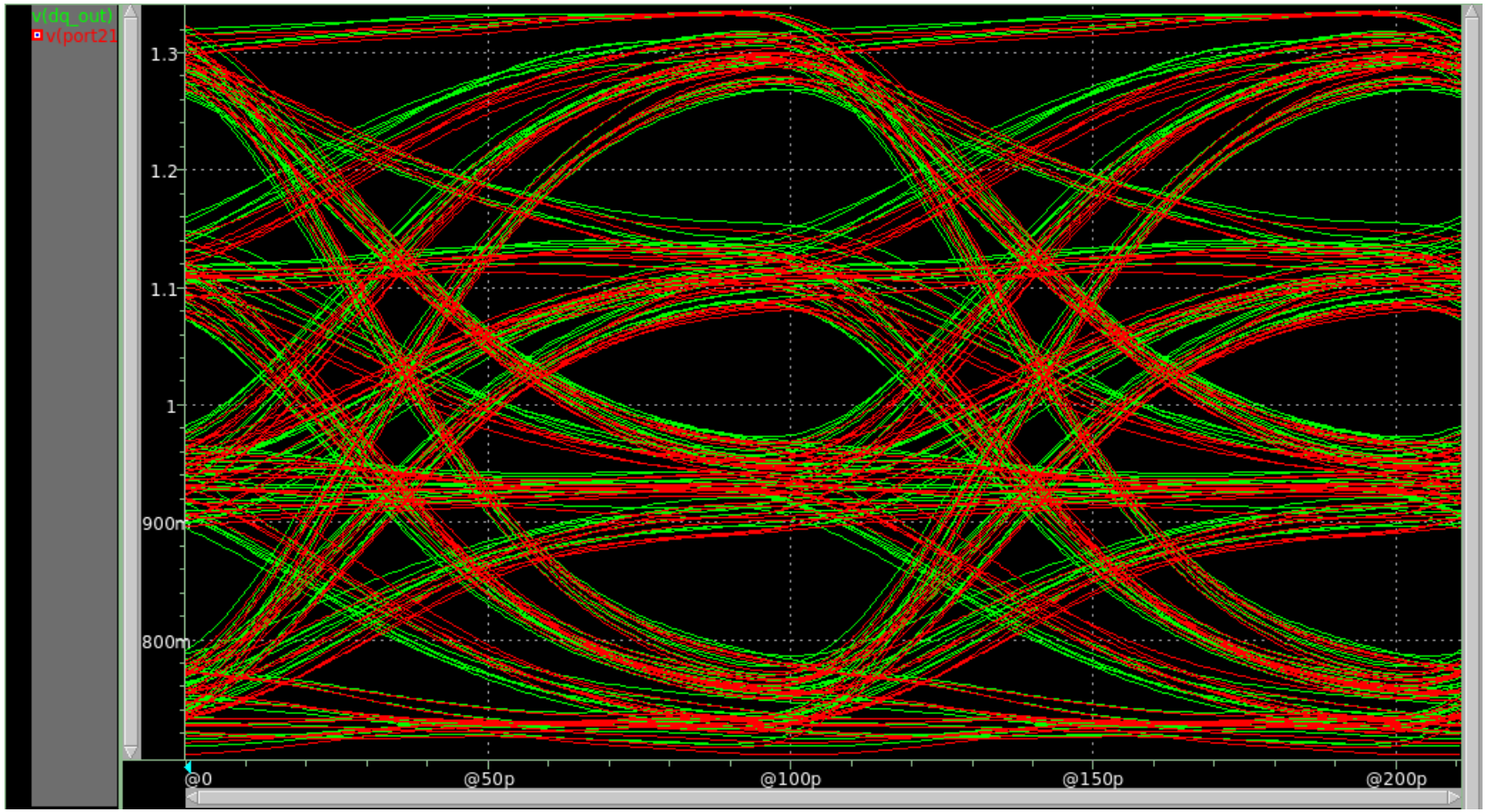
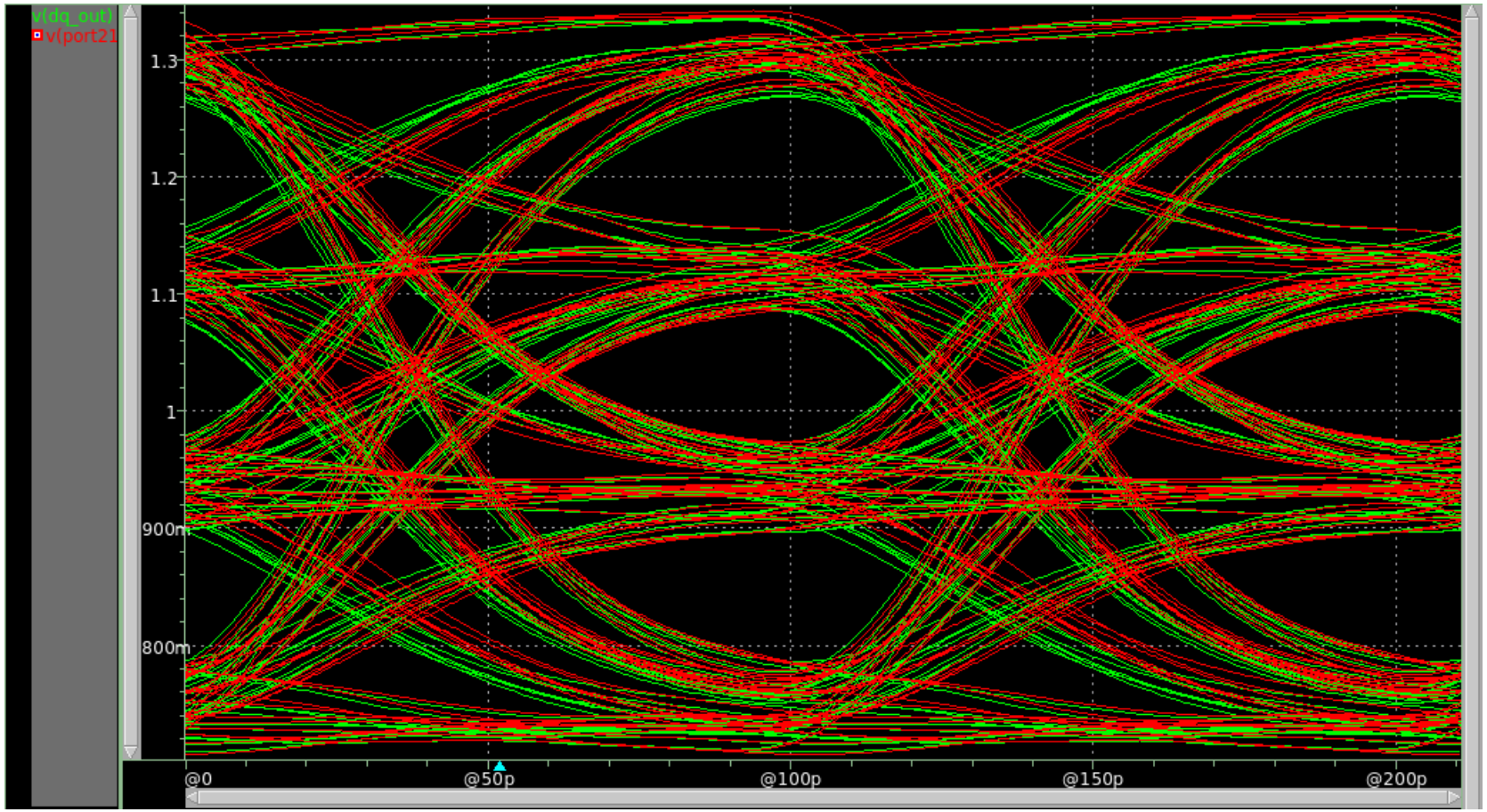


SPICE vs. Multi-edge IBIS-AMI sim with IBIS Buffer Tx

SPICE=green, IBIS-AMI=red

Eye shape improvements seen with Pullup and pulldown impedance, linearity, and slew rate differences included

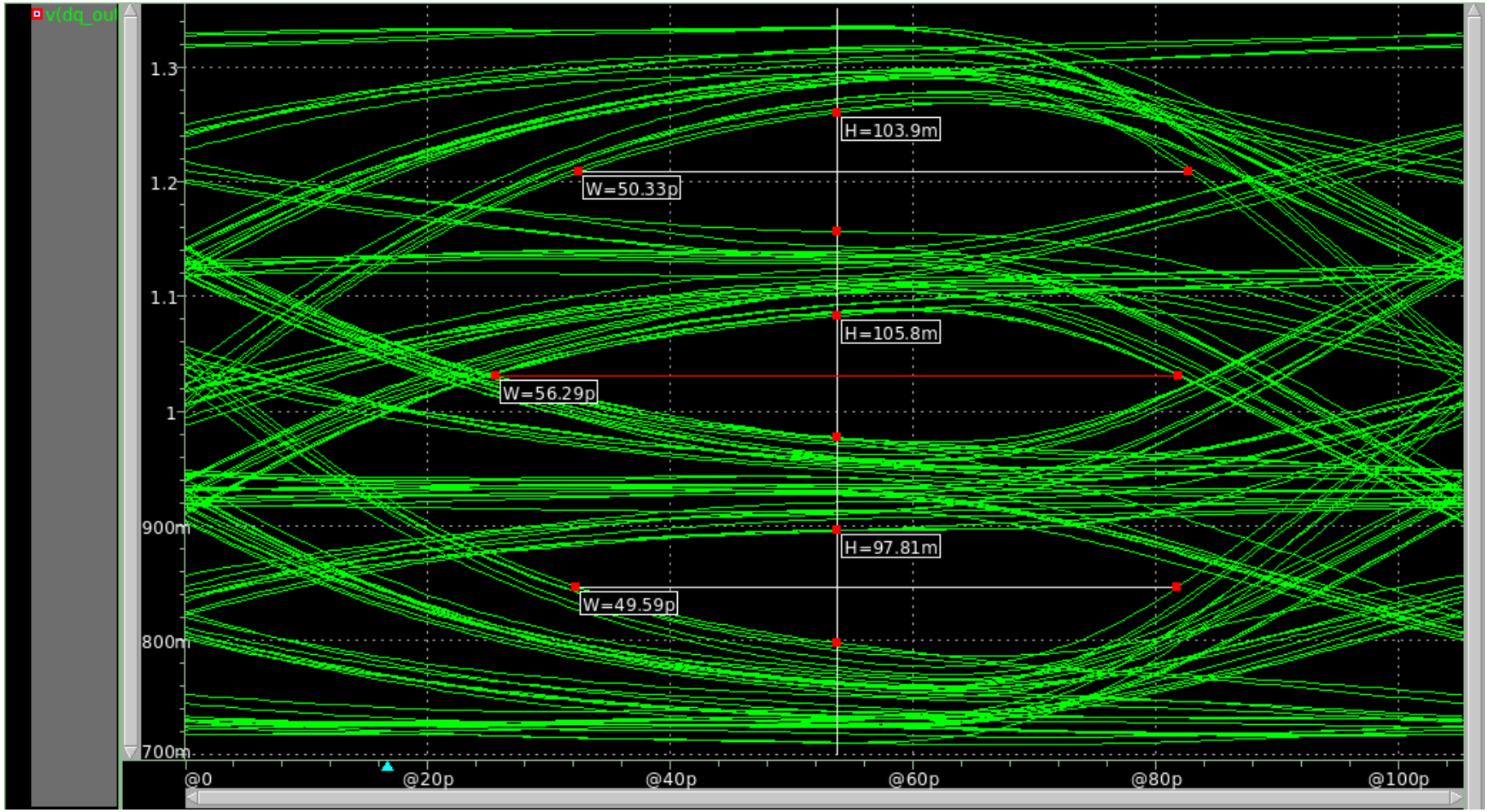


Eye Height and Eye Width Comparison

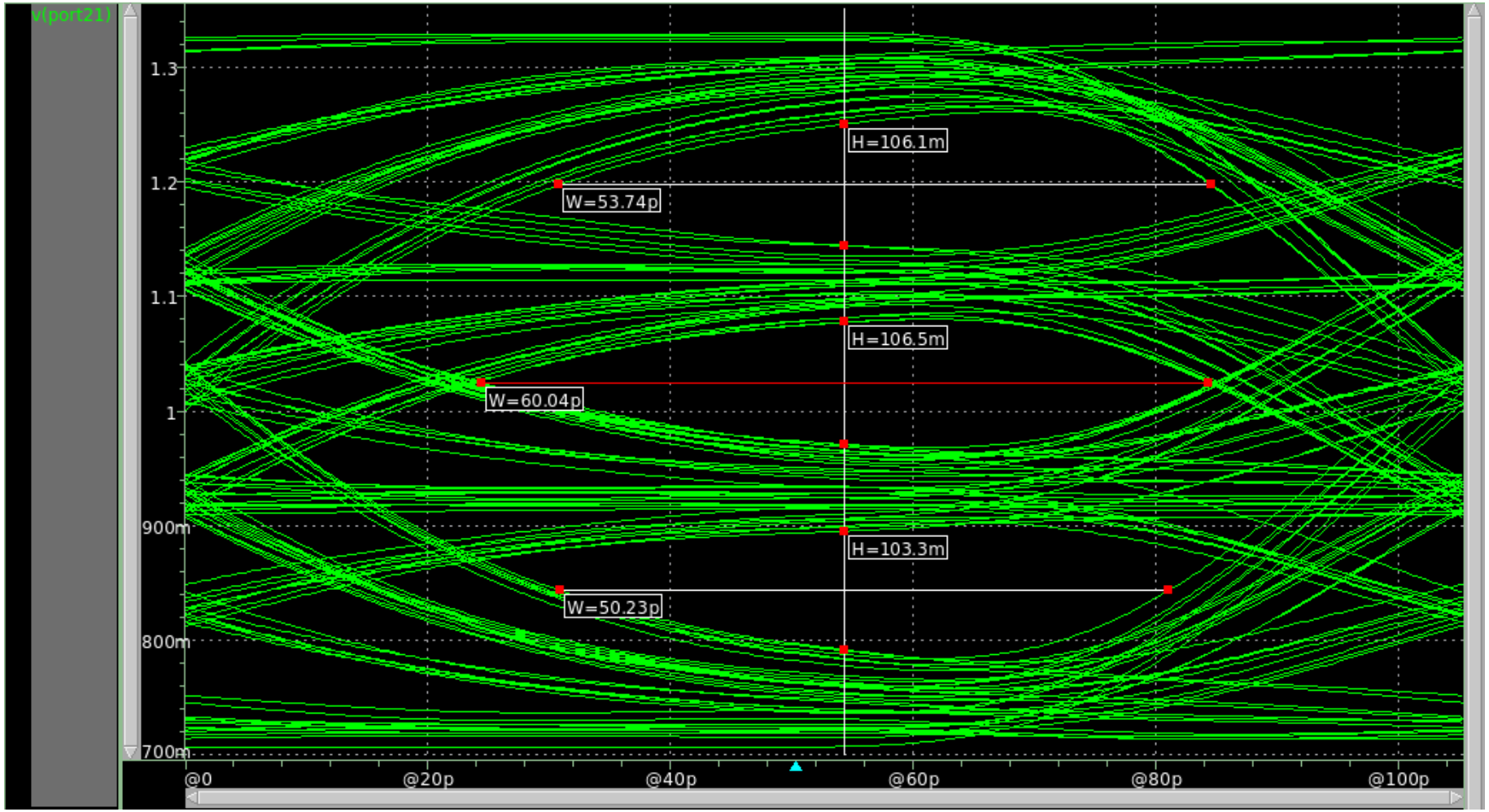
	Transient Sim SPICE Tx	AMI – Single Edge Ideal Tx	AMI – Single Edge IBIS Buffer	AMI – Multi-Edge IBIS Buffer
Upper Eye Height (mV)	103.9	106.1	105.6	98.5
Upper Eye Width (ps)	50.3	53.7	52.1	51.4
Middle Eye Height (mV)	105.8	106.5	103.9	104.3
Middle Eye Width (ps)	56.3	60.0	59.2	58.7
Lower Eye Height (mV)	97.8	103.3	98.1	98.5
Lower Eye Width (ps)	49.6	50.2	48.9	49.1

Sampling point based on timing of max eye width of center eye.
Eye Width measured at middle of voltage swing at sampling point for all eyes.

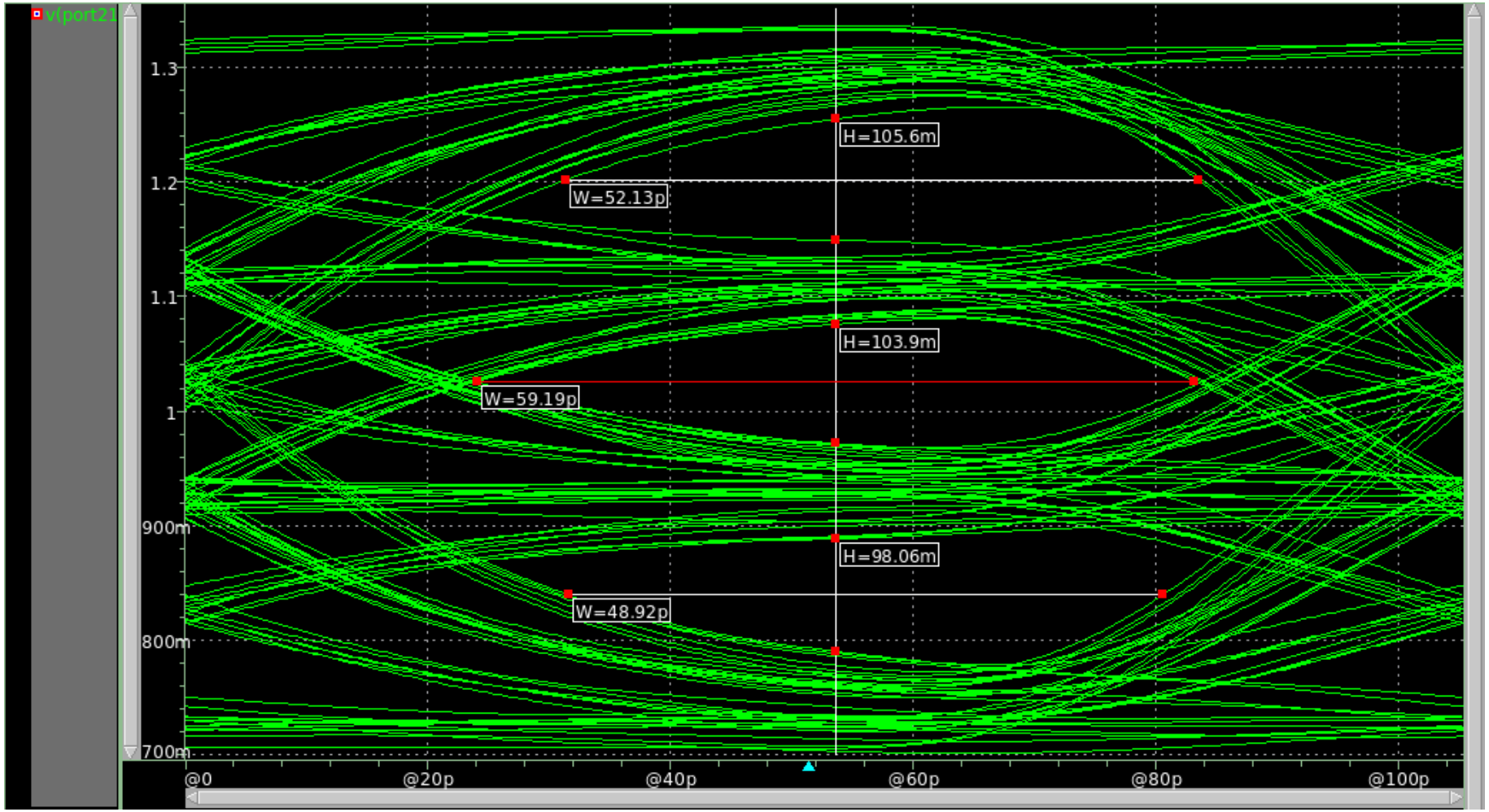
Transient Sim with SPICE Transistor-level Tx



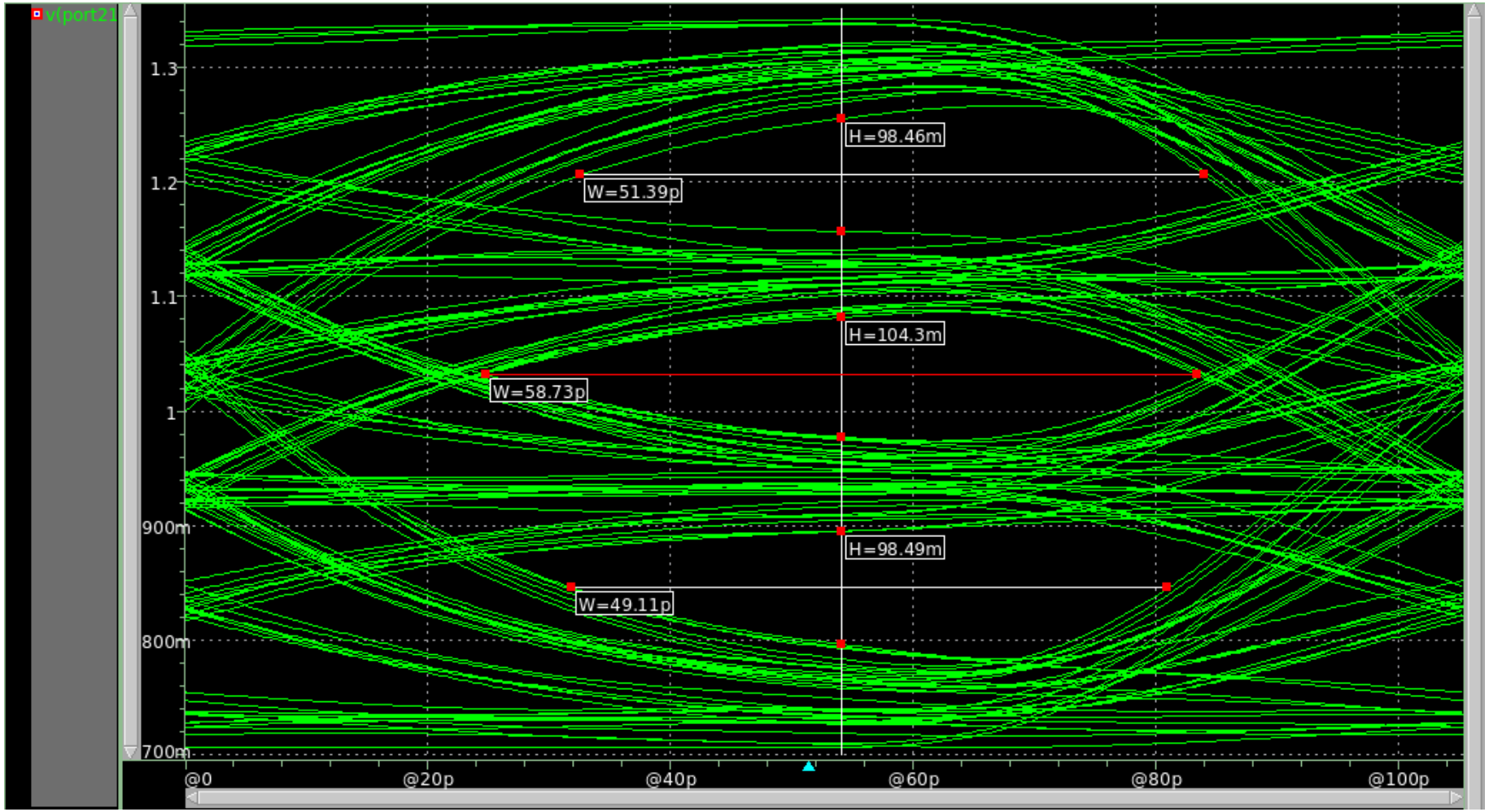
Single Edge IBIS-AMI sim with Ideal TX



Single Edge IBIS-AMI sim with IBIS Buffer TX



Multi-edge IBIS-AMI with IBIS Buffer Tx



Conclusions

- Multi-edge IBIS-AMI simulation modes developed for DDRx simulation improve accuracy
  - Eye shape improvements seen with pullup and pulldown impedance, linearity, and slew rate differences included
- Some edge transition timing does not match SPICE model in any IBIS-AMI simulation modes
  - IBIS buffer model including more I-V and V-t data could better capture edge timing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