

Output Buffer PSIJ Analysis

Can we put a BIRD on it?

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Overview

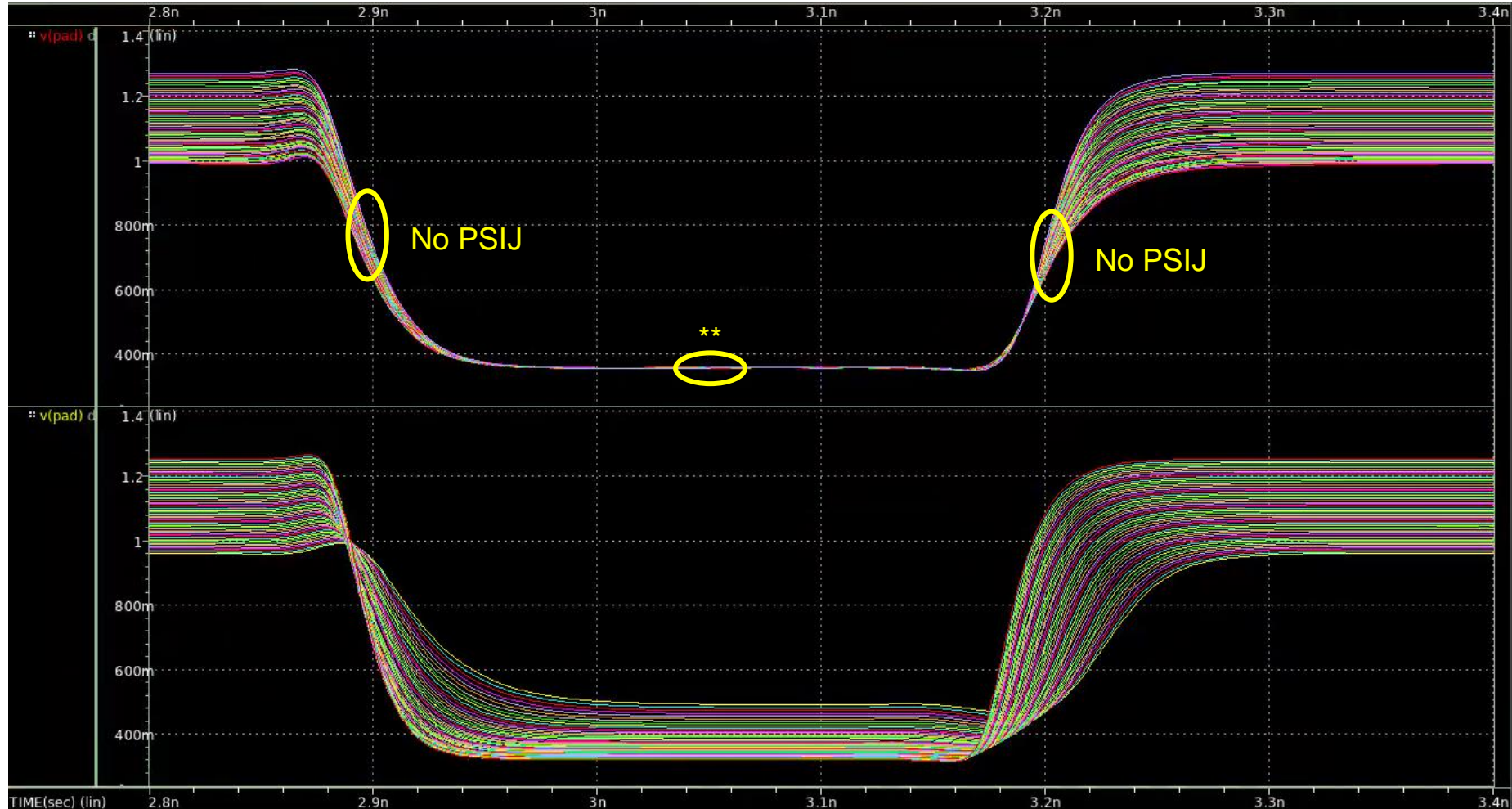
- Study Power Supply Induced Jitter (PSIJ) of a Micron Tx buffer to provide input for a new BIRD
- DDRx DQ
- Questions to analyze
 - How to measure PSIJ value?
 - Are there test load dependencies?
 - 50-ohm load to VTT = VSS, VDDQ (fixed), or VDDQ (variable)
 - What voltage level to measure?
 - Fixed or VDDQ-dependent
 - How to vary VDDQ, VSS, or both?
 - How does the test load measurement compare to measuring the internal delay of the pre-driver logic gates?
 - Should there be unique PSIJ values for pullup and pulldown?
 - How linear is PSIJ?

What's the Problem?

HSPICE with IBIS B element (IBIS) versus transistor-level model (HSPICE)

VDDQ Sweep 0.85 - 1.35 V, Typ Corner, R load = 50 ohm to VTT=VDDQ(fixed)

IBIS



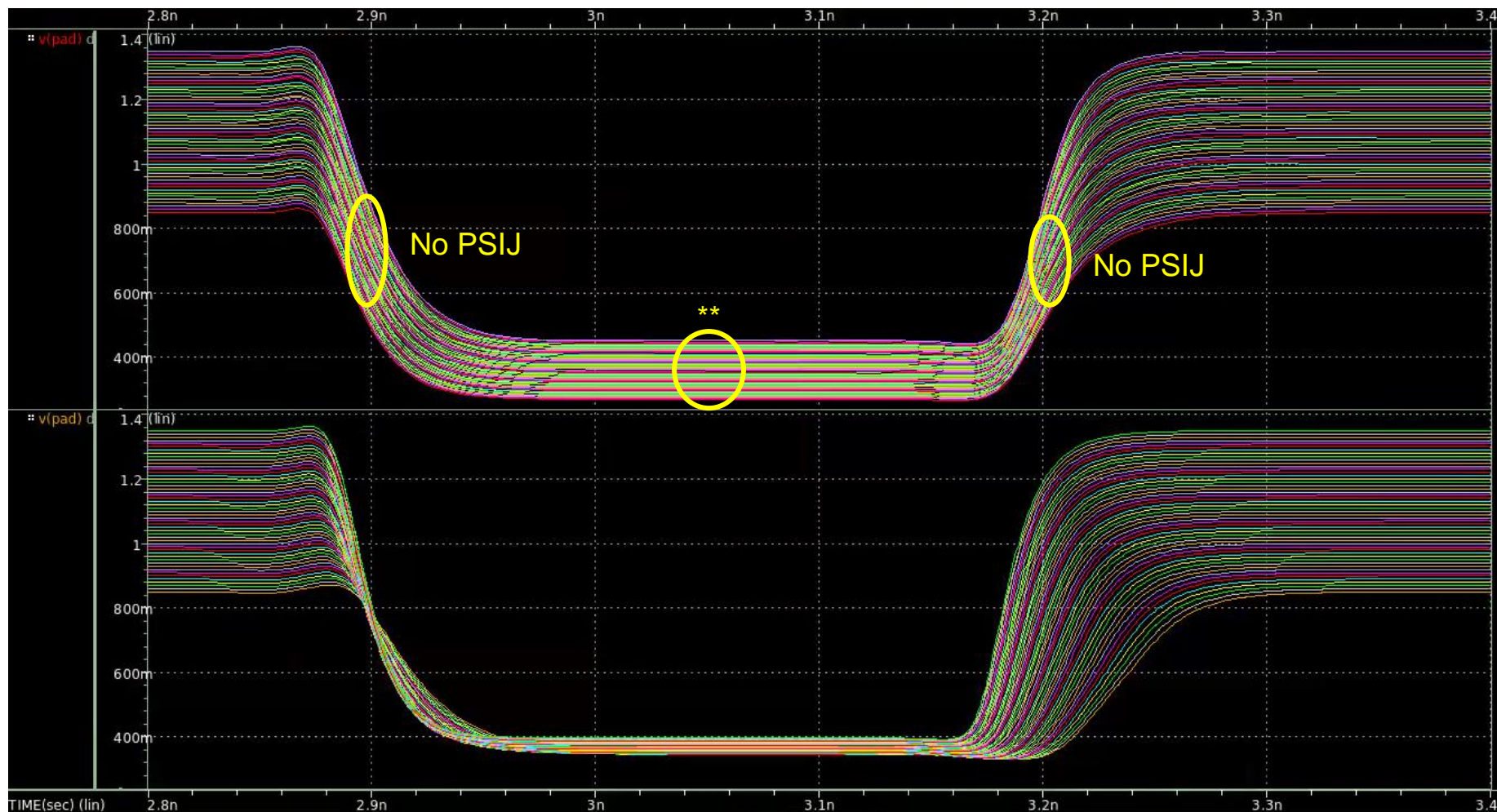
HSPICE

** Secondary issues of ISSO_PD modulation and pre-driver slew rate effects not matching transistor-level model

VDDQ Sweep 0.85 - 1.35 V, Typ Corner, R load = 50 ohm to VTT=VDDQ(variable)

IBIS

HSPICE

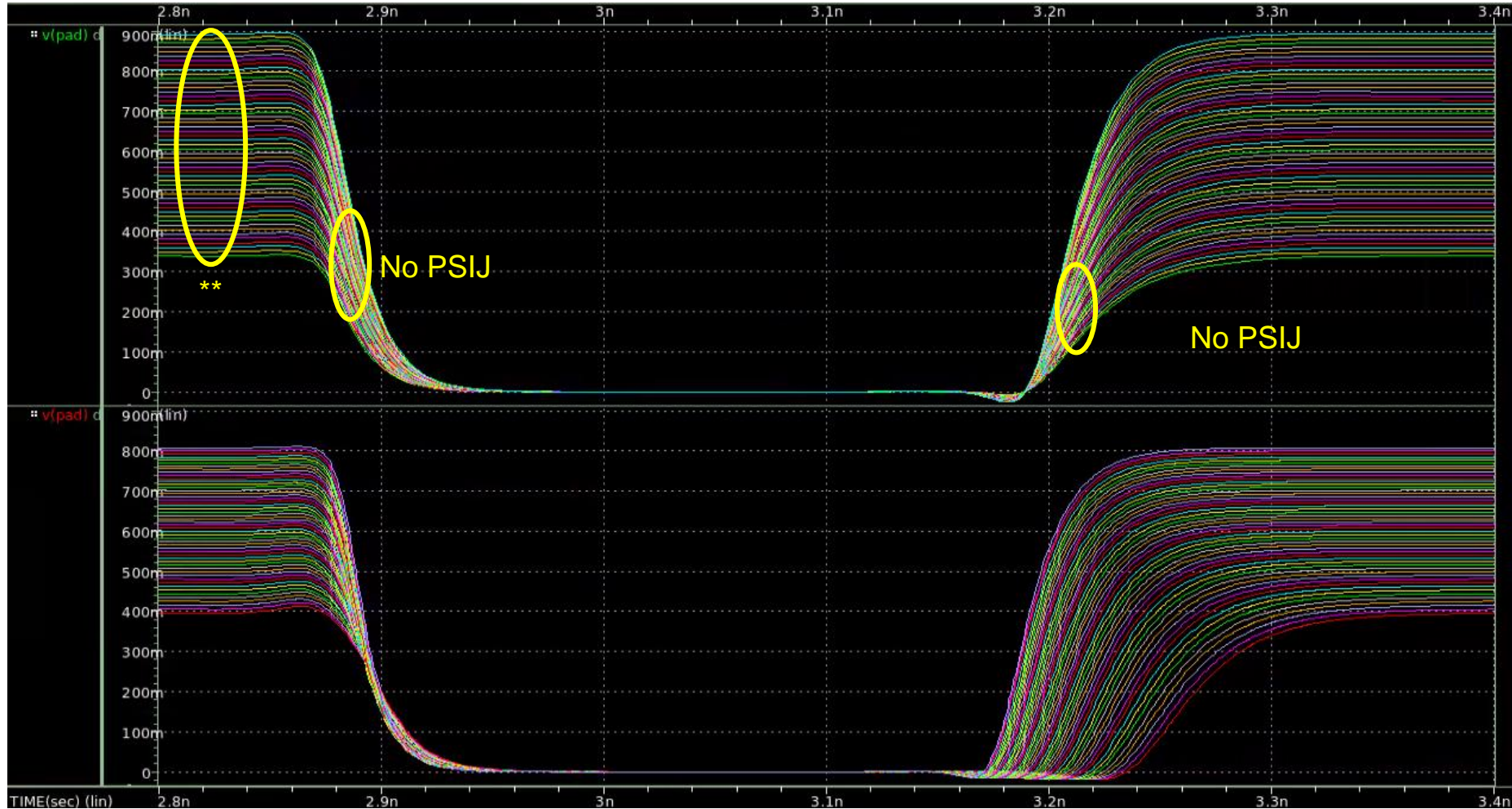


** Secondary issues of ISSO_PD modulation and pre-driver slew rate effects not matching transistor-level model

VDDQ Sweep 0.85 - 1.35 V, Typ Corner, R load = 50 ohm to VTT=VSS

IBIS

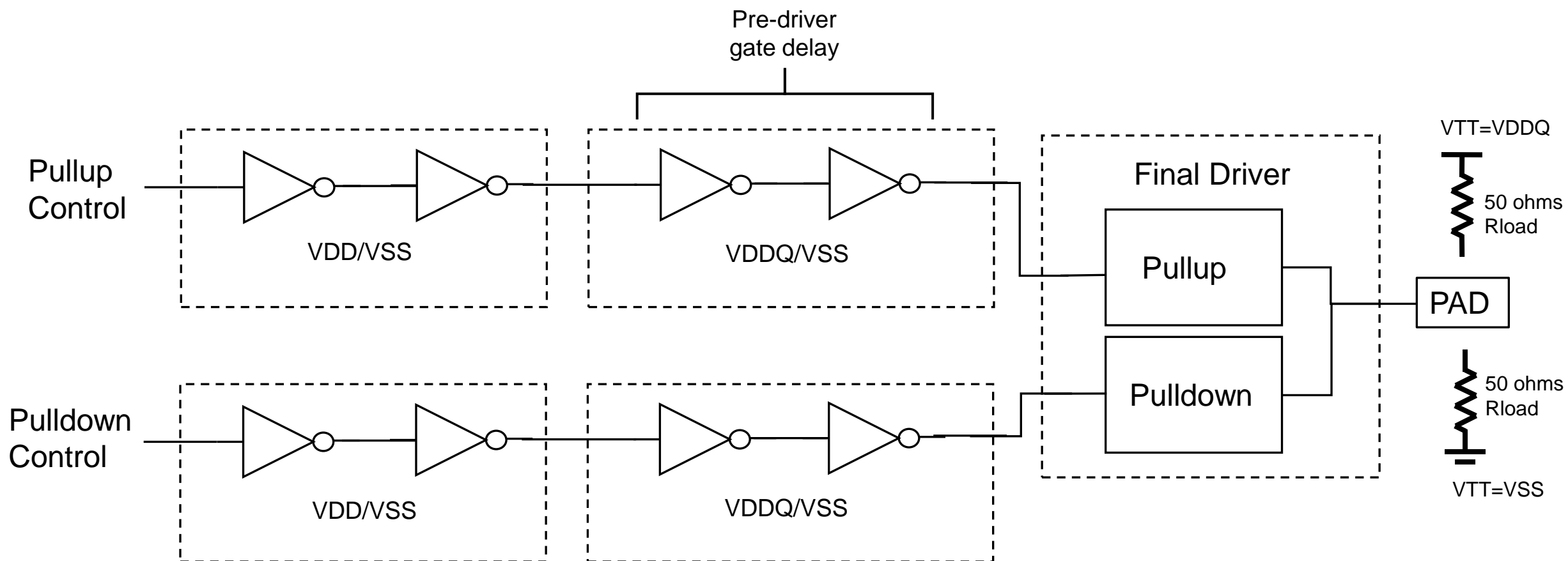
HSPICE



** Secondary issues of ISSO_PU modulation and pre-driver slew rate effects not matching transistor-level model

PSIJ Characterization

Pre-driver and Final Driver Schematic

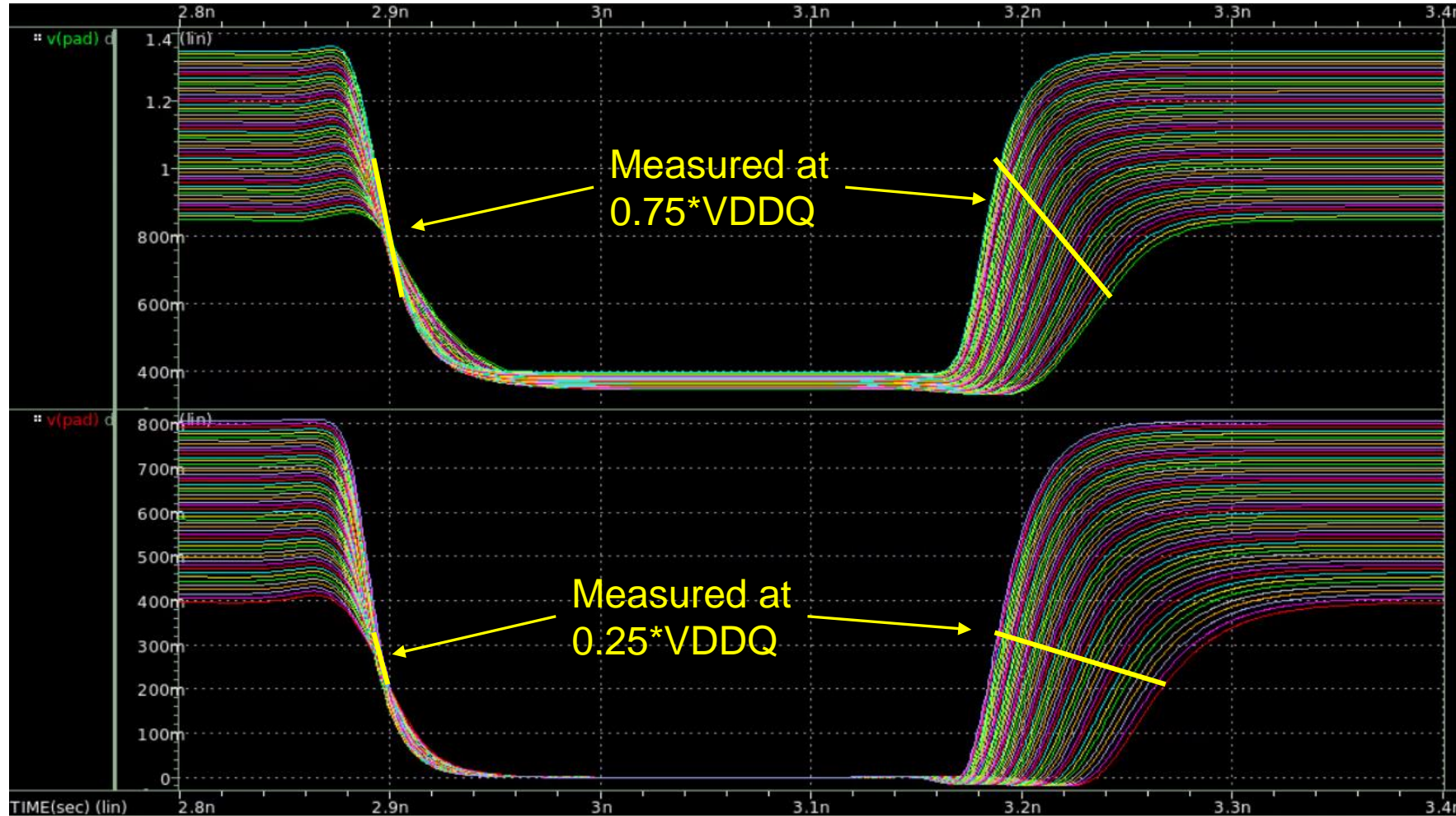


VDDQ and VSS variation controlled at this level

VDDQ Sweep 0.85 - 1.35 V, Typ Corner, VTT=Variable

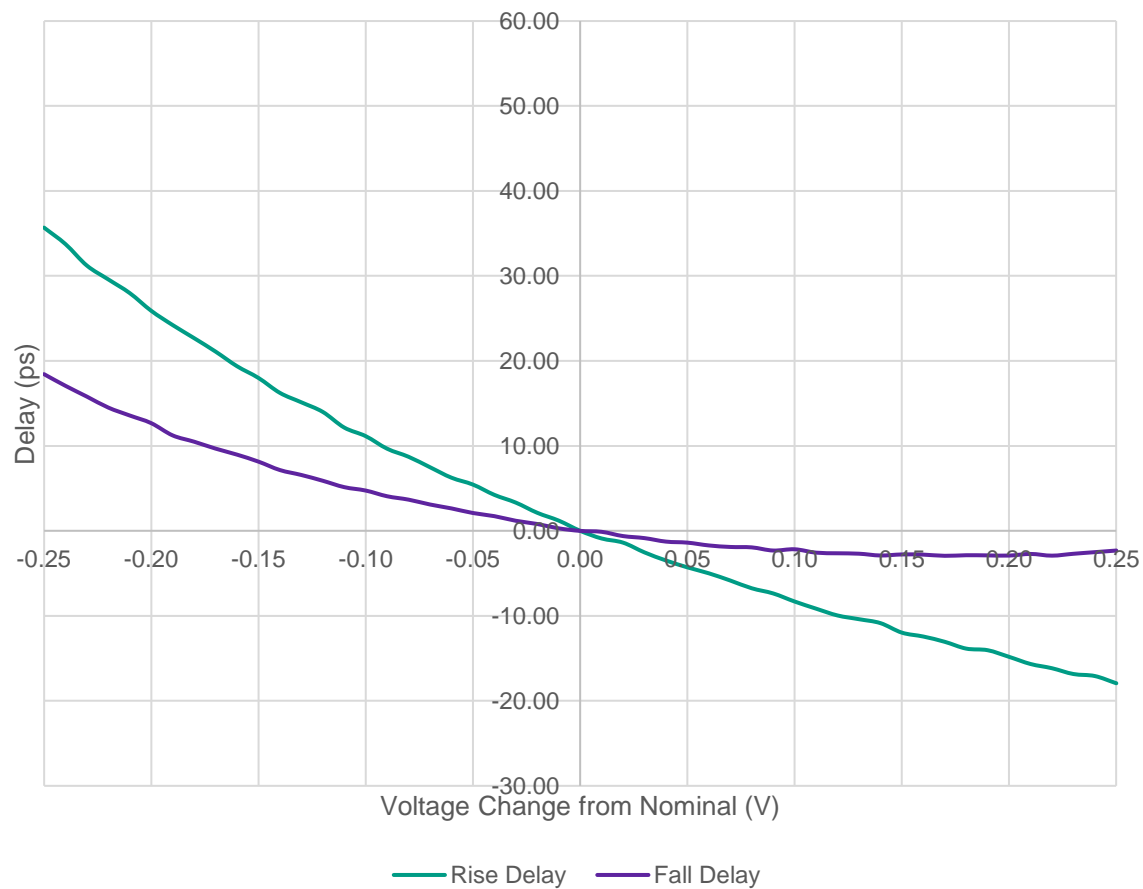
R load =
50 ohm
to VDDQ
(variable)

R load =
50 ohm
to VSS

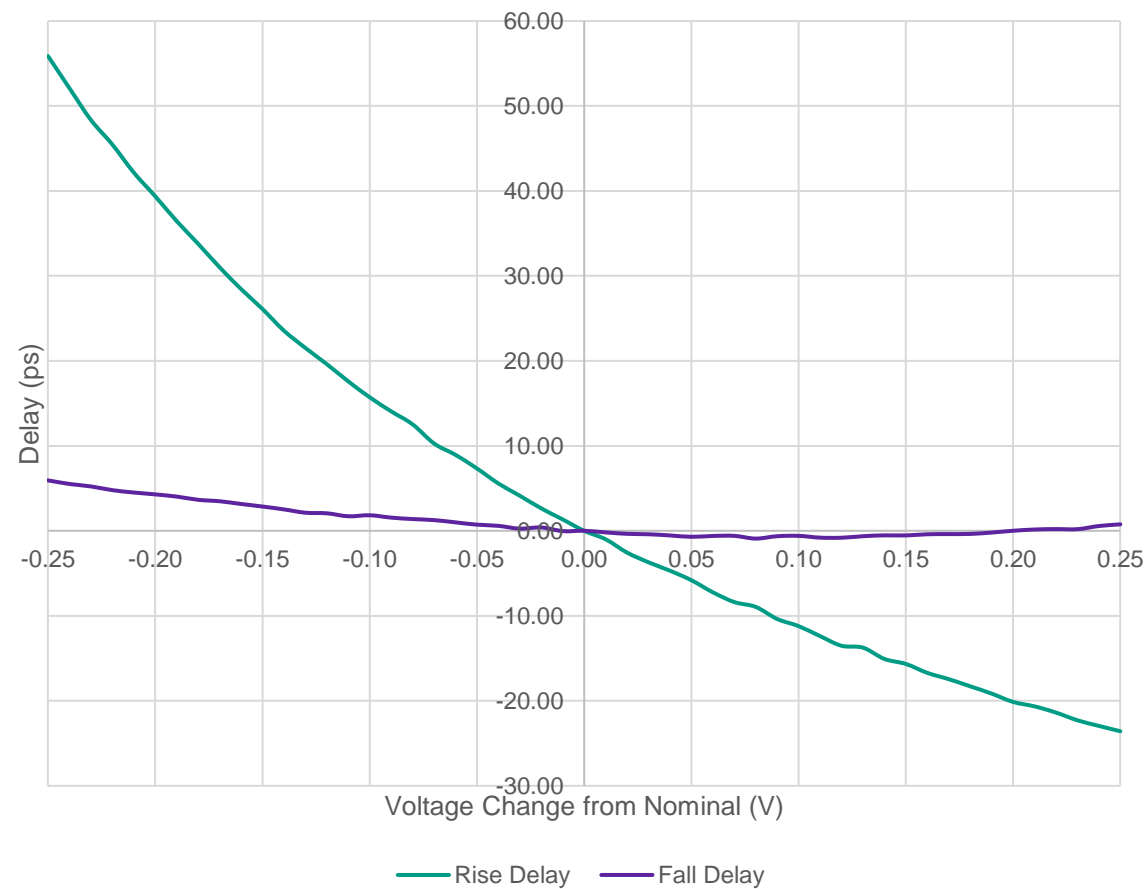


PSIJ Plots, VDDQ Sweep, VTT=VDDQ(variable) or VSS

PSIJ, Vtt=VDDQ (variable)



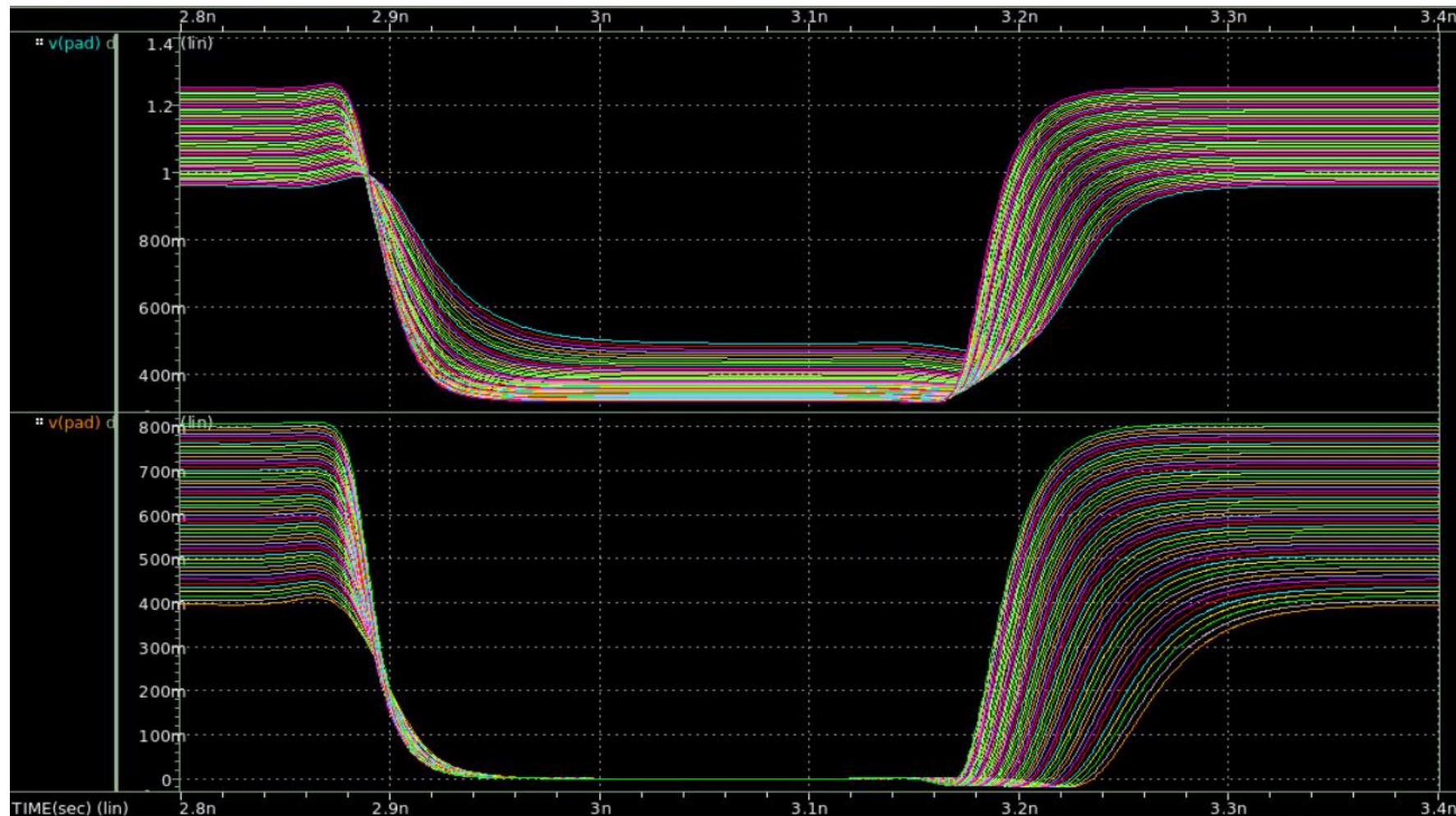
PSIJ, Vtt=VSS



VDDQ Sweep 0.85 - 1.35 V, Typ Corner, VTT=fixed

R load =
50 ohm
to VDDQ
= 1.1V
(fixed)

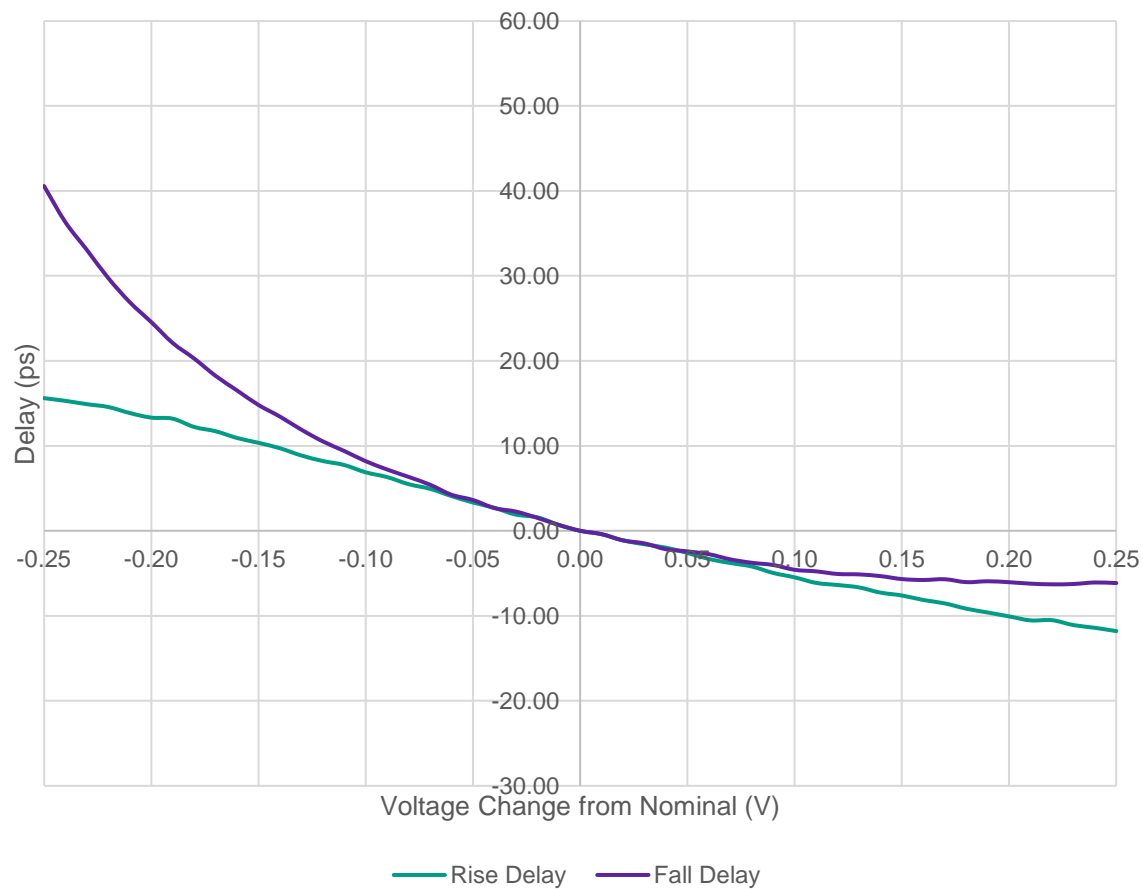
R load =
50 ohm
to VSS



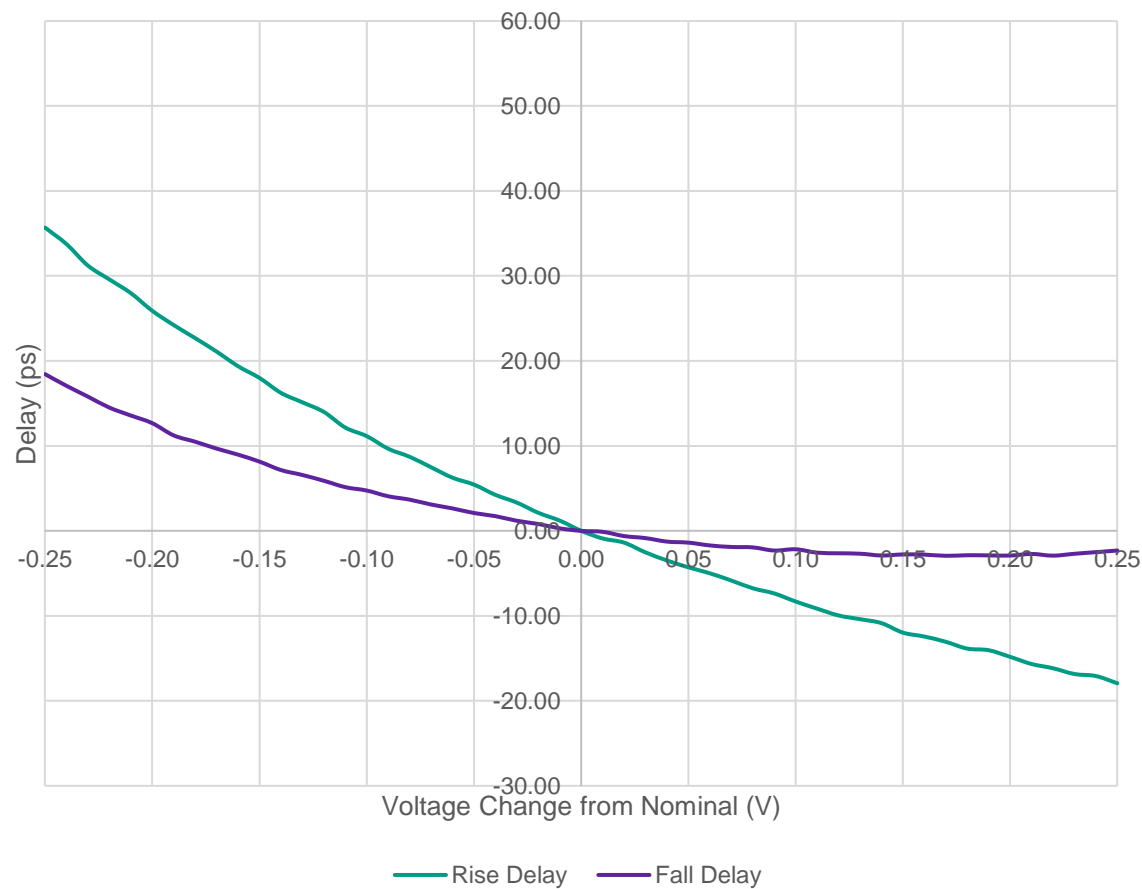
Delay from two gate pre-driver delays and Vgs modulation

PSIJ Plots, VDDQ Sweep, $V_{TT}=V_{DDQ}$ (fixed vs. variable)

PSIJ, $V_{tt}=V_{DDQ}$ (fixed)



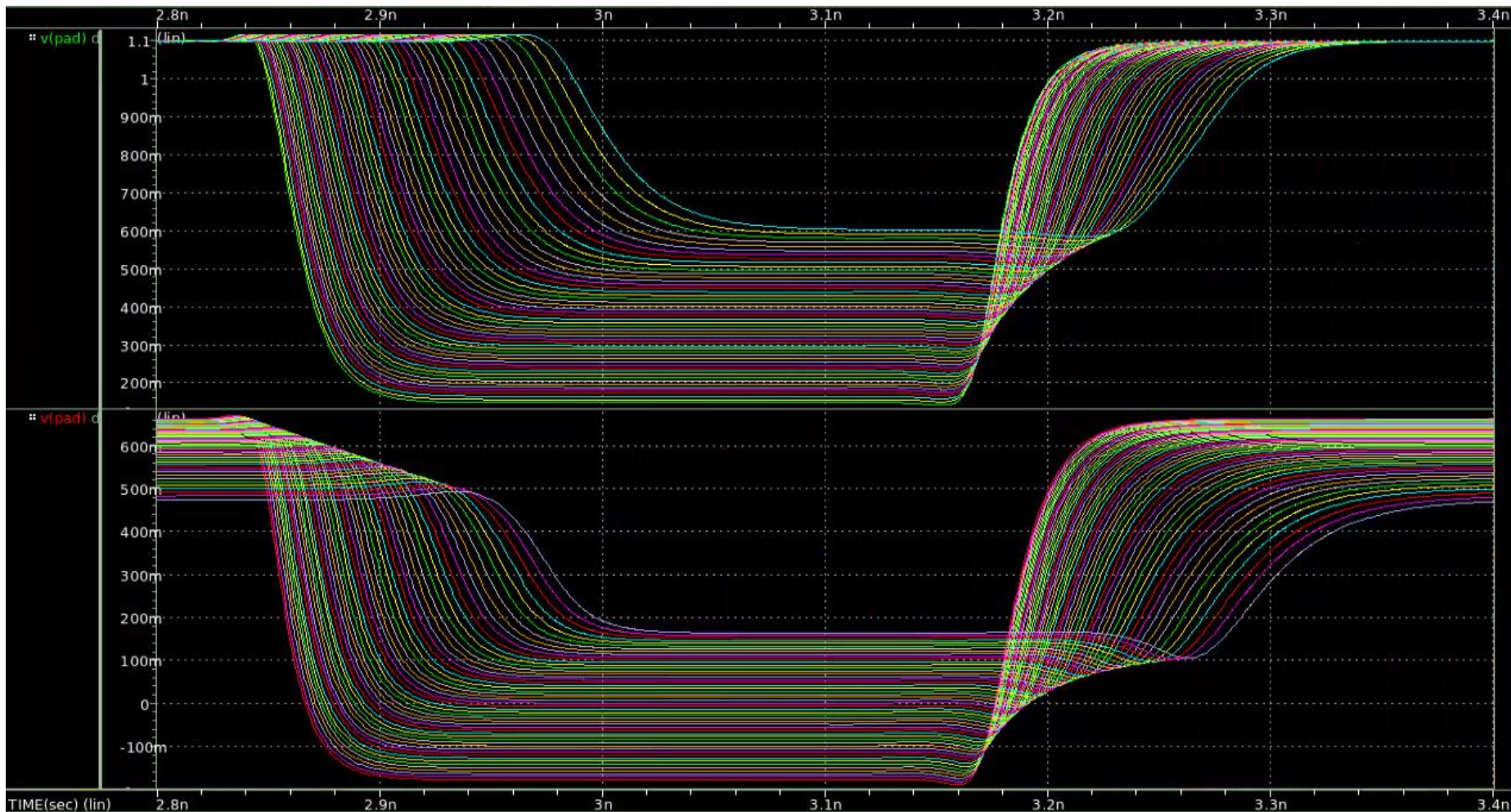
PSIJ, $V_{tt}=V_{DDQ}$ (variable)



No change to $V_{TT}=V_{SS}$ plot

VSS Sweep -0.25 - 0.25 V, Typ Corner, $V_{TT}=V_{DDQ}$ (fixed) or VSS

R load =
50 ohm
to 1.1V



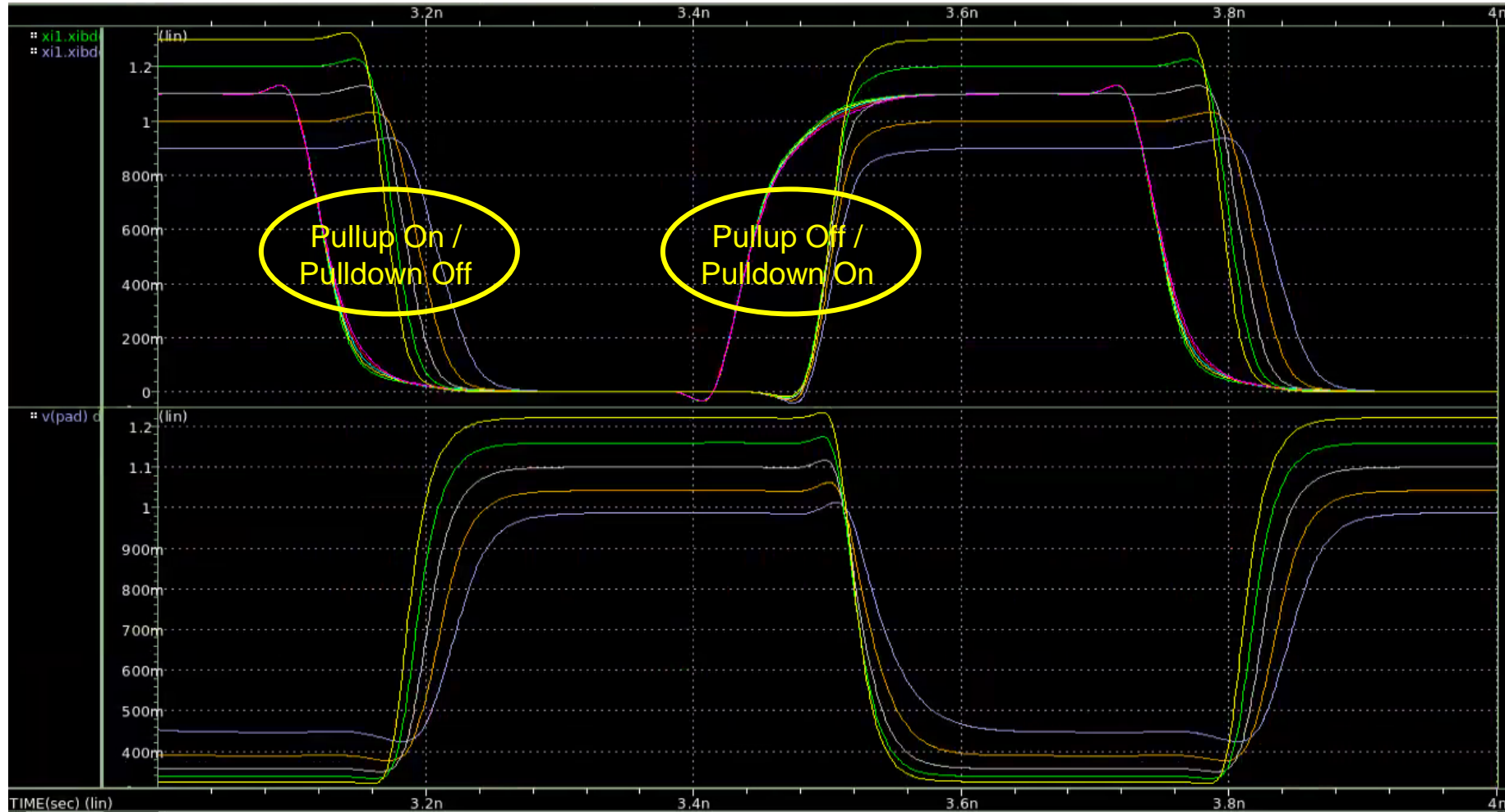
R load =
50 ohm
to 0V

VSS not easily isolated to “VSSQ” domain transistors, so isolated to circuits shown in slide 7.

Pre-driver Delay Characterization

Pullup/Pulldown Pre-driver Delays

Pre-driver
IN & OUT



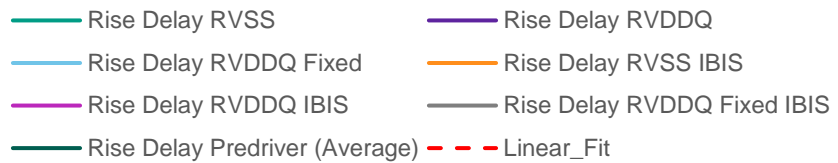
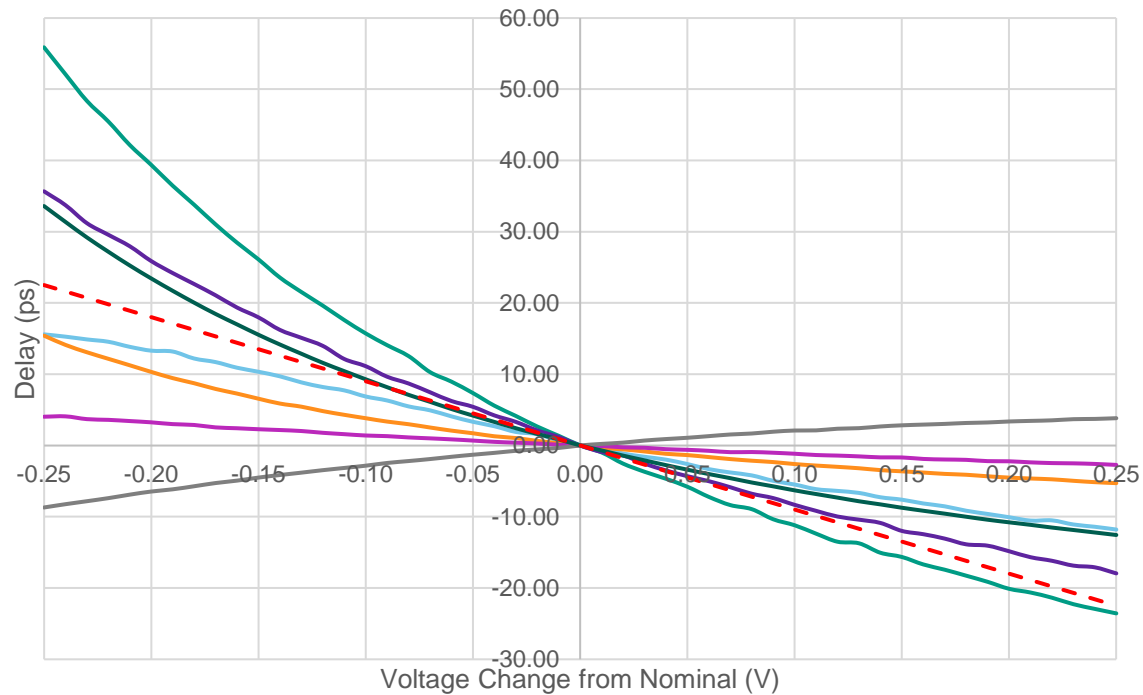
PAD

Note: Waveforms shown for VDDQ sweep with smaller range and step size than in other plots.

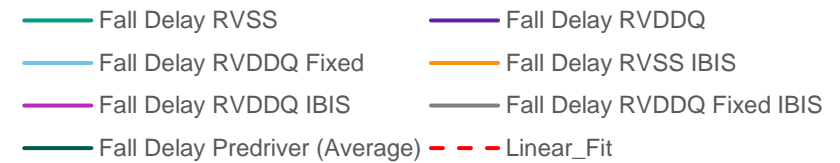
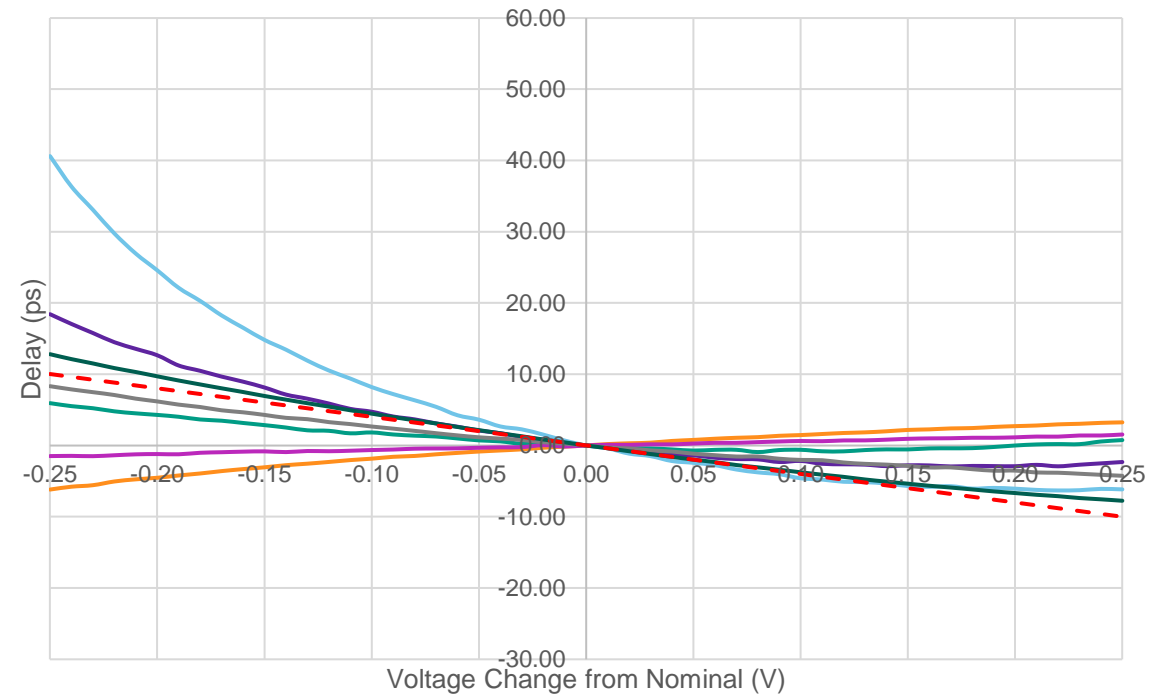
PSIJ Plots

PSIJ Plots, VDDQ Sweep

Pullup PSIJ

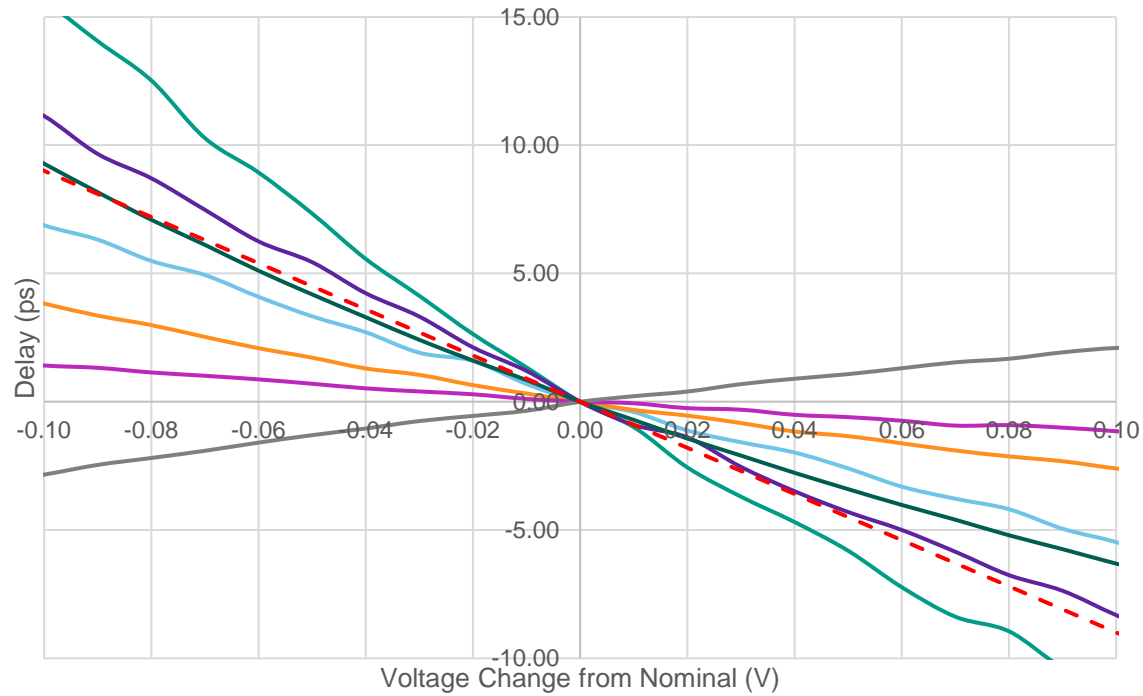


Pulldown PSIJ

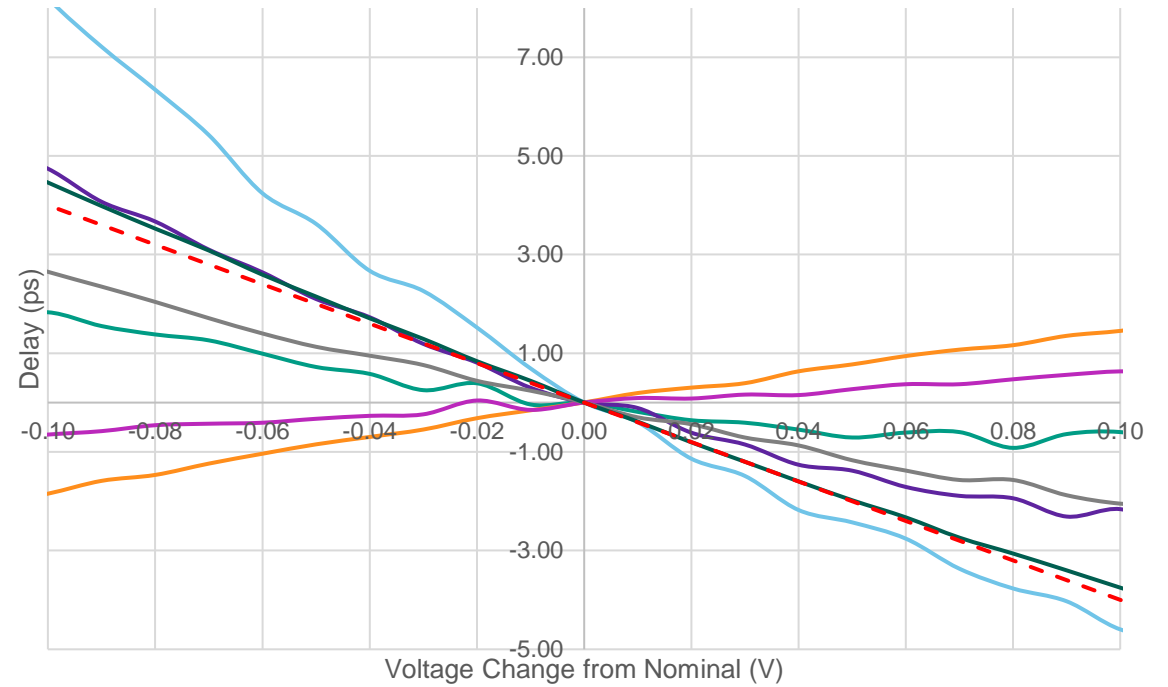


PSIJ Plots, VDDQ Sweep, Zoomed

Pullup PSIJ



Pulldown PSIJ



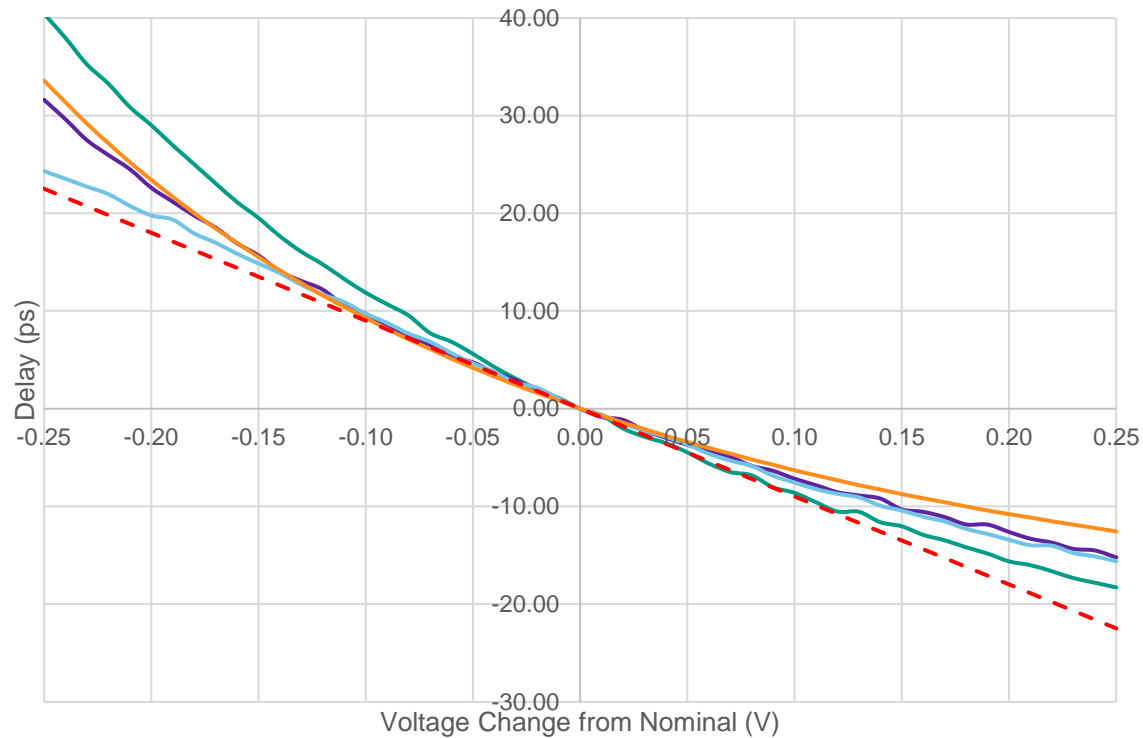
- Rise Delay RVSS
- Rise Delay RVDDQ Fixed
- Rise Delay RVDDQ IBIS
- Rise Delay RVSS IBIS
- Rise Delay RVDDQ Fixed IBIS
- Rise Delay Predriver (Average)
- - - Linear_Fit
- Rise Delay RVDDQ

- Fall Delay RVSS
- Fall Delay RVDDQ Fixed
- Fall Delay RVDDQ IBIS
- Fall Delay RVSS IBIS
- Fall Delay RVDDQ Fixed IBIS
- Fall Delay Predriver (Average)
- - - Linear_Fit
- Fall Delay RVDDQ

Pullup PSIJ ~90 ps/V, Pulldown PSIJ ~40 ps/V

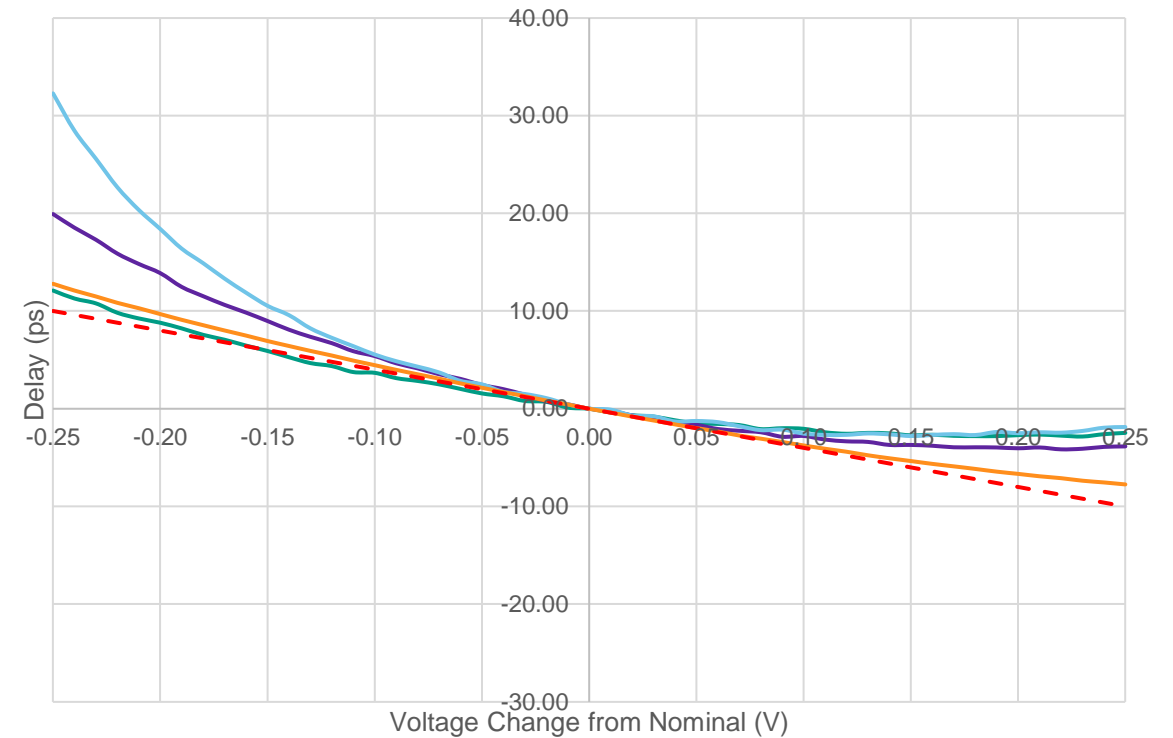
PSIJ Plots, VDDQ Sweep, Subtracting IBIS Sim Jitter

Pullup PSIJ



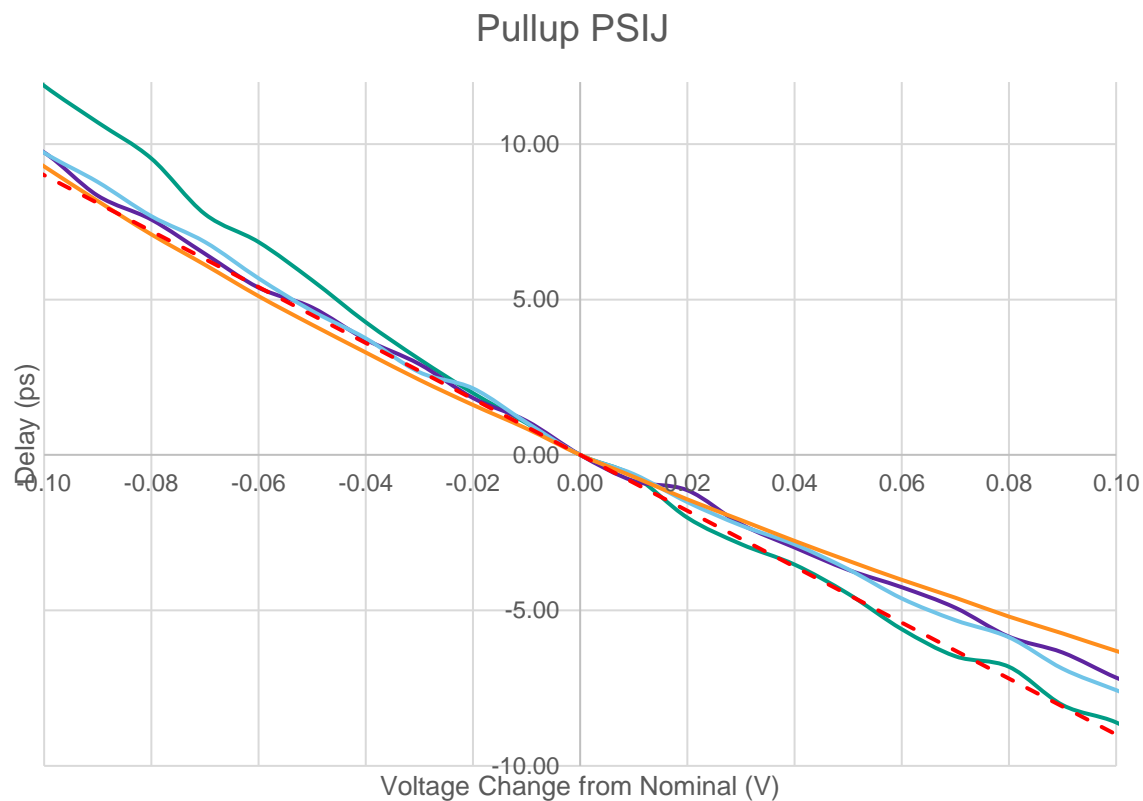
— Rise Delay RVSS (-IBIS) — Rise Delay RVDDQ (-IBIS)
— Rise Delay RVDDQ Fixed (-IBIS) — Rise Delay Predriver (Average)
- - - Linear_Fit

Pulldown PSIJ

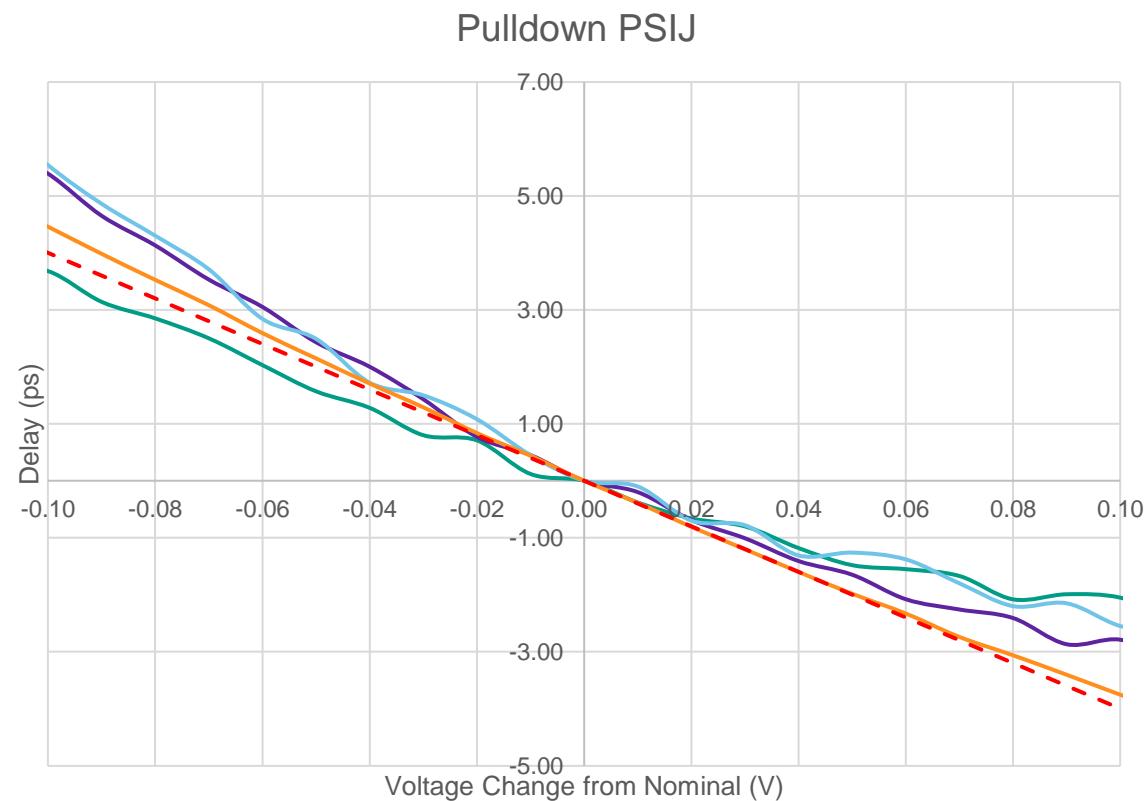


— Fall Delay RVSS (-IBIS) — Fall Delay RVDDQ (-IBIS)
— Fall Delay RVDDQ Fixed (-IBIS) — Fall Delay Predriver (Average)
- - - Linear_Fit

PSIJ Plots, VDDQ Sweep, (-) IBIS Sim Jitter, Zoomed



— Rise Delay RVSS (-IBIS) — Rise Delay RVDDQ (-IBIS)
 — Rise Delay RVDDQ Fixed (-IBIS) — Rise Delay Predriver (Average)
 - - - Linear_Fit



— Fall Delay RVSS (-IBIS) — Fall Delay RVDDQ (-IBIS)
 — Fall Delay RVDDQ Fixed (-IBIS) — Fall Delay Predriver (Average)
 - - - Linear_Fit

Pullup PSIJ ~90 ps/V, Pulldown PSIJ ~40 ps/V

Wrap Up

Conclusions

- Noted that varying VDDQ voltage changes V_{GS} of final driver pulldown transistor
 - Gate modulation of pulldown device varies I_{DS} in transistor-level model but not in IBIS model
 - ISSO_PD modulates I_{DS} based on changes to V_{GS} , but only source, not gate voltage
 - Pre-driver slew rate variation also not modeled in IBIS
- Timing should be measured at a % of VDDQ to adjust relative to voltage swing at the test load. “%” should be chosen by model maker to align closer to 50% level of voltage swing. Avoid measuring beyond 20-80% swing levels.
- PSIJ can be measured with any test load but may be best to use datasheet timing test load
- PSIJ (pre-driver contribution) cannot be accurately measured from only waveform characterization at the pad due to test load and measurement method dependencies
- To estimate pre-driver PSIJ:
 - Measure the PSIJ from an IBIS model simulation to a test load
 - Subtract the IBIS PSIJ contribution from transistor-level model simulation of same test load
- PSIJ is not linear across voltage, but error is <2 ps across +/-100mV VDDQ variation

