**IBIS Open Forum Minutes**

Meeting Date: **November 17, 2014**

Meeting Location: **Taipei, Taiwan**

**VOTING MEMBERS AND 2014 PARTICIPANTS**

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 Feng Miao, Zuli Qin, Haisan Wang, Hui Wang

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 Xianzhao Zhao

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 Xuefeng Chen, Jinghua Huang, Lianpeng Sang

 Deng Shi

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 (Teraspeed Consulting Group)

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 Changgang Yin, Shunlin Zhu

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 Reinhard Remmert

**OTHER PARTICIPANTS IN 2014**

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Fujitsu Shogo Fujimori

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Wiwynn Corp. Scott CH Lee\*, Kevin TK Wang\*

Xpeedic Technology Wenliang Dia, Feng Ling, Zhouxiang Su

Zhejiang Uniview Technologies Fei Ye, Feng Ye

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

**UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

Date Meeting Number Meeting Password

November 20, 2014 Asian IBIS Summit – Yokohama – no teleconference

December 5, 2014 205 475 958 IBIS

For teleconference dial-in information, use the password at the following website:

 <https://ciscosales.webex.com/ciscosales/j.php?J=205475958>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

 <http://www.cisco.com/web/about/doing_business/conferencing/index.html>

NOTE: "AR" = Action Required.

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**WELCOME AND kEYNOTE COMMENTS**

The Asian IBIS Summit took place on Monday, November 17, 2014 at the Sherwood Hotel in Taipei. Approximately 59 people from 19 organizations attended.

The statements below summarize the material presented. More details are available through the summit presentations posted online at:

<http://www.eda.org/ibis/summits/nov14b/>

Michael Mirmak convened the meeting, welcomed the attendees and thanked the IBIS Open Forum for their ongoing support of the IBIS Summit series in the Republic of China. Michael continued by thanking the co-sponsors: the major sponsor Intel Corporation and also the co-sponsors ANSYS, Cadence Design Systems, IO Methodology and Synopsys.

**ACTIVITIES AND DIRECTION OF IBIS**

Michael Mirmak (Intel Corporation, USA)

Michael Mirmak began by noting that the current version of IBIS is IBIS 6.0, and a parser, IBISCHK6, was released in June 2014. A user’s guide for IBISCHK6 is in development from the IBIS Quality task group and a work-in-progress document is available for review. An IBIS model review service is also available. As of today, three approved BIRDs propose major changes to IBIS 6.0, while five other approved BIRDs make clarifications or corrections. Eleven other BIRDs are proposed but not approved, and these cover areas including backchannel adaptation for equalization, expanded package modeling capabilities, Touchstone support for AMI analog buffer models and parameter passing for External Circuits. A major revision of the IBIS Open Forum basic policies and procedures is also underway. Changes to the IBIS Open Forum charter will allow for greater involvement in votes and officer elections by membership companies worldwide.

A question was asked if CTLE and DFE characteristics can be included in the "analog" descriptions for IBIS-AMI support. Michael responded that this is for the buffer impedance, not the algorithmic section; IBIS has two parts. A second question was if the Touchstone analog descriptions will be available for traditional IBIS. Michael responded yes, that is the goal; the initial intent is to have this available for AMI before traditional IBIS.

**HANDLING OF OVERCLOCKING CAUSED BY DELAY IN WAVEFORM TABLES**

Radek Biernacki\*, Ming Yang\*, Randy Wolff\*\* and Justin Butterfield\*\* (\*Keysight Technologies and \*\*Micron Technology, USA)

[Presented by Lance Wang (IO Methodology, USA)]

Lance Wang began by defining overclocking of IBIS models. He then described how power aware IBIS models can suffer from fictitious overclocking. This overclocking is imposed by EDA tools improperly handling the added delay in V-T waveforms inherent in models that include both V-T and I-T data tables. BIRD168.1 was introduced (and approved) to allow model makers to describe the intrinsic delays between pre-driver switching current and driver voltage switching. The delays can be used to define unique triggering events in the EDA software for I-T and V-T data tables. The presentation suggested that EDA tools may not be automatically processing delays correctly; only model makers know the right amount of delay to remove.

**DIFFERENTIAL BUFFER USING IBIS MODELS FOR PDN SIMULATIONS**

Lance Wang (IO Methodology, USA)

Lance Wang presented a case study of differential pair buffers in Power Delivery Network (PDN) simulations. The IBIS specification does not indicate how to make an IBIS power aware model for true differential pair buffers. Lance used a 1.5V LVDS true-differential buffer with balanced pullup and pulldowns for his study. The buffer also had access to the power supply connections for both the positive and negative signal drivers. The simulation correlated well to the transistor model when the IBIS model was extracted from separate power supplies for each of the positive and negative pins. If one doesn’t have access to each buffer’s power pins separately, this creates a problem. For this model, one can get a combined ISSO curve by setting up both pullup and pulldown, then taking the average for each buffer. For [Composite Current] waveforms, one can take one rising edge and one falling edge curve at the same time for the differential pair and add the results together. The resulting model is not a perfect correlation to the transistor model, but the results are better than using an IBIS model without the power aware features.

**TRUE DIFFERENTIAL IBIS MODEL FOR SERDES ANALOG BUFFER**

Shivani Sharma, Tushar Malik and Taranjit Kukal (Cadence Design Systems, India)

[Presented by Skipper Liang, (Cadence Design Systems, Taiwan)]

Skipper Liang gave an overview of current differential buffer modeling techniques in IBIS. An alternative approach to S-parameter characterization was shown using standard IBIS tabular data formats along with series elements to model differential current. This extended the approach suggested in the IBIS cookbook suggesting modeling of differential current using series resistance. A modeling flow was shown for extraction of common and differential mode impedances. From the impedance at a specific frequency one can calculate series and common mode reactances and resistances. Depending on the sign the reactance could be inductive or capacitive. A parallel RL network is then modeled using the series model type. A parallel RC network is modeled using C\_comp and clamp I-V tables. The true differential model provides much better accuracy than a pseudo differential IBIS model for channel simulation in terms of jitter, eye opening and reflection losses.

**IBIS AMI VALIDATION**

Zilwan Mahmod and Anders Ekholm (Ericsson, Sweden)

[Presented by Zilwan Mahmod (Ericsson, Sweden)]

Zilwan Mahmod began by describing design goals he has with IBIS AMI analysis. IBIS AMI models must be validated, as correct and validated models are needed. Certification is the first step a model must go through to check that the model behavior is reasonable. Zilwan presented a long checklist of items to verify. To do active correlation, the PCB model in simulation must be adjusted to match the real channel characteristics as seen in measurements. S-parameters from measurement can be used in the correlation exercise, but the PCB models need to be adjusted for later use in post-layout simulation. TX active validation is feasible, but RX active validation is not, because measurements at the decision point are not possible.

Zilwan's experience shows that many models fail certification for various reasons such as syntax errors, run time errors, simulated DC levels that don't match measured DC levels, idealized analog models, etc.

**SIGNING IBIS MODEL AGAINST DDR4 SPEC**

Tushar Malik and Taranjit Kukal (Cadence Design Systems, India)

[Presented by Thunder Lay (Cadence Design Systems, Taiwan)]

Thunder Lay noted that one should certify controller IBIS models before performing system simulations. If the models do not adhere to the JEDEC DDR4 standard, a designer may wrongly associate performance issues with interconnect elements. DDR4 compliance checks can include output impedance, single-ended slew rate, differential slew rate and pulse width. A methodology was shown for testing a model against these compliance checks. Thunder concluded that IBIS verification against JEDEC requirements can help in quickly verifying PHY netlists for compliance and ensuring that IBIS models have been correctly make with proper netlist settings.

**CORNER CONSIDERATIONS**

Bob Ross (Teraspeed Labs, USA)

[Presented by Anders Ekholm (Ericsson, Sweden)]

Anders Ekholm stated that corners mean the assignment of typ, min or max entries in IBIS models. Different areas of IBIS have different corner definitions. Anders reviewed the selection of corners for [Model]s, [External Model]s, [External Circuit]s, [Package]s and IBIS-AMI models.

He noted that IBIS contains several methods to describe corners and to assign and pass parameters. Model makers should minimize parameter passing with corners because of different possible interpretations. EDA tools should be capable of mixing or matching

typ, min and max conditions. He also described how L and C corner values derived from Td and Zo corners can give different “effective” ranges than desired.

**BEST PRACTICES FOR HIGH-SPEED SERIAL LINK SIMULATION**

Minggang Hou (ANSYS, China)

[Presented by Jack Wu (ANSYS, Taiwan)]

Jack Wu presented methods for improving accuracy of serial link simulations. He began by showing how to determine the maximum bandwidth needed in a channel model based on the rise time of the signals into the model. He then emphasized the need for enough low frequency data points in a channel S-parameter model and described how to determine the minimum frequency step needed in the S-parameter model. Jack then described passivity and causality issues with S-parameters. He concluded by saying that S-parameter data integrity is key for good signal integrity simulations.

**CONCLUDING ITEMS**

Michael Mirmak thanked the co-sponsors, presenters and attendees for their participation and support. The meeting adjourned at 4:30 PM.

**NEXT MEETING**

The Asian IBIS Summit in Yokohama will be held November 20, 2014. No teleconferences will be available for the Summit meetings. The next IBIS Open Forum teleconference meeting will be held December 5, 2014.

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**NOTES**

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This meeting was conducted in accordance with ANSI guidance.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:

subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:

subscribe ibis-users <your e-mail address>

Help and other commands:

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ibis-request@eda.org

To join, change, or drop from either or both:

IBIS Open Forum Reflector (ibis@eda.org)

IBIS Users' Group Reflector (ibis-users@eda.org)

State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.eda.org/ibis/bugs/ibischk/>

[http://www.eda.org/ibis/bugs/ibischk/bugform.txt](http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt)

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.eda.org/ibis/tschk_bugs/>

<http://www.eda.org/ibis/tschk_bugs/bugform.txt>

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported

BUGs at:

[http://www.eda.org/ibis/icm\_bugs/](http://www.eda-stds.org/ibis/icm_bugs/)

[http://www.eda.org/ibis/icm\_bugs/icm\_bugform.txt](http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt)

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

[http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt](http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt)

[http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt](http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt)

[http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt](http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt)

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.eda.org/ibis>

Check the IBIS file directory on eda.org for more information on previous discussions and results:

[http://www.eda.org/ibis/directory.html](http://www.eda-stds.org/ibis/directory.html)

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**IBIS – SAE STANDARDS BALLOT VOTING STATUS**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Organization** | **Interest Category** | **Standards Ballot Voting Status** | **October 3, 2014** | **October 24, 2014** | **November 14, 2014** | **November 17, 2014** |
| Altera | Producer | Inactive | - | X | - | - |
| ANSYS | User | Active | - | - | X | X |
| Applied Simulation Technology | User | Inactive | - | - | - | - |
| Cadence Design Systems | User | Active | X | X | X | X |
| Ericsson | Producer | Active | - | - | X | X |
| Huawei Technologies | Producer | Inactive | - | - | X | - |
| Infineon Technologies AG | Producer | Inactive | - | - | - | - |
| Intel Corp. | Producer | Inactive | X | - | - | X |
| IO Methodology | User | Active | X | X | - | X |
| Keysight Technologies (Agilent) | User | Active | X | X | X | - |
| LSI (Avago) | Producer | Inactive | - | - | - | - |
| Maxim Integrated Products | Producer | Inactive | - | - | - | - |
| Mentor Graphics | User | Active | X | X | X | - |
| Micron Technology | Producer | Inactive | X | X | - | - |
| Qualcomm | Producer | Inactive | - | - | - | - |
| Signal Integrity Software  | User | Inactive | X | X | - | - |
| Synopsys | User | Active | X | X | X | - |
| Teraspeed Labs | General Interest | Inactive | X | X | - | - |
| Toshiba | Producer | Inactive | X | - | - | - |
| Xilinx | Producer | Inactive | - | - | - | - |
| ZTE | User | Inactive | - | - | X | - |
| Zuken | User | Inactive | - | - | - | - |

**I/O Buffer Information Specification Committee (IBIS)**

Criteria for Member in good standing:

* Must attend two consecutive meetings to establish voting membership
* Membership dues current
* Must not miss two consecutive Meetings

Interest categories associated with SAE ballot voting are:

* Users - Members that utilize electronic equipment to provide services to an end user.
* Producers - Members that supply electronic equipment.
* General Interest - Members are neither producers nor users. This category includes, but is not limited to, Government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.