

**IBIS Open Forum Minutes**

Meeting Date: **November 13, 2017**

Meeting Location: **Shanghai, China**

**VOTING MEMBERS AND 2017 PARTICIPANTS**

ANSYS Curtis Clark, Toru Watanabe, Baolong Li

Applied Simulation Technology (Fred Balistreri)

Broadcom [Bob Miller], (Cathy Liu)

Cadence Design Systems Brad Brim, Sivaram Chillarige, Debabrata Das

Ambrish Varma, Kumar Keshavan, Ken Willis

Brad Griffin, Aileen Chen\*, Lanbing Chen\*

Guoyu Cui\*, Wei Dai\*, Zhiyu Guo\*, Henry He\*

Jinsong Hu\*, Liang Jiang\*, Skipper Liang\*

Ping Liu\*, Feng Miao\*, Zuli Qin\*, Haisan Wang\*

Hui Wang\*, Yitong Wen\*, Clark Wu\*, Janie Wu\*

Susan Wu\*, Benny Yan\*, Haidong Zhang\*

Alex Zhao\*, Zhangmin Zhong\*

Cisco Systems Lei (Jason) Liu\*, Cassie (Xu) Yan\*

CST Stefan Paret, Matthias Troescher, Burkhard Doliwa

Danilo Di Febo, Alexander Melkozerov

Ericsson Zilwan Mahmod, Guohua Wang\*, Amy X Zhang\*

GLOBALFOUNDRIES Steve Parker

Huawei Technologies Haiping Cao\*, Wei (Richard) Gu\*, Zhenxing Hu\*

Peng Huang\*, Hongxing Jiang\*, Longfang Lv\*

Luya Ma\*, Guangjiang Wang\*, Huichao Weng\*

Zhengrong Xu\*, Hang (Paul) Yan\*, Chen (Jeff) Yu\*

Xiaojun (Steve) Zhou\*, Zhengyi Zhu\*, Huajun Chen\*

Shengli Wang\*, Zen Wei\*

Huawei Technologies (Hisilicon) Fangxu Yang\*

IBM Luis Armenta, Adge Hawes, Greg Edlund

Infineon Technologies AG (Christian Sporrer)

Intel Corporation Michael Mirmak, Hsinho Wu, Eddie Frie

Gianni Signorini, Barry Grquinovic

Masashi Shimanouchi

IO Methodology Lance Wang\*

Keysight Technologies Radek Biernacki, Pegah Alavi, Fangyi Rao

Stephen Slater, Jian Yang, Heidi Barnes

Maxim Integrated Joe Engert, Don Greer, Yan Liang, Hock Seow

Mentor, A Siemens Business Arpad Muranyi, Nitin Bhagwath, Praveen Anmula

(formerly Mentor Graphics) Fadi Deek, Raj Raghuram, Dmitry Smirnov

Bruce Yuan, Carlo Bleu, Chao Jiang\*, David Xu\*

Micron Technology Randy Wolff, Justin Butterfield, Jeff Shiba, Harry Shin

NXP (John Burnett)

Qualcomm Tim Michalka, Kevin Roselle

Raytheon Joseph Aday

SiSoft Mike LaBonte\*, Walter Katz, Todd Westerhoff

Steve Silva

Synopsys Kevin Li, Ted Mido, John Ellis, Scott Wedge

Wonsae Sim, Xuefeng Chen\*, Jinghua Huang\*

Yijiang Huang\*, Deng Shi\*, Yuyang Wang\*

Teraspeed Labs Bob Ross

Xilinx (Raymond Anderson)

ZTE Corporation Rongxing Ban\*, Xinjian Chen\*, Fengling Gao\*

Tao Guo\*, Lili Wei\*, Yangye Yu\*, Shunlin Zhu\*

Zuken Ralf Bruening, Michael Schaeder, Alfonso Gambuzza

**OTHER PARTICIPANTS IN 2017**

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Amphenol Fred Shen\*, Holly Wang\*

ASR Microelectronics Lili Dia\*, Shulong Wu\*

ASUS Nick Huang, Bin-chyi Tseng

Aurora System Murong Lu\*, Jiaxin Sun\*

BasiCAE Kiki Li\*, Darcy Liu\*, July Tao\*, Lisa Wu\*

Brite Semiconductor Haonan Wang\*

Celestica Wilson Chen\*, Sophia Feng\*, Lurker Li\*

Weiqing Liiu\*, Vincent Wen\*

Continental AG Stefanie Schatt

eASIC David Banas

Edadoc Deheng Chen\*, Bruce (Jun) Wu\*, Hong Zhang\*

Extreme Networks Bob Haller

Flextronics Renjun Sun\*

Ghent University Paolo Manfredi

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Ilia State University Nana Dikhaminjia

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KEI Systems Shinichi Maeda

Lattice Semiconductor Maryam Shahbazi, Dinh Tran

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Lenovo Group Shaogao Zheng\*

Lexington Consulting Mike Barg

Missouri Science and Technology Giorgi Maghlakelidze

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SAE-ITC (Thomas Munns), Jose Godoy

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SMICS Sheral (Xuejiao) Qi\*

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Spreadtrum Communications Junyong Deng\*, Ganyue Wang\*, Shiqing Si\*

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TopBrain Ye Li\*

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Yi Chuan Technology Wei Ming Lu\*

Zhaoxin Liam Li\*, Eddrick Wang\*

Zhejiang Uniview Technologies Busen Cai\*, Jilun Fang\*

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

**UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

Date Meeting Number Meeting Password

November 15, 2017 Taipei IBIS Summit – no teleconference

November 17, 2017 Tokyo IBIS Summit – no teleconference

December 1, 2017 624 999 876 IBISfriday11

For teleconference dial-in information, use the password at the following website:

<http://tinyurl.com/zeulerr>

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

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**OFFICIAL OPENING**

The Asian IBIS Summit took place on Monday, November 13, 2017 at the Parkyard Hotel in Shanghai. About 107 people representing 33 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

<http://www.ibis.org/summits/nov17a/>

Hang (Paul) Yan of Huawei welcomed the participants to the 13th annual Asian IBIS Summit (China).

Mike LaBonte welcomed participants on behalf of the IBIS Open Forum and convened the meeting.

Mike continued by thanking all the co-sponsors. The primary sponsor was Huawei Technologies, and the co-sponsors were Cadence Design Systems, IO Methodology, Mentor, a Siemens Business, MostecEDA (SPISim), Synopsys, Teledyne LeCroy, and ZTE Corporation.

**IBIS UPDATE**

Mike LaBonte (SiSoft, USA)

Mike LaBonte detailed the activities of the IBIS Open Forum over the past year. He showed a possible timeline for the passage of IBIS 7.0, as well as the status of all current BIRDs that may or may not be part of IBIS 7.0. Mike gave a brief summary of the changes in three BIRDs likely to become part of IBIS 7.0.

**IBIS INTERCONNECT MODELING USING IBIS-ISS AND TOUCHSTONE**

Michael Mirmak (Intel Corporation, USA)

[Presented by Mike LaBonte (SiSoft, USA)]

Mike LaBonte presented on behalf of Michael Mirmak. The concepts found in BIRD189.x were summarized. The new format is an improvement over existing IBIS [Define Package Model] in several ways, allowing for both cascaded model sections as well as coupling in any combination. The Touchstone format and the ability to separately model buffer to pad and pad to pin connections would be helpful for the high speed signals used today. The addition of die pads for rails allowed for circuit topologies suitable for modeling the power and ground rails in chips.

**SIGNAL INTEGRITY ANALYSIS FOR 56G-PAM4 CHANNEL OF 400G SWITCH**

Sophia Feng, Vincent Wen (Celectica, PRC)

[Presented by Sophia Feng (Celectica, PRC)]

Sophia Feng noted that switch bandwidth is moving from 100G to 400G, with data rates moving from 25G NRZ SerDes to 56G PAM4 SerDes. She showed simulation results from analyses of a 200GBASE-KR4, a 400GAUI-8 CSM/200GBASE-CR4, and a CEI-56G-VSR-PAM4 channel.

**THINK PAM4 SERDES**

Xiaojun Zhou (Huawei Technologies, PRC)

Xiaojun Zhou introduced the PAM4 SerDes architecture and described equalization options including CTLE, FFE, and DFE. More receivers are changing from analog to digital architectures to leverage DSP technology. The presentation illustrated the need for a more general PAM4 simulator to support digital RX equalization. The current IBIS-AMI specification is suited for analog based RX, but it lacks support for the digital architectures.

A participant stated that on page 19, it is noted the IBIS-AMI API doesn't work for digital equalization. Is there any other method for analysis for digital equalization? Xiaojun answered that they are only using measurement for now.

**COMPARISON OF TIME DOMAIN AND STATISTICAL IBIS-AMI ANALYSES**

Mike LaBonte (SiSoft, USA)

Mike LaBonte noted that a dual IBIS-AMI model has an AMI file with GetWave\_Exists set to true and Init\_Returns\_Impulse set to true. This is the best option for running both time domain and statistical analysis. Mike reviewed some fundamentals of channel simulation including inputs and outputs of time-domain and statistical simulations, channel impairments, step response and pulse response analysis, eye height prediction from pulse response cursor analysis, and methods for all the ISI in a given channel. He then discussed jitter and noise impairments and equalization methods. He concluded that IBIS-AMI time domain simulation with AMI\_GetWave can model non-linear effects such as DFE and saturation, but it can be impossible to simulate enough bits to prove the low BER requirements of some technologies. IBIS-AMI statistical simulation can quickly evaluate low BER, but it cannot see time-variant effects such as DFE and saturation. So, dual IBIS-AMI models are required.

**A WAY TO EVALUATE POST-FEC BER BASED ON IBIS-AMI MODEL**

Yanye Yu, Tao Guo, Shunlin Zhu (ZTE Corporation, PRC)

[Presented by Yanye Yu (ZTE Corporation, PRC)]

Yanye Yu noted that Forward Error Correction (FEC) is being used in SerDes systems to increase serial link system budgets and relax BER requirements. FEC is found in 100GE/400GE/800GE specifications. FEC is a forced function in 400GE and 800GE systems, but there is no FEC function model in IBIS-AMI yet. Yanye proposed a solution to evaluate the post-FEC BER using an FEC model. Yanye described details of the model based on error propagation theory and showed results of a simulation using the model.

**CHARACTERIZING AND MODELING OF A LINEAR CTE**

Skipper Liang (Cadence Design Systems, ROC)

Skipper Liang noted that when creating an IBIS-AMI model for an RX, it is necessary to divide the buffer between the analog part and the algorithmic part. He showed a method in which modelers no longer need to model the RX IBIS (analog part) model. A dummy IBIS model is used, and the buffer characteristics are put in the AMI model. The CTE is modeled using a step response time domain characterization. The method is only valid when the equalizer is purely linear.

**USING DATA FILES FOR IBIS-AMI MODELS**

Lance Wang (IO Methodology, USA)

Lance Wang noted that creating IBIS-AMI models can require making executables for many platforms and OS’s. He presented the concept of creating a single DLL/SO file that references external data files, allowing reuse of code for different transceivers by only modifying the data file. If using data files, the DLL/SO contains AMI standard functions, data processing functions and data file processing functions that might include decryption of the data file. The data file can contain code, data, parameters, and it could be encrypted. With this approach, the DLL/SO file could be developed by professional programmers and used for many different data files. The data file can then be created by designers or modelers and would not require compilation. A test case was shown that pointed to the data file through a Model\_Specific parameter.

**IBIS-AMI MODELING USING SCRIPTS AND SPICE MODELS**

Wei-hsing Huang (SPISim, USA)

Wei-hsing Huang investigated the creation of IBIS-AMI models using scripting languages and existing SPICE models. The flow could reduce AMI modeling time and serve as an intermediate step towards full C/C++ implementation. Considerations include performance and the redistribution and use of models that could rely on an external SPICE simulator.

A question was asked: “For the GetWave function, when you use the on-the-fly method to simulate the SPICE circuit to get the modified waveform, will it be very slow also?” Wei-hsing responded that it will be slower than an algorithm-based GetWave function. But, since it is using a high impedance load for the SPICE circuit, it will be a lot faster than just using the SPICE circuit for simulations.

**LEVERAGING IBIS CAPABILITIES FOR MULTI-GIGABIT INTERFACES**

Ken Willis (Cadence Design Systems, USA)

[Presented by Zuli Qin (Cadence Design Systems, PRC)]

Zuli Qin noted that the presentation related to the EDI CON paper “Signal Integrity Methodology for Double-Digit Multi-Gigabit Interfaces”. Use of Spice [External Model]s makes it easy to write simple parameterized Spice subcircuits for I/O buffers when IBIS availability does not align with a project schedule. The EDA tool user can select parameter values from a GUI using the [External Model] “Parameters” and “Converter\_Parameters” syntax.

Zuli described the typical modules of an Rx AMI model including gain, CTLE and DFE. These modules typically adapt at different rates, and the initial modules like gain and CTLE usually adapt more slowly than the DFE. Zuli showed how adjusting the adaptation algorithms of the AMI model led to better adaptation and a significant difference in final eye height. Zuli showed details of the backchannel flow from BIRD147. Zuli went on to show the application of IBIS-AMI modeling and simulation techniques to DDR4/5. Cadence developed an IBIS-AMI model for a DDR4 controller that included equalization. Zuli showed correlation between an IBIS-AMI model-based channel simulation and a transistor-level circuit simulation.

**CLOSING REMARKS**

Mike LaBonte thanked the co-sponsors, presenters and attendees for their participation and support.

**NEXT MEETING**

The next IBIS Open Forum teleconference meeting will be held December 1, 2017. The following IBIS Open Forum teleconference meeting is tentatively scheduled on December 15, 2017.

The Asian IBIS Summit in Taipei will be held November 15, 2017. The Asian IBIS Summit in Tokyo will be held November 17, 2017. No teleconferences will be available for the Summit meetings.

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**NOTES**

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to [info@ibis.org](mailto:info@ibis.org). Examples of inquiries are:

* To obtain general information about IBIS.
* To ask specific questions for individual response.
* To subscribe to the official [ibis@freelists.org](mailto:ibis@freelists.org) and/or [ibis-users@freelists.org](mailto:ibis-users@freelists.org) email lists (formerly [ibis@eda.org](mailto:ibis@eda.org) and [ibis-users@eda.org](mailto:ibis-users@eda.org)).
* To subscribe to one of the task group email lists: [ibis-macro@freelists.org](mailto:ibis-macro@freelists.org), [ibis-interconn@freelists.org](mailto:ibis-interconn@freelists.org), or [ibis-quality@freelists.org](mailto:ibis-quality@freelists.org).
* To inquire about joining the IBIS Open Forum as a voting Member.
* To purchase a license for the IBIS parser source code.
* To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

<http://www.ibis.org/bugs/ibischk/>   
[http://www.ibis.org/ bugs/ibischk/bugform.txt](http://www.ibis.org/%20bugs/ibischk/bugform.txt)

The BUG Report Form for tschk2 resides along with reported BUGs at:

<http://www.ibis.org/bugs/tschk/>   
<http://www.ibis.org/bugs/tschk/bugform.txt>

The BUG Report Form for icmchk resides along with reported BUGs at:

<http://www.ibis.org/bugs/icmchk/>   
<http://www.ibis.org/bugs/icmchk/icm_bugform.txt>

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

<http://www.ibis.org/bugs/s2ibis/bugs2i.txt>   
<http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt>   
<http://www.ibis.org/bugs/s2iplt/bugsplt.txt>

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

<http://www.ibis.org/>

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

<http://www.ibis.org/directory.html>

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**SAE STANDARDS BALLOT VOTING STATUS**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Organization** | **Interest Category** | **Standards Ballot Voting Status** | **October 6, 2017** | **October 18, 2017** | **October 27, 2017** | **November 13, 2017** |
| ANSYS | User | Active | X | X | X | - |
| Applied Simulation Technology | User | Inactive | - | - | - | - |
| Broadcom Ltd. | Producer | Inactive | X | - | - | - |
| Cadence Design Systems | User | Inactive | X | - | - | X |
| Cisco Systems | User | Inactive | - | - | - | X |
| CST | User | Inactive | X | - | - | - |
| Ericsson | Producer | Inactive | - | - | - | X |
| GLOBALFOUNDRIES | Producer | Inactive | X | - | X | - |
| Huawei Technologies | Producer | Inactive | - | - | - | X |
| IBM | Producer | Inactive | X | - | - | - |
| Infineon Technologies AG | Producer | Inactive | X | - | X | - |
| Intel Corp. | Producer | Active | X | X | X | - |
| IO Methodology | User | Active | X | - | X | X |
| Keysight Technologies | User | Active | X | X | X | - |
| Maxim Integrated | Producer | Inactive | - | - | - | - |
| Mentor, A Siemens Business | User | Active | X | X | X | X |
| Micron Technology | Producer | Active | X | - | X | - |
| NXP | Producer | Inactive | X | - | - | - |
| Qualcomm | Producer | Inactive | - | X | - | - |
| Raytheon | User | Inactive | X | - | - | - |
| SiSoft | User | Active | X | - | X | X |
| Synopsys | User | Active | X | X | X | X |
| Teraspeed Labs | General Interest | Active | X | X | X | - |
| Xilinx | Producer | Inactive | X | - | - | - |
| ZTE Corp. | User | Inactive | - | - | - | X |
| Zuken | User | Inactive | X | - | - | - |

Criteria for SAE member in good standing:

* Must attend two consecutive meetings to establish voting membership
* Membership dues current
* Must not miss two consecutive meetings

Interest categories associated with SAE standards ballot voting are:

* Users - members that utilize electronic equipment to provide services to an end user.
* Producers - members that supply electronic equipment.
* General Interest - members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.