

Meeting Date: November 1, 2019 Meeting Location: Shanghai, China

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Yuyang Wang*, Jinhua Huang*

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In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date Meeting Number Meeting Password

November 4, 2019 Asian IBIS Summit (Taipei) – no teleconference November 8, 2019 Asian IBIS Summit (Tokyo) – no teleconference November 22, 2019 624 227 121 IBISfriday11

For teleconference dial-in information, use the password at the following website:

http://tinyurl.com/IBISfriday

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The Asian IBIS Summit took place on Friday, November 1, 2019 at the Parkyard Hotel in Shanghai. About 82 people representing 25 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis.org/summits/nov19a/

Randy Wolff opened the summit by welcoming everyone and thanking primary sponsor Huawei Technologies. He invited Paul Han of Huawei to give a welcome address, which was followed by Randy's welcome address. Each emphasized the importance of IBIS to the industry. Randy also thanked sponsors ANSYS, Cadence Design Systems, Keysight Technologies, Synopsys, and ZTE Corporation. He noted that minutes of the meeting would be posted. There would be two breaks for refreshments and vendor interaction, and free lunch. The Summit would be followed by a vendor presentation session led by Lance Wang of Zuken as moderator.

IBIS CHAIR'S REPORT

Randy Wolff (Micron Technology, USA)

Randy described the status and activities of the IBIS Open Forum. There are 26 member companies of IBIS in 2019. The 2019-2020 officers have changed significantly from the previous year. Many IBIS meetings occur weekly to yearly from task groups to Summits around the world. SAE ITC is the parent organization of IBIS, providing financial and legal services. IBIS has four task groups meeting weekly to discuss technical topics, IBIS quality, and the Editorial task group, which meets only as needed to produce new IBIS specification documents. The latest IBIS milestone is the release of IBIS 7.0 and the ibishchk7 parser to support it.

Beyond IBIS 7.0, there are currently five BIRDs in discussion. The interconnect task group is working on an important update to EBD to support IBIS-ISS and Touchstone models. BIRD200 is already approved, and it improves die capacitance modeling. BIRD195.1 is also approved, and it simplifies some AMI input models.

Randy encouraged new contributions to IBIS from the meeting participants to ensure that IBIS continues to meet the needs of new technology, including improving power delivery design. He also described the BIRD process, and he noted that ideas do not need to be written in formal BIRD templates, but first can be presented in task groups for discussion before a BIRD is proposed.

HOW TO OBTAIN BUFFER IMPEDANCE FROM IBIS

Lance Wang (Zuken, USA)

Lance explained that matching output buffer impedance to interconnect impedance is a necessary task for the SI engineer. Impedance is represented as a complex quantity Z. He showed how to measure input and output impedance of an I/O buffer. Example I-V curves for input and output buffers were shown, including inputs with ODT. Obtaining impedance from an IBIS model starts with overlaying a load line on the Pullup or Pulldown I-V curves. Operating point impedance is the intersection of the load line and the I-V curve. I/O impedance may vary for different loads.

C-PHY SI SIMULATION WITH IBIS MODEL

Bailing Zhang (ANSYS, PRC)

Bailing gave an overview of the C-PHY interface, which provides high throughput performance over bandwidth limited channels for connecting to peripherals, including displays and cameras. C-PHY uses a group of three conductors rather than conventional pairs. The group of three wires is called a lane. Multiple bits are encoded into each symbol epoch, and the data rate is ~2.28x the symbol rate. The signal is received using a group of three differential receivers. The C-PHY interface can co-exist on the same pins/pads as the D-PHY interface signals. Using IBIS model in EDA software to do the C-PHY SI simulation is very convenient, accurate and fast.

A comment was made that we know the stimulus coding could impact the eye opening. It was asked what code sequence was used in the simulations. Bailing responded that they used some specific code sequence for these simulations. For these code sequences, the eye is opened for the signals.

INNOVATIONS IN DDR MEMORY SIMULATION

Stephen Slater (Keysight Technologies, USA) [Presented by Jiajie Zhao (Keysight Technologies, PRC)]

Jiajie defined the measure of success for a DDR5 design, as no system failures under stress testing with satisfactory product quality risk. Ensuring success with DDR5 requires complicated methodology. Challenges for DDR5 include managing crosstalk and jitter and using BER specifications. Closed eyes need equalization and training. Innovations are required in LPDR5 and DDR5 modeling and simulations. The signal return path design becomes very important for reducing crosstalk.

Key insights are that jitter and crosstalk are very significant. Simulation must predict eye closure due to random jitter down to the system BER (1e-16) in a practical time. EM simulation must capture crosstalk accurately.

DDR5 and LPDDR5 are the first DRAM technologies to include DFE in the receiver. DDR5 Rx specifications are inside the die, so virtual probing inside the die is needed. DDR5 Rx testing now includes a loopback test feature. Skew adjustment is also performed with Write-leveling by the controller.

IBIS-AMI has been widely adopted by IC, system and EDA companies for SerDes signals, but this is the first application to DDR single-ended signals. IBIS-AMI flows for DDR5 must be able to support passing the DC common mode voltage to the Rx model, modeling of asymmetric eyes due to driver rise/fall mismatch, and inclusion of external clocking to track uncorrelated jitter between DQ and DQS. A backchannel interface for training could also be an improvement.

One person asked about the PDN. Jiajie noted that for now, they must work on PDN separately.

IBIS-AMI AND COM CO-DESIGN FOR 25G SERDES

Nan Hou*, Amy Zhang*, Guohua Wang*, David Zhang**, Anders Ekholm** (Ericsson, *PRC, **Sweden)

[Presented by Nan Hou (Ericsson, PRC)]

Nan started with an overview of the IBIS-AMI flow. Channel operating margin (COM) is related to the ratio of a calculated signal amplitude to a calculated noise amplitude. She described the COM flow, the channel transfer function, and the method for determining the optimal EQ settings. She noted that the channel transfer function combines frequency domain calculations with a time domain calculation to include DFE.

Two cases were shown of simulating COM results, followed by IBIS-AMI simulation with the recommended COM parameter settings. She stressed that COM is only useful for optimizing signal to noise ratio, if other types of optimization are needed, then other methods must be used. In a co-design simulation flow, COM is used for channel optimization followed by IBIS-AMI simulation.

HOW TO FIX A SHORT CHANNEL PROBLEM WITH AMI AND COM SIMULATION

Dongdong Ye, Shunlin Zhu (ZTE Corporation, PRC) [Presented by Dongdong Ye (ZTE Corporation, PRC)]

Dongdong tested four CEI-56G-LR-PAM4 channels. The backplane trace length was varied between 1-4 inches. With the increase of channel length, the parameters that meet the requirements of BER increase, and the system margin increases as well. For IBIS-AMI and COM simulation, 16 channels were simulated. The first AMI results were inconsistent with the trend of actual test results while the COM results were consistent. It was suspected that the differences were caused by the connector. With the connector removed, the AMI results trend was similar to the COM results. It was shown that COM simulation could provide more information compared to AMI simulation. The COM simulation tool supports exporting the insertion loss curve after CTLE. When the channel insertion loss is very small, CTLE compensates too much for the insertion loss at low frequency band, which is not conducive to reducing ISI. During AMI simulation, it will be more helpful to find the problem if more detailed information can be output (such as the CTLE curve). When analyzing problems, it is recommended that both COM and AMI simulation should be done if possible.

A comment was made that in your case, AMI and COM simulations do not agree each other. Do you know the reason? Dongdong noted that COM simulations used the reference models. IBIS-AMI should be more detailed. That is why they might not agree with each other.

CELESTICA 112G SI CHANNEL STUDY FOR 800G SWITCH

Bowen Shi, Sophia Feng (Celestica, PRC) Presented by Bowen Shi (Celestica, PRC)

Bowen showed details of modeling an 802.3ck C2M host channel including a host board, connector, and host compliance board. COM simulation was done for a 100G-CR channel. 5 aggressor FEXT channels and 3 aggressor NEXT channels on both sides of the victim channel

were considered for the COM crosstalk analysis. 24 taps of fixed DFE were used in the COM simulation. Since the COM configuration is not finalized, it is currently difficult to pass the COM 3dB margin. The PCB still can be an option for a 112G switch, but the SI performance of the PCB needs to be improved. The host channel trace length is only 6 inches, so it is difficult to improve the insertion loss performance to get better COM margin, so it has a higher expectation on crosstalk to improve the SNR (BER).

CHANNEL SIMULATION OVER DDR4/5 AND ABOVE

Kumar Keshavan*, Ambrish Varma*, Ken Willis*, Skipper Liang** (Cadence Design Systems, *USA, **ROC)

Presented by Skipper Liang (Cadence Design Systems, ROC)

Skipper noted that as the transmission rate of a memory bus goes beyond 5Gbps, besides the well-known timing and overshoot/undershoot analysis, it requires BER prediction analysis and channel analysis. Two additional concerns we need to face while using a channel engine to deal with a memory bus include asymmetric rising/falling edges and strobes as a timing reference.

As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, we encounter IBIS I/O models with asymmetric rising and falling edges. This is different from the highly symmetric drivers we typically encounter with serial link analysis. Traditional single-step response methods for impulse response generation may not reproduce circuit simulation results accurately enough. An EDA tool can handle this without changes to the IBIS specification. Characterization methods using rising and falling edges captured the rising/falling asymmetry behavior very well for channel simulation.

As channel simulation and IBIS-AMI modeling methods are adapted from serial link to DDR interface analysis, serial link CDR algorithms are often used for analysis. Using a default CDR instead of the actual strobe to get clock ticks will miss important impairments/jitter for a parallel bus topology. Analysis results show false optimism using the CDR approach as compared to a true strobe timing methodology. It is necessary to model delay accurately between data and strobe.

A comment was made that you mention your channel simulation can handle the PDN simulation as well. How does your PDN simulation result compare with the real measurements? Skipper replied that our PDN analysis is basically for the worst-case scenario.

OPEN DISCUSSION

One person asked about potential advances to IBIS in the area of power delivery modeling. Randy Wolff commented that IBIS models that include power-aware information are useful for SSO simulation. There is still room to improve the modeling of power supply induced jitter (PSIJ) that affects the timing of the output buffer. Power delivery effects are also not integrated with the IBIS-AMI flows, and this is an issue to address for DDR5 and other new IBIS-AMI flows. Chip core power is also not addressed by IBIS.

Kevin Li of Synopsys asked about the ability to form a technical discussion group similar to the

ATM task group for IBIS participants in Asia. He commented that the meeting time for ATM meetings is not good for people in Asia. Randy responded that he would support formation of a group like this. He would need someone to chair the group to schedule and lead meetings and provide reports to the IBIS Open Forum.

CLOSING REMARKS

Randy Wolff closed the Summit, thanking the sponsors, the authors and presenters, and all participants. He encouraged participation from Asia in IBIS and for all to consider proposing their ideas for IBIS through the BIRD process. The summit was adjourned.

NEXT MEETING

The next IBIS Open Forum teleconference meeting will be held on November 22, 2019. The following IBIS Open Forum teleconference meeting is tentatively scheduled on December 13, 2019.

The Asian IBIS Summit in Taipei will be held November 4, 2019. The Asian IBIS Summit in Tokyo will be held November 8, 2019. No teleconference will be available for the Summit meetings.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

All inquiries may be sent to info@ibis.org. Examples of inquiries are:

- To obtain general information about IBIS.
- To ask specific questions for individual response.
- To subscribe to the official ibis@freelists.org and/or ibis-users@freelists.org email lists (formerly ibis@eda.org and ibis-users@eda.org).
- To subscribe to one of the task group email lists: ibis-macro@freelists.org, ibis-macro@freelists.org, ibis-macro@freelists.org, ibis-macro@freelists.org, ibis-ibis-macro@freelists.org, <a href="ma
- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/ http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/ http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/ http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	September 6, 2019	September 27, 2019	October 18, 2019	November 1, 2019
ANSYS	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	_
Broadcom Ltd.	Producer	Inactive	_	_	_	_
Cadence Design Systems	User	Inactive	X	_	_	X
Cisco Systems	User	Inactive	-	_	_	X
Dassault Systemes	User	Inactive	_	-	_	-
Ericsson	Producer	Inactive	_	-	_	X
GLOBALFOUNDRIES	Producer	Active	X	-	X	_
Google	User	Inactive	X	X	-	_
Huawei Technologies	Producer	Inactive	-	-	-	X
Infineon Technologies AG	Producer	Inactive	Х	Х	_	_
Instituto de Telecomunicações	User	Inactive	-	-	_	-
IBM	Producer	Active	X	X	X	-
Intel Corp.	Producer	Active	X	X	X	X
Keysight Technologies	User	Active	X	X	-	X
Maxim Integrated	Producer	Inactive	-	-	-	-
Mentor, A Siemens Business	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	X
NXP	Producer	Inactive	-	-	-	-
SiSoft	User	Active	X	X	X	-
SPISim	User	Active	X	X	X	-
Synopsys	User	Active	X	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	-
Xilinx	Producer	Inactive	-	-	=	
ZTE Corp.	User	Inactive	-	-	=	X
Zuken	User	Active	X	X	X	X

Criteria for SAE member in good standing:

- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings

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- Users members that utilize electronic equipment to provide services to an end user.
- Producers members that supply electronic equipment.
- General Interest members are neither producers nor users. This category includes, but is not limited to, government, regulatory agencies (state and federal), researchers, other organizations and associations, and/or consumers.