IBIS Open Forum Minutes

Meeting Date: April 8, 2022
Meeting Location: On-site and Virtual IBIS Summit After DesignCon 2022

VOTING MEMBERS AND 2022 PARTICIPANTS

Analog Devices (Maxim Integrated)	Tushar Pandey, Jermaine Lim
ANSYS	Curtis Clark*
Applied Simulation Technology	(Fred Balistreri)
Broadcom	(Yunong Gan)
Cadence Design Systems	Zhen Mu, Jared James*, Ken Willis*
Celestica	(Sophia Feng)
Cisco Systems	(Stephen Scearce)
Dassault Systemes	(Stefan Paret)
Ericsson	(Guohua Wang)
Google	(Hanfeng Wang)
Huawei Technologies	(Hang (Paul) Yan)
Infineon Technologies AG	(Christian Sporrer)
Instituto de Telecomunicações	(Abdelgader Abdalla)
Intel Corporation	Hsinho Wu*, Michael Mirmak*, Jingbo Li*, Liwei Zhao*
Keysight Technologies	Radek Biernacki*, Ming Yan*, Fangyi Rao*, Majid Ahadi Dolotsara*, Pegah Alavi*, Saish Sawant*
Luminous Computing	(David Banas)
Marvell	Steven Parker
MathWorks	Mike LaBonte*, Walter Katz*
Micron Technology	Randy Wolff*, Aniello Viscardi*, Justin Butterfield*
MST EMC Lab	(Chulsoon Hwang)
SerDesDesign.com	(John Baprawski*)
Siemens EDA	Arpad Muranyi*, Weston Beal*, Amin Maher*, Scott Wedge*, Steve Kaufer*, Todd Westerhoff*, Vladimir Dmitriev-Zdorov*
STMicroelectronics	(Olivier Bayet)
Synopsys	Ted Mido*
Teraspeed Labs	Bob Ross*
Xilinx	(Bassam Mansour)
Waymo	Zhiping Yang
ZTE Corporation	(Shunlin Zhu)
Zuken	(Michael Schäder)
Zuken USA	Lance Wang*

OTHER PARTICIPANTS IN 2022

Amazon Lab126	Ashkar Hashemi*
Ciena	Hugues Tournier*
IBM	Greg Edlund*
Mercury Systems	Vincent Tam*
National Central University, Taiwan	Chiu-Chih Chou*
OVT	Sirius Tsang*
SAE ITC	José Godoy*

Serial Link Systems	Aleksey Tyshchenko*, David Halupka*
University of Colorado, Boulder, ECEE	Eric Bogatin*
University of Illinois	José Schutt-Aine*

In the list above, attendees at the meeting are indicated by *. Those submitting an email ballot for their member organization for a scheduled vote are indicated by ^. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The connection information for future IBIS teleconferences is as follows:

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All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting.

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The On-site and Virtual IBIS Summit After DesignCon 2022 took place on Friday, April 8, 2022, as a hybrid meeting. About 40 people representing 21 organizations attended. The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

https://ibis.org/summits/apr22/

Start times and durations listed in these minutes refer to the meeting recording linked at:

https://ibis.org/summits/apr22/summit_recording.mp4

Randy Wolff opened the summit by welcoming everyone and thanking them for joining, noting that it was good to see people face-to-face. He said it was the first hybrid IBIS summit, a practice that might be continued in the future. Randy thanked the sponsors Cadence Design

Systems, Keysight Technologies, Siemens EDA, and Synopsys, saying that sponsorship supported the in-person meeting logistics.

IBIS CHAIR'S REPORT
Randy Wolff (Micron Technology, USA)
(Start 00:01:55, Duration 18:30)

Randy Wolff gave an overview of the structure and activities of the IBIS Open Forum. He invited people to consider serving in officer roles, thanking the current officers. Randy described each BIRD under consideration for IBIS 7.2. The future additions to IBIS might involve DDR5 training, power aware improvements, and serdes operating at 112Gbps and beyond, for example. A Touchstone 3.0 specification was under consideration, possibly with pole-residue format and port naming. Randy said anyone could join a task group to participate or subscribe to relevant IBIS email lists. He showed the IBIS web page, pointing out useful links.

FITTED POLES/RESIDUES: FILE FORMAT, TRANSFORMATIONS, LIMITATIONS
Vladimir Dmitriev-Zdorov (Siemens EDA, USA)
(Start 00:21:00, Duration 41:00)

Vladimir Dmitriev-Zdorov describe a method and format for fitting a poles and residues model to an analog system. Careful steps were required to create an accurate response. In particular, the sampling interval mattered. Expressing as rational functions allow for time domain simulation by convolution. Recursive convolution was a simulation method that worked efficiently. The arrangement of poles in pole-residue representation must be correct and stable. "Realness" required all complex pole-residues to be in complex-conjugate pairs. The representation format could help enforce that. In the proposed format, a very high frequency value represented infinity, but there may be a better way to represent that. It helped to have a common set of poles that span all matrix components. Temporarily separating out delay had benefits during solution, since not all components of the model had the same delay. The result was better accuracy, fewer poles, and smaller file size. Performance was much better than equivalent circuit simulations.

A standardized pole-residue model definition format was needed. The PLS format was proposed, which Vladimir reviewed. It was an existing format, and some possible changes were described. PLS models could be transformed to other formats, but there could be complications.

CIRCUIT SYNTHESIS OF MULTIPORT NETWORKS FROM PASSIVE POLES AND RESIDUES
Chiu-Chih Chou*, Jose Schutt-Aine**
(National Central University, ROC*; University of Illinois, USA**)
[Presented by Chiu-Chih Chou*, Jose Schutt-Aine**]
(Start 01:03:20, Duration 43:00)

José Schutt-Aine said model order reduction reduced the number of ports in a multi-port model, reducing computation time. Passivity enforcement was required, and that could be accomplished by residue perturbation. Additional steps were required to make SPICE implement recursive convolution. A vector fitting method was found to do that without changing the SPICE software. Complex poles required careful fitting to an equivalent subcircuit. The approach was compared to direct convolution.

Chiu-Chih George Chou described 6 topologies used for circuit synthesis from models in pole-residue format. This was evaluated with and without using poles common across components. A PI networks could be used for Y matrices and no controlled sources would be required, but there may be negative element values. It was possible to apply that approach to S-parameters by adding controlled sources. A state-space model approach utilized an RC circuit with controlled sources for the input, state, and output equations. The state space model also could be converted to a PI model. It was necessary to choose between Single-In-Single-Out (SISO) or Multiple-In Multiple-Out (MIMO) approaches. Directly using pole-residue format would involve a Foster G element. George showed a table comparing the 6 approaches. The sixth approach would not be supported by all simulators due to the Foster G element requirement, but it was fastest.

Walter Katz asked about the difference between pole-residue and pole-zero formats. Vladimir Dmitriev-Zdorov said we needed a sum, not a ratio. He felt residues were more convenient.

Bob Ross said there was a limitation in vector fitting for duplicate poles, asking if that could be extended for multiple poles. Vladimir said criticality was the question. He said it was impossible to get two poles at the same frequency. José said if the problem came up a solution could be to extract again with a different order. He had not seen any trouble with duplicate poles.

Arpad asked about the size of the model files José was working with. Jose said he had not taken steps to optimize size, he was collecting element values to use in the assembled SPICE circuits. George said order was the key factor, and the size would be smaller using the sixth model. Randy Wolff asked if there were example models for people to look at. José said they had public examples.

TIME-DOMAIN EXTRACTION AND SPICE MACROMODELING
Bob Ross (Teraspeed Labs, USA)
(Start 02:00:15, Duration 42:10)

Bob Ross showed several mathematical representations of time domain measurements, among which transformations were possible. For difference equations a natural log representation could be used. A recursive Taylor series method was used for time step calculations of higher order terms. Examples of step and impulse response fittings were shown. That method resulted in Laplace transform polynomial ratios.

Bob said SPICE macro models also could be produced, starting with the results of the previous method. He said SPICE was a lowest common denominator format between tools, where no other common format existed. He reviewed the characteristics or different types of macromodel implementations. A feedback network could be used to characterize operational amplifiers, and the open loop response could be determined from the closed loop response. The arrangement of poles and zeros would inform the choice of model order to use. The circuit could be reduced using cancellations.

Arpad Muranyi asked if the macro models were SPICE. Bob said they were.

Arpad asked how much time was needed to produce the models. Bob said there were 8 termination types, constraints, and other factors that took quite a while.

Arpad asked Bob to compare his method to that from the previous presentation. Bob said José had used vector fitting, but he was not sure of any differences in limitations and realizability. He said there were some similarities, however.

PORT NAMING ENHANCEMENT FOR TOUCHSTONE FILES
Walter Katz (MathWorks, USA)
(Start 02:43:00, Duration 30:15)

Walter Katz showed an example S-parameter model, noting that it was not known which physical attachment each port was associated with. He listed proposed requirements for a new Touchstone format that would have that information. An IEEE document showed an example of what that might look like. Walter posed some optional features that might also be supported. One question was whether both physical and logical names should be supported. Walter showed a proposal currently being discussed by the IBIS Interconnect Task Group.

Fangyi Rao asked how the physical name would be found. Walter said the name of the pin was the physical name. In the example there was a controller and two memories. Randy Wolff said proposed table format was like IBIS, but the hope was that it could serve uses other than IBIS. Arpad Muranyi said the data was often generated by an extraction tool from layout. He felt that the tools should not have to rewrite their algorithms for the new format. Walter agreed, saying all that was needed was a format to map into those tools.

Aleksey Tyshchenko said a connector could be used in multiple places, and it would not always have the same connections. Walter said the logical names might be meaningless, but the physical pins for the connector would be given, and those would always be the same. He noted that pin numbers on the two sides of a connector would usually be the same, but not always.

Michael Mirmak said we were trying to strike a balance. Some wanted to quantify two-sided passive networks, but also there could be systems with multiple cascaded Touchstone files of differing dimensions. He said some people called for keeping Touchstone data only, and adding a wrapper file around it, but it was easy to lose track when multiple files had to be used together. Walter drew a parallel to using AMI and Verilog models together, agreeing with Michael that having linkage information inside files rather than in an outside wrapper would help get it right.

Randy said the reference designator portion of the physical name was not needed or not known for a model provided for a connector by the vendor. Walter said there could be design-specific and non-specific Touchstone files. Arpad felt the two scenarios needed to be addressed by the new proposal.

Michael asked if there was an easy way to look at the [Begin Port Data] keyword as being overloaded. He gave [Temperature] as an example of an IBIS keyword that was about how data was collected, which was different from how it would be applied. The "end" column was about orientation and should be invariant, whereas the "Phy-name" column was about how the data was collected. He suggested separating the two categories. Walter gave another example involving connectors in a car. He said "near end" and "far end" had to be used carefully because that was defined only in the context of where used.

Ken Willis said S-parameter ports could represent a group of power and ground pins. Walter said those could be a single port and deciding the physical name could be a problem. He said several pins could belong to a reference port, noting that Siemens had a format giving a list of pins in the reference port section. Ken said it would help to have the information about the reference pins. Walter agreed.

IBIS-AMI MODELING AND CORRELATION METHODOLOGY FOR ADC-BASED SERDES BEYOND 100 GB/S
Aleksey Tyshchenko*#, Clinton Walker**##, David Halupka*#, Richard Allred***##, Tripp Worrell***##, Barry Katz***##, Adrien Auge**#

(SeriaLink Systems*, Alphawave IP**, MathWorks***; Canada#, USA##)
[Presented by Aleksey Tyshchenko (SeriaLink Systems, Canada)]
(Start 03:14:10, Duration 42:50)

Aleksey Tyshchenko said IBIS-AMI was analog centric, creating challenges for modeling Analog to Digital Converter ADC-based serdes. He said there was no waveform at the decision point. A minimum SNR was needed to achieve a maximum BER. Channel Operating Margin (COM) analysis could be used to assess that. He showed a parametric TX model that could be modeled by COM. He showed an RX model that produced an approximated output waveform. Non-linearity could be handled different ways. Adaptation could be modeled using statistical analysis. Noise was a factor and needed to be modeled by injecting noise into the RX CTLE. That would need to be estimated into the impulse response for statistical analysis. A technique was shown to get RMS noise. A block inside the RX model measured SNR.

Aleksey showed the tradeoffs of ADC interleaving choices. That affected latency, which made clock recovery more difficult. A parameterized model made it easier to study demultiplexer ratio effects. An IBIS bridge was used to connect the model to simulators. Maximum Likelihood Sequence Estimation (MLSE) was an algorithm for making decisions from only partially equalized signals. A trellis representation was used to handle eye diagrams with a fair amount of ISI. MLSE would provide BER information, while the RX would calculate SNR. In tests against measurement, good correlation had been achieved, measuring for typical and worst-case conditions. MLSE was a better method when there was high insertion loss.

Michael Mirmak asked if it would help to add digital output types to AMI. Aleksey said the samples converted by the ADC could still be thought of analog, but the clock jitter was embedded into the SNR of the samples. The clock was a problem only if it crossed the UI boundary, making that digital output not very important.

Arpad Muranyi wondered about the correlation of ADC models to silicon, also asking if the method was based only on SNR and BER. Aleksey said timing was only approximate in ADC implementations, and a distribution of samples could determine SNR. BER was easy to measure in the lab, and measured BER could be correlated to simulated SNR through an analytical expression.

Arpad asked what IBIS change would be needed. Aleksey said ADC implementations processed only one sample per UI. The models could be faster if the interface between model and simulator reflected that better, and it was easy enough to work with the existing standard through up-sampling, but it would help if the simulator knew the signal was digital and receive it as such.

Lance Wang believed the input to the ADC was equalized. Aleksey said that was correct. He said the signal integrity community was used to using eye diagrams, but with an ADC serdes there was no eye. It would be better to find new ways to analyze the signal rather than try to create an eye. Jared James said standards were still setting eye width and height requirements. Aleksey said standards were agnostic regarding implementation. Aleksey said for an ADC serdes the eye would collapse vertically, not horizontally. Only eye height mattered. He was not sure how an ADC implementation would be verified against standards.

David Halupka asked whether the proprietary MLSE algorithm would go into the simulator or stay in the model. Aleksey said he had no answer for where the LLSE algorithm could be moved to. Other ADC algorithms could go into simulators.

FREE ON-LINE SERDES SYSTEM CHANNEL SIMULATION
John Baprawski (SerDesign.com, USA)
(Start 03:57:30, Duration 13:10)

John Baprawski described a free cloud-based system for simulating parameterized series channels. The system contained standard parameterized serdes blocks. He showed a PAM4 example simulation output. High frequency aliasing was evident, because the channel impulse response had aliasing. Channel models from other tools could be used by importing the impulse response. John encouraged people to try the tool.

Someone asked about a slide showing an eye diagram difference between SerDesDesign.com and an EDA tool. John said high frequency aliasing cause the difference. Each tool had its own algorithm to convert frequency domain channel characterization to time domain. He said every tool gave different results. One solution was to ensure that every tool used the same impulse response. John was glad to hear that Touchstone 3 was being worked on. He hoped it would provide a means for channel models to be portable among tools. Someone said even with the same models there could be different results between tools. John said more work was needed to get consistency among tools.

CLOSING REMARKS
(Start 04:10:55, Duration 1:00)

Randy Wolff thanked presenters and sponsors. He encouraged people to participate in the IBIS task groups, to guide the future of IBIS.

NEXT MEETING

The next IBIS Open Forum teleconference meeting would be held on April 22, 2022. The following IBIS Open Forum teleconference meeting was tentatively scheduled for May 13, 2022.

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NOTES

IBIS CHAIR: Randy Wolff (208) 363-1764
     rrwolff@micron.com
     Principal Engineer, Silicon SI Group, Micron Technology, Inc.
     8000 S. Federal Way
     P.O. Box 6, Mail Stop: 01-720
     Boise, ID 83707-0006

VICE CHAIR: Lance Wang (978) 633-3388
     lance.wang@ibis.org
     Solutions Architect, Zuken USA
     238 Littleton Road, Suite 100
     Westford, MA 01886

SECRETARY: Mike LaBonte
     mlabonte@mathworks.com
     Senior Engineer
     1 Lakeside Campus Drive
     Natick, MA 01760

TREASURER: Bob Ross (503) 246-8048
     bob@teraspeedlabs.com

Engineer, Teraspeed Labs
10238 SW Lancaster Road
Portland, OR 97219

LIBRARIAN: Zhiping Yang (650) 214-0868
zhipingyang@google.com
Sr. Hardware Manager, Google LLC
1600 Amphitheatre Parkway
Mountain View, CA 94043

WEBMASTER: Steven Parker (845) 372-3294
sparker@marvell.com
Senior Staff Engineer, DSP, Marvell
2070 Route 52
Hopewell Junction, NY 12533-3507

POSTMASTER: Curtis Clark
curtis.clark@ansys.com
ANSYS, Inc.
150 Baker Ave Ext
Concord, MA 01742

This meeting was conducted in accordance with SAE ITC guidelines.

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- To inquire about joining the IBIS Open Forum as a voting Member.
- To purchase a license for the IBIS parser source code.
- To report bugs or request enhancements to the free software tools: ibischk6, tschk2, icmchk1, s2ibis, s2ibis2 and s2iplt.

The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.ibis.org/bugs/ibischk/
http://www.ibis.org/ bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.ibis.org/bugs/tschk/
http://www.ibis.org/bugs/tschk/bugform.txt

The BUG Report Form for icmchk resides along with reported BUGs at:

http://www.ibis.org/bugs/icmchk/
http://www.ibis.org/bugs/icmchk/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.ibis.org/bugs/s2ibis/bugs2i.txt
http://www.ibis.org/bugs/s2ibis2/bugs2i2.txt
http://www.ibis.org/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.ibis.org/

Check the IBIS file directory on ibis.org for more information on previous discussions and results:

http://www.ibis.org/directory.html

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SAE STANDARDS BALLOT VOTING STATUS

Organization	Interest Category	Standards Ballot Voting Status	February 18, 2022	March 11, 2022	April 1, 2022	April 8, 2022
Analog Devices (Maxim Integrated)	Producer	Inactive	X	-	-	-
ANSYS	User	Active	X	X	X	X
Applied Simulation Technology	User	Inactive	-	-	-	-
Broadcom Ltd.	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	-	X	X
Celestica	User	Inactive	-	-	-	-
Cisco Systems	User	Inactive	-	-	-	-
Dassault Systemes	User	Inactive	-	-	-	-
Ericsson	Producer	Inactive	-	-	-	-
Google	User	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Instituto de Telecomunicações	User	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	X
Keysight Technologies	User	Active	X	X	X	X
Luminous Computing	General Interest	Inactive	-	-	-	-
Marvell	Producer	Active	X	-	X	-
MathWorks (SiSoft)	User	Active	X	X	X	X
Micron Technology	Producer	Active	X	X	X	X
MST EMC Lab	User	Inactive	-	-	-	-
SerDesDesign.com	User	Inactive	-	-	-	X
Siemens EDA (Mentor)	User	Active	X	X	X	X
STMicroelectronics	Producer	Inactive	-	-	-	-
Synopsys	User	Active	X	X	X	X
Teraspeed Labs	General Interest	Active	X	X	X	X
Waymo	User	Inactive	X	-	X	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE Corp.	User	Inactive	-	-	-	-
Zuken	User	Active	-	X	X	X

Criteria for SAE member in good standing:
- Must attend two consecutive meetings to establish voting membership
- Membership dues current
- Must not miss two consecutive meetings (voting by email counts as attendance)

Interest categories associated with SAE standards ballot voting are:
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