

Mixed Signal Channel Modeling for Signal Integrity Analysis



Saliou DIEYE

Agilent EESOF EDA

Saliou_dieye@agilent.com

Riccardo GIACOMETTI

Agilent EESOF EDA

Riccardo_giacometti@agilent.com

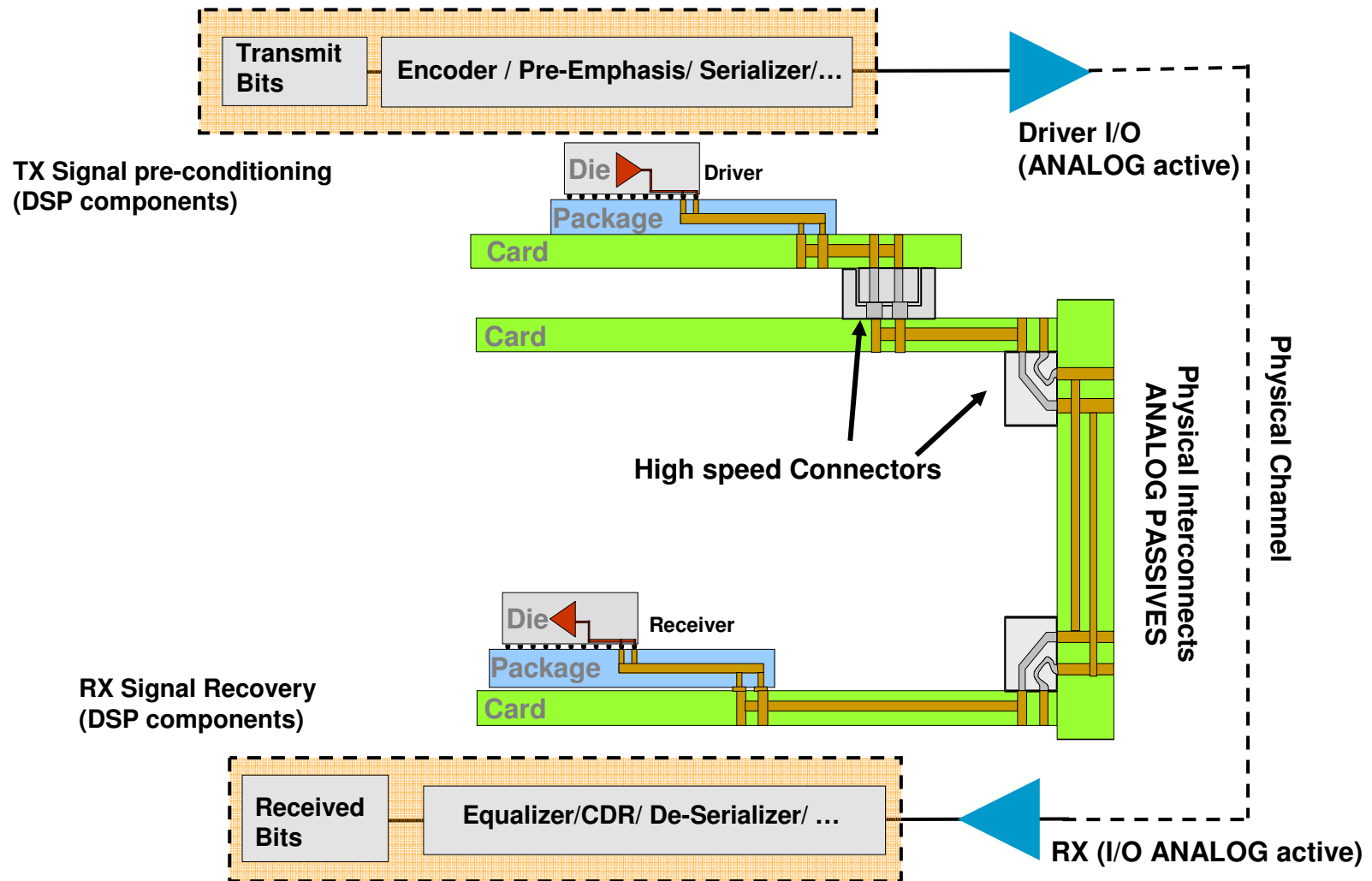


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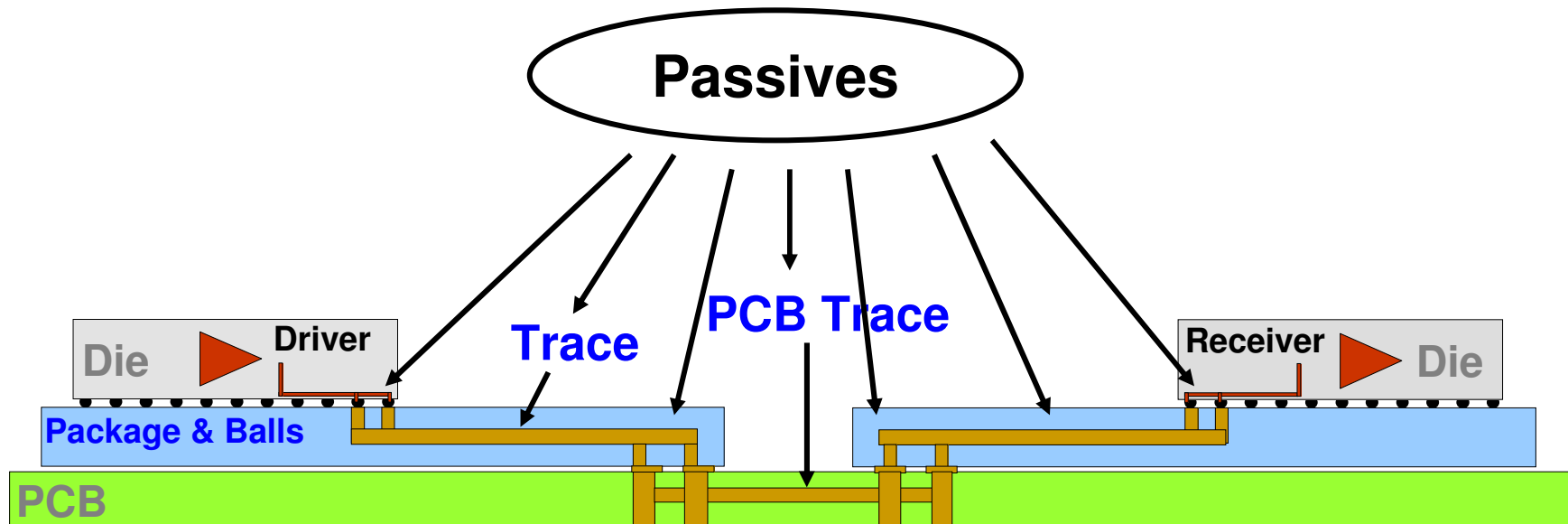
Agenda

- Analog Modeling
- DSP Modeling
- Mixed domain (analog + DSP) co-simulation

Typical Channel (DSP and ANALOG component models)



Modeling Analog devices – Passive components



For passive structures

- **S-parameters** – Can be obtained from **Measurement** or **EM simulation**
- **Analytical models** – obtained from software package libraries
- **IBIS models** – where available.
- **SPICE models** – lumped component based models

Transmission Line models for PCB traces

Account for impedance, delay, conductor loss, dielectric loss, and crosstalk

Analytical microstrip, stripline models

MACLIN3
 CLin1
 Subst="MSub1"
 W1=25.0 mil
 W2=15.0 mil
 W3=15.0 mil
 S1=8.0 mil
 S2=12.0 mil
 L=100.0 mil

MBSTUB
 Stub1
 Subst="MSub1"
 W=25.0 mil
 Ro=60.0 mil
 Angle=60
 D=3.0 mil

MCROSSO
 Cros1
 Subst="MSub1"
 W1=25.0 mil
 W2=50.0 mil
 W3=25.0 mil
 W4=50.0 mil

MCURVE
 Curve 1
 Subst="MSub1"
 W=25.0 mil
 Angle=90
 Radius=100.0 mil

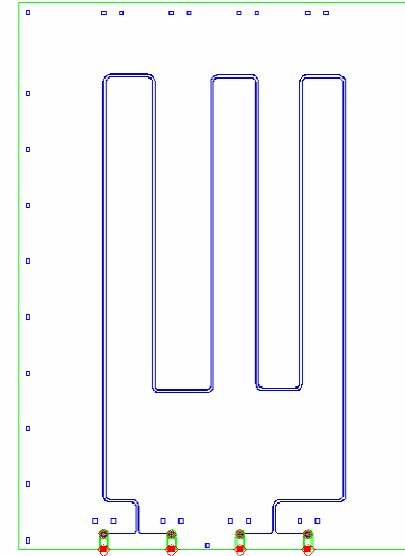
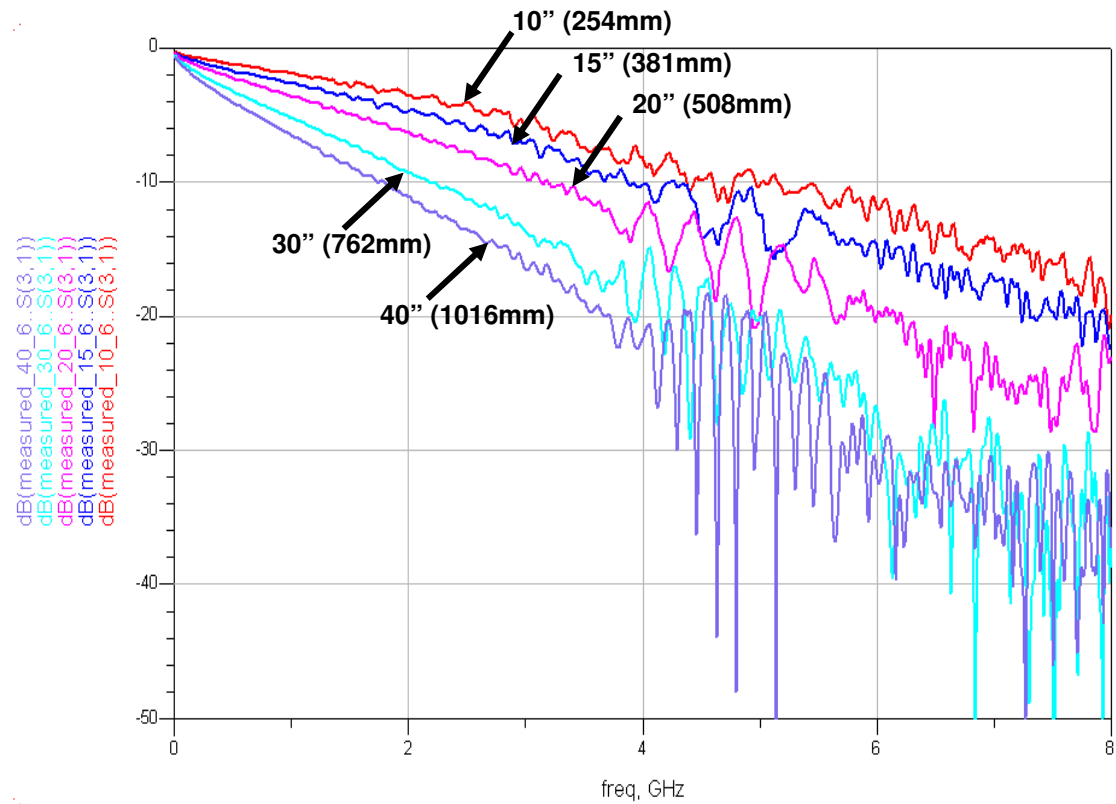
Multilayer Interconnect Models use a built-in field-solver

MLCTLC
 CLin1
 Subst="Subst"
 Length=100.0 mil
 W=10.0 mil
 S=5.0 mil
 Layer=1
 RL0C_File=
 ReuseRL0C=no

MLSLANTED8
 Slant1
 Subst="Subst"
 L_COffset=100.0 mil
 Y_Offset=100.0 mil
 W=10.0 mil
 S=2.0 mil
 Layer=1

MLCNR8B
 Com1
 Subst="Subst"
 Angle=90
 W=10.0 mil
 S=5.0 mil
 Layer=1

Measurement based modeling



Touchstone Files

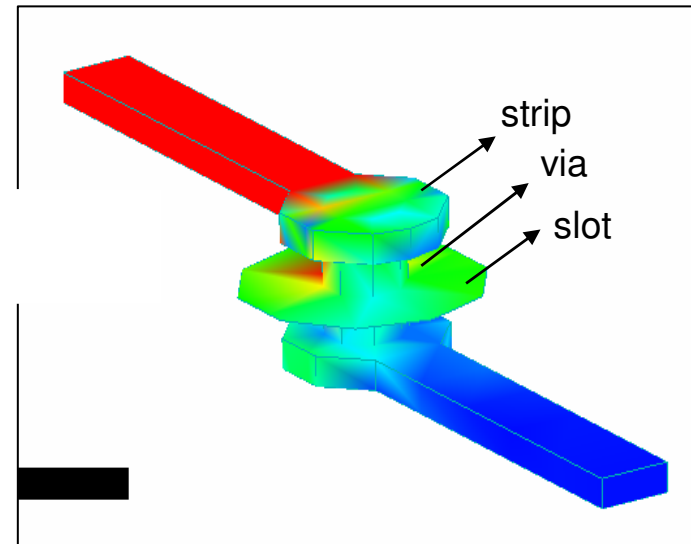
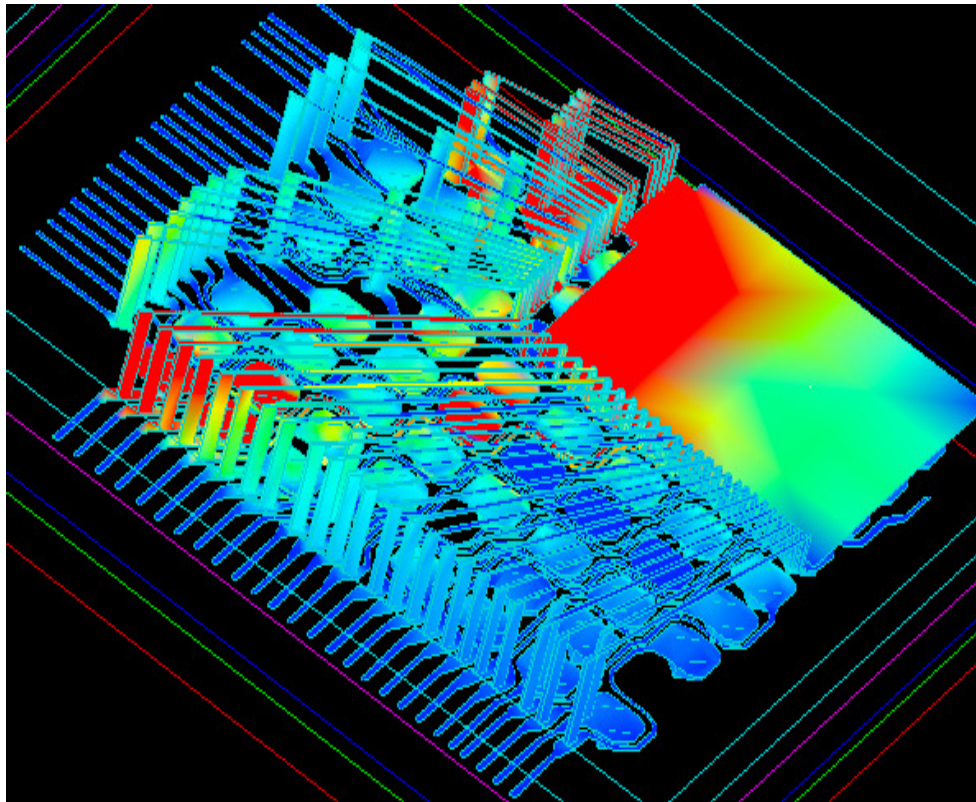
CITI Files

MDIF Files

TDR or VNA Measurements

EM based modeling: 3D Planar EM Simulation

Efficient, accurate simulation of board interconnects

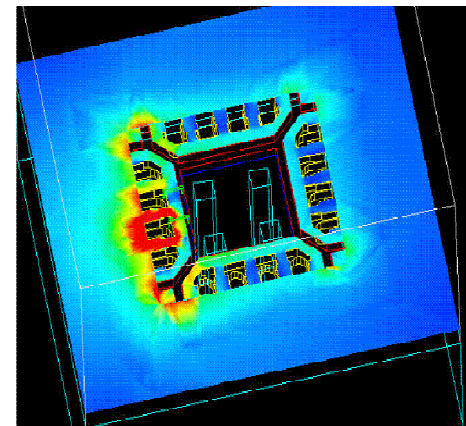
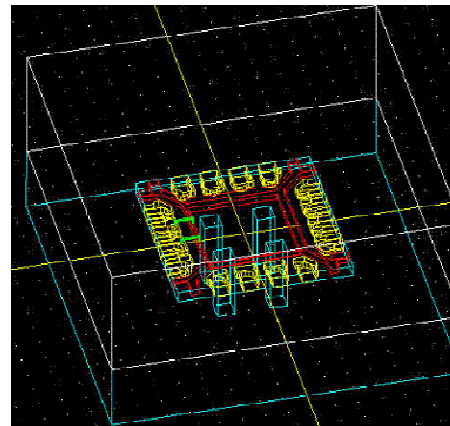
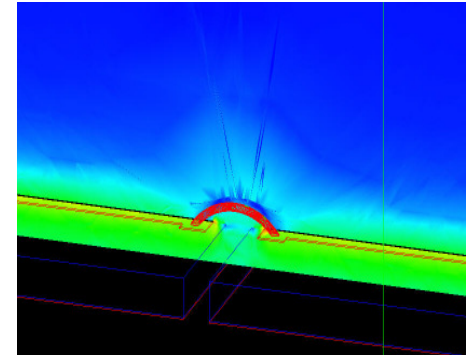
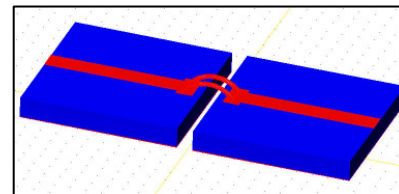


Accurate simulation of Via holes now possible with Method of Moments Planar EM

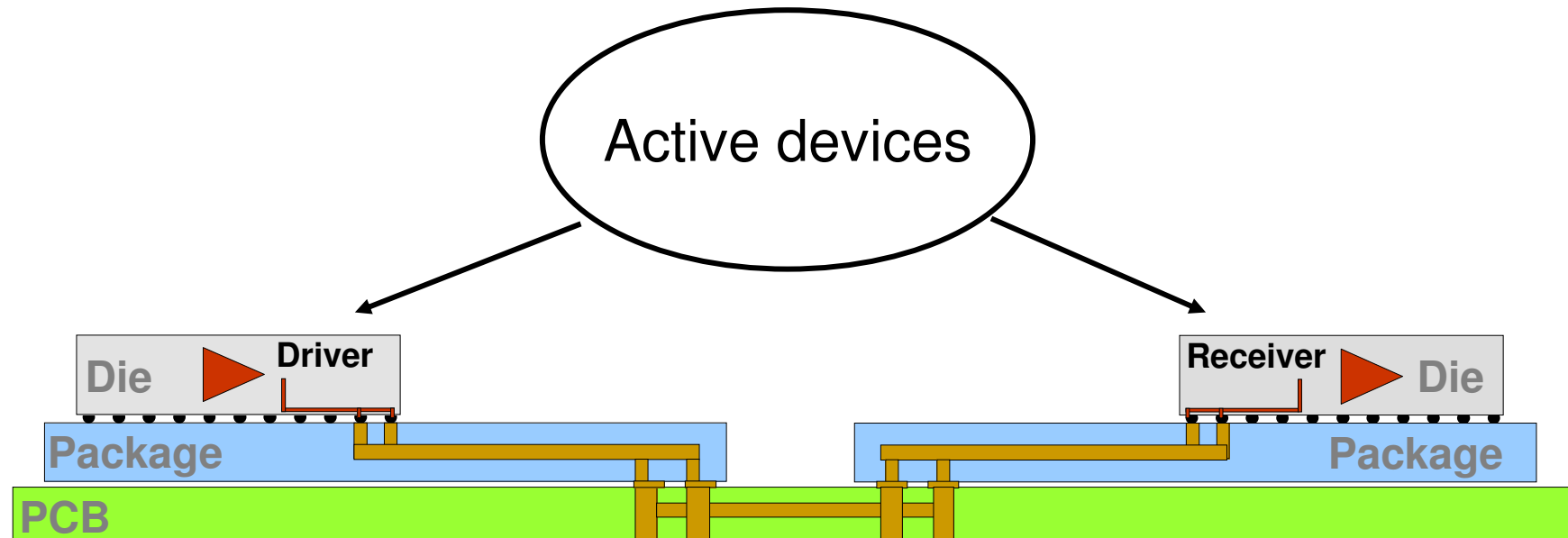
EM Based Models: 3D Full Wave EM simulation

Fast and accurate electromagnetic simulation of arbitrary 3D passive components including:

- Traces, vias, and transitions
- Connectors and packages
- Modeling wire bonds



Modeling Analog Active Components

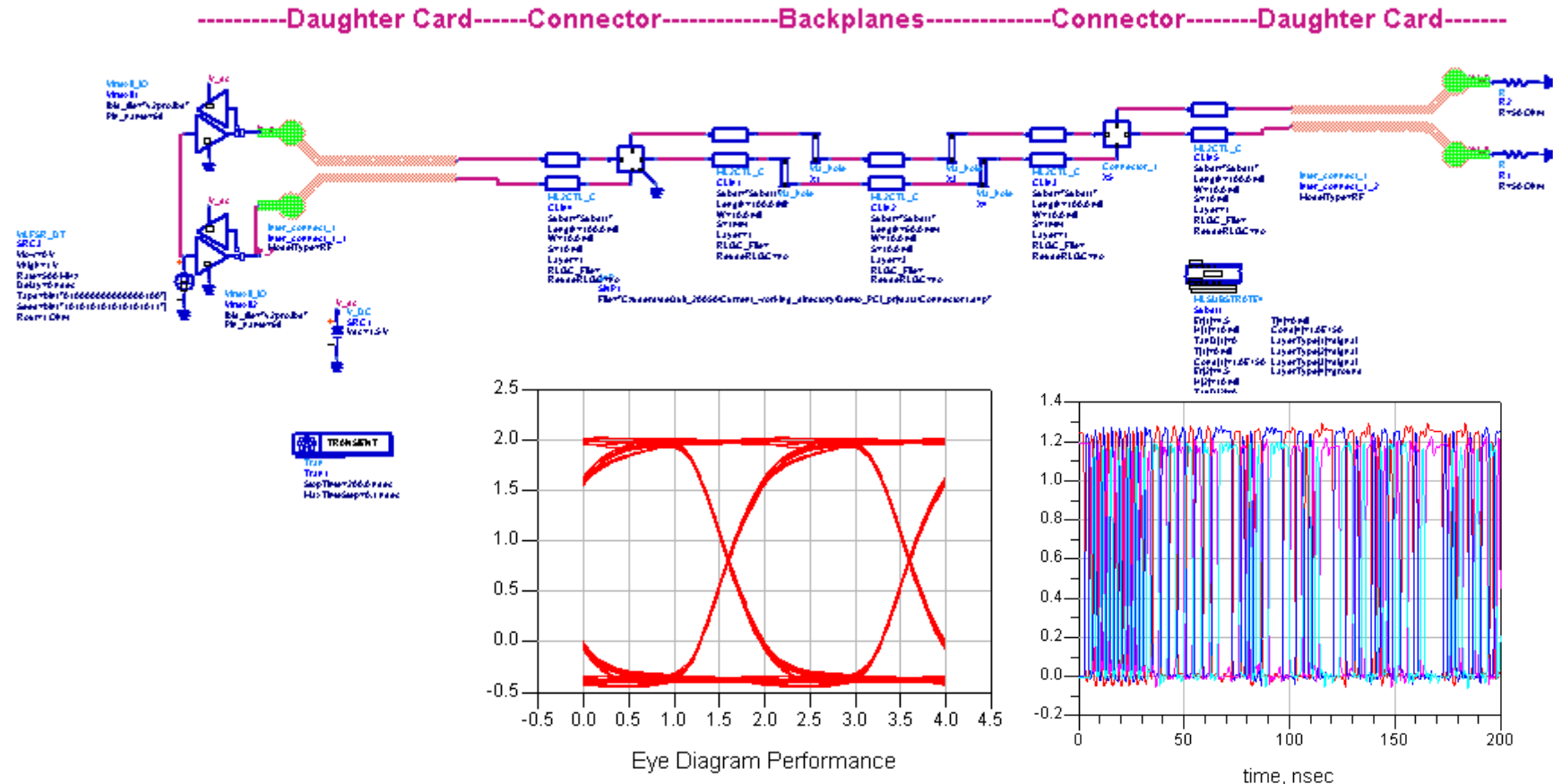


For Analog active devices, IC vendors provide

- **IBIS** – behavioral modeling of I/O buffers
- **HSPICE models** – transistor level models, can protect vendor IP
- **VerilogA** – transistor level or behavioral model

I/O Driver + Interconnect Modeling

Channel Simulation- PCI Express



I/O simulation with Xilinx Virtex-II Pro IBIS Models

VerilogA IBIS Macro Models

```

include "constants.vams"
include "disciplines.vams"

module Buffers_ads (In_D, En_D, IO_P, IO_N, PC_ref, PU_ref, PD_ref,
input In_D, En_D;
electrical In_D, En_D, Rcv_D;
electrical IO_P, IO_N, PC_ref, PU_ref, PD_ref, GC_ref, PC_refPB,

IO_buffer PosM (In_PM, En_D, Rcv_PM, IO_P, PC_ref, PU_ref,
IO_buffer NegM (In_NM, En_D, Rcv_NM, IO_N, PC_ref, PU_ref,
IO_buffer PosB (In_PB, En_D, Rcv_PB, IO_P, PC_refPB, PU_refPB,
IO_buffer NegB (In_NB, En_D, Rcv_NB, IO_N, PC_refNB, PU_refNB,

analog begin
V(In_PM) <+ V(In_D);
V(In_NM) <+ V(PU_ref) - V(In_D);
V(In_NB) <+ absdelay( V(In_D), 10.0e-9);
V(In_PB) <+ absdelay((V(PU_ref)-V(In_D)), 10.0e-9);

V(PC_ref, PC_refPB) <+ 0.0;
V(PU_ref, PU_refPB) <+ 0.0;
V(PD_ref, PD_refPB) <+ 0.0;
V(GC_ref, GC_refPB) <+ 0.0;

V(PC_ref, PC_refNB) <+ 0.0;
V(PU_ref, PU_refNB) <+ 0.0;
V(PD_ref, PD_refNB) <+ 0.0;
V(GC_ref, GC_refNB) <+ 0.0;
end

```

TRANSIENT

Trai
Trai1
StopTime=6000 usec
MaxTimeStep=0.1 usec

ML2CTL_C
CLin1
Sibst="Sibst"
Length=10mm
W=10.0mil
S=5.0mil
Layer=1
RLGC_File=
RetseRLGC=10

ML2CTL_C
CLin2
Sibst="Sibst"
Length=10mm
W=10.0mil
S=5.0mil
Layer=1
RLGC_File=
RetseRLGC=10

ML2CTL_C
CLin3
Sibst="Sibst"
Length=60mm
W=10.0mil
S=5.0mil
Layer=1
RLGC_File=
RetseRLGC=10

MUCRNR2
Con1
Sibst="Sibst"
Angle=90
W=10.0mil
S=5.0mil
Layer=1

MUCRNR2
Con2
Sibst="Sibst"
Angle=90
W=10.0mil
S=5.0mil
Layer=1

MLSUBSTR
Sibst
Er=4.5

out, V

time, nsec

Analog Components of a Channel

Transmission Lines

Via Holes

High Speed Connectors

Package

I/O – IBIS models and Transistor level models

DSP Components in a Channel

Decision Feedback Equalizer

Feed Forward Equalizer

Clock and Data Recovery

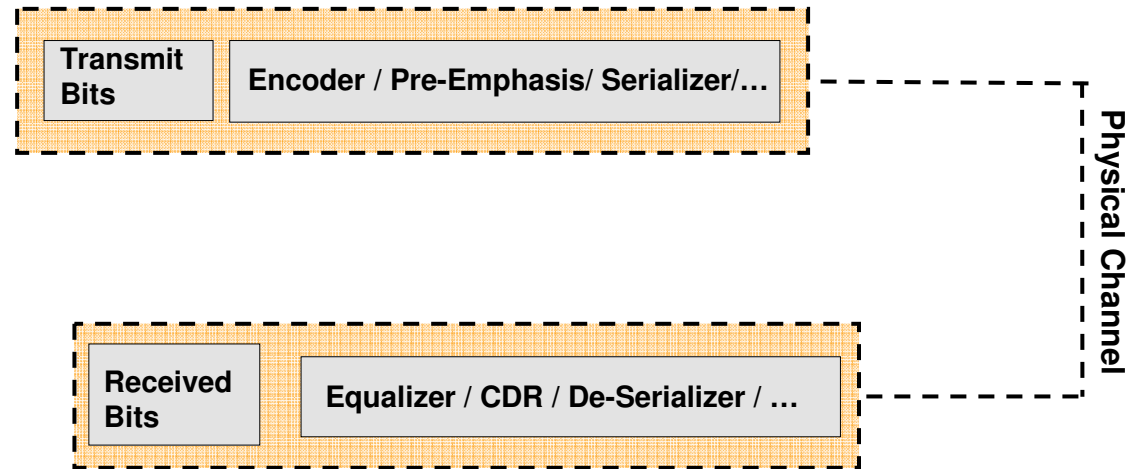
Gain Controls

SERDES Models

*Can I mix DSP
and ANALOG
models in a
single
simulation?*

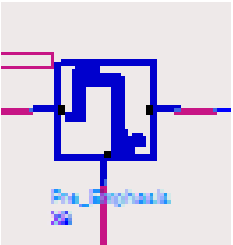


Modeling Pre-emphasis and Equalization

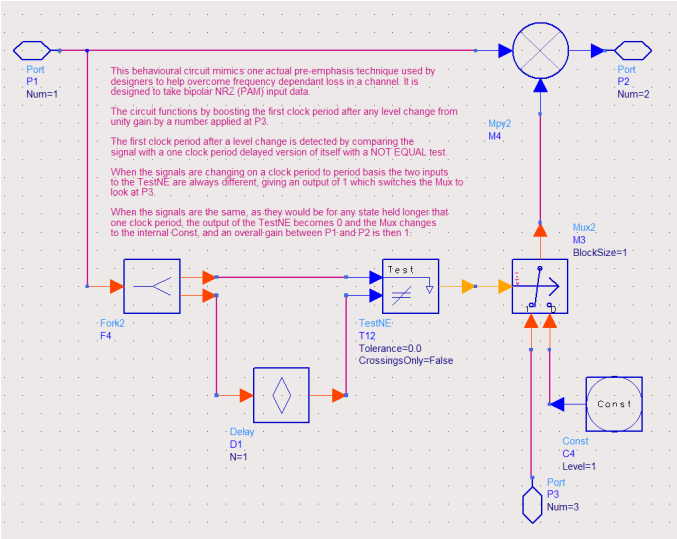


DSP components can be represented in different ways: C/C++, System C, MATLAB, HDL

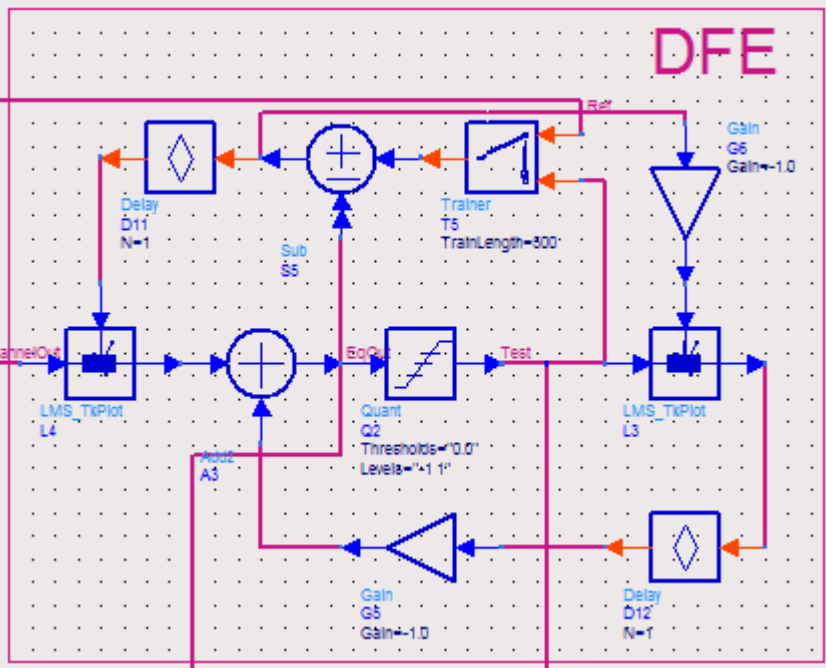
DSP Behavioral Models



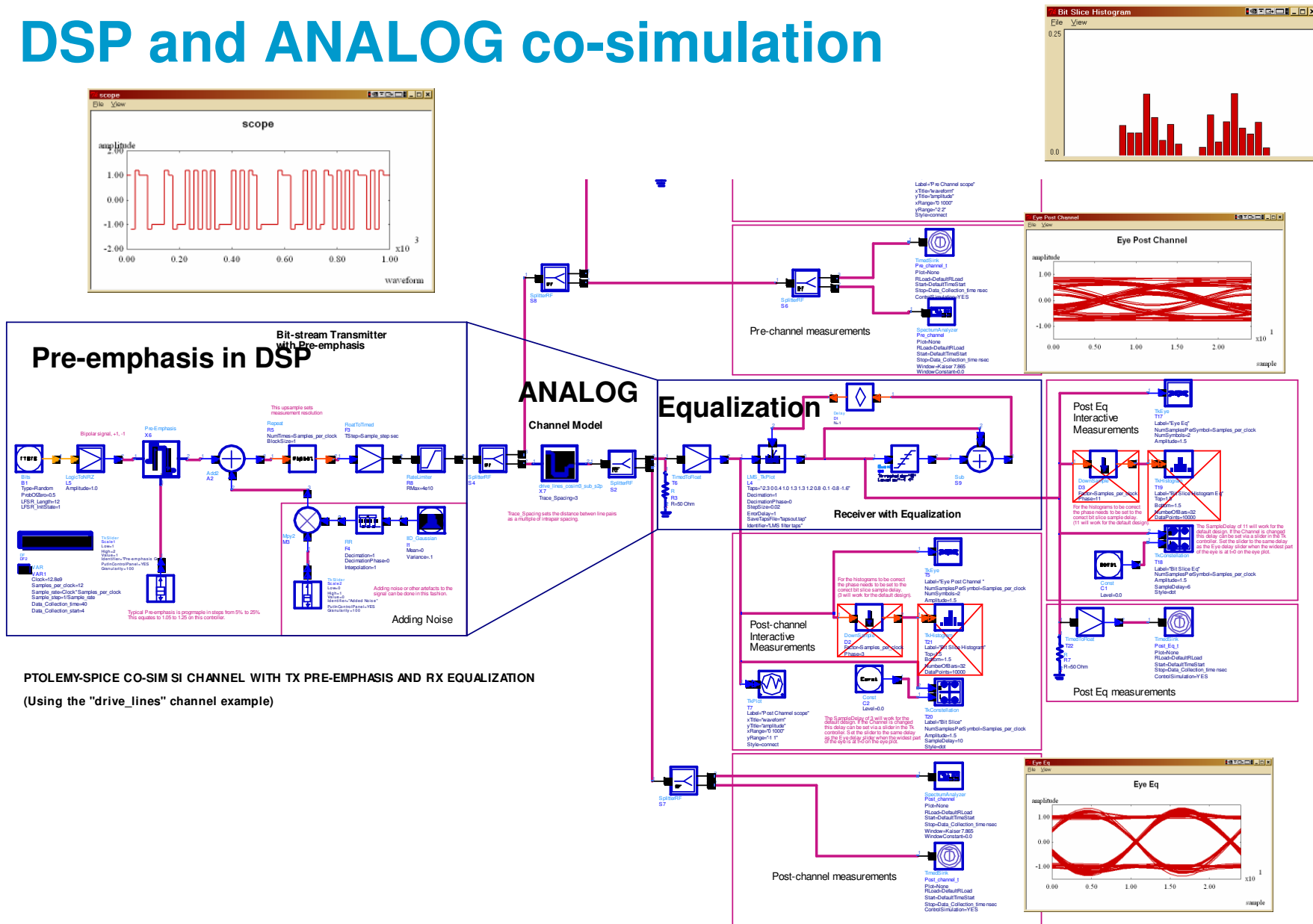
Pre-Emphasis



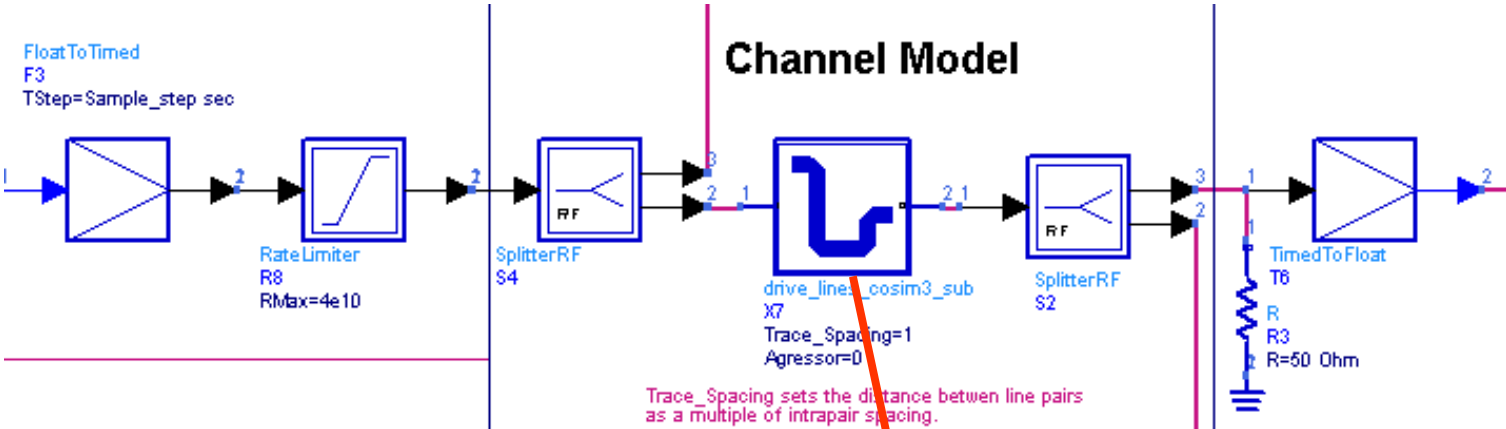
Equalization



DSP and ANALOG co-simulation



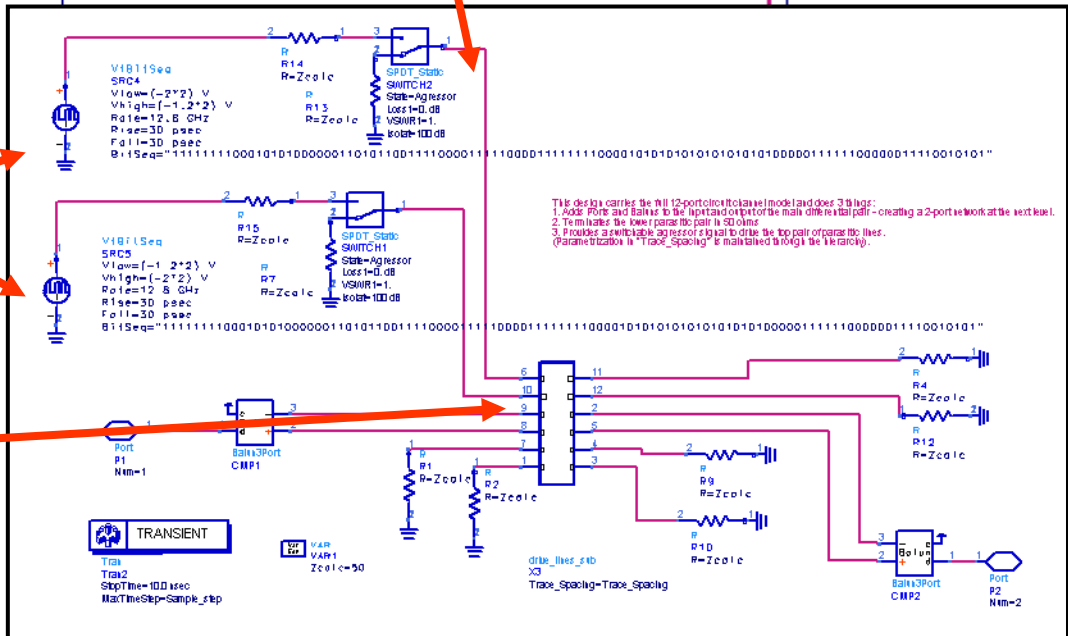
Channel Model



Trace_Spacing sets the distance between line pairs as a multiple of intrapair spacing.

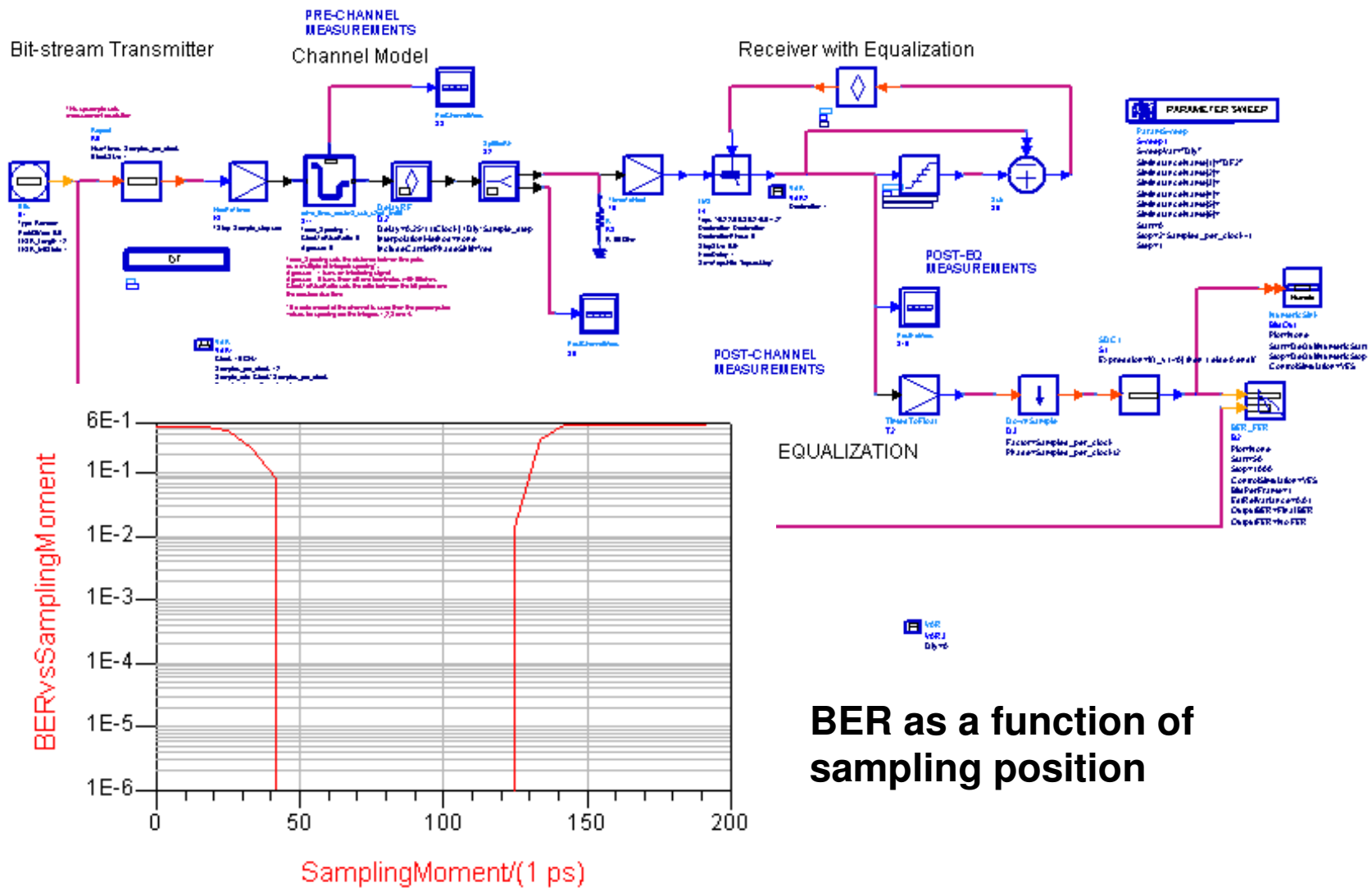
Aggressor Lines

Channel Sub-network



This design carries the full 12-port circuit model and does 3 things:
 1. Adds ports and buses to the input and output of the main drive_line pair - creating a 2-port network at the external.
 2. Terminates the lower parasitic pair in 50 Ohms.
 3. Provides a switchable aggressor signal to drive the top pair of parasitic lines.
 (parameterized in 'Trace_Spacing' & maintained through the hierarchy).

Bit Error Ratio Simulation



BER as a function of sampling position