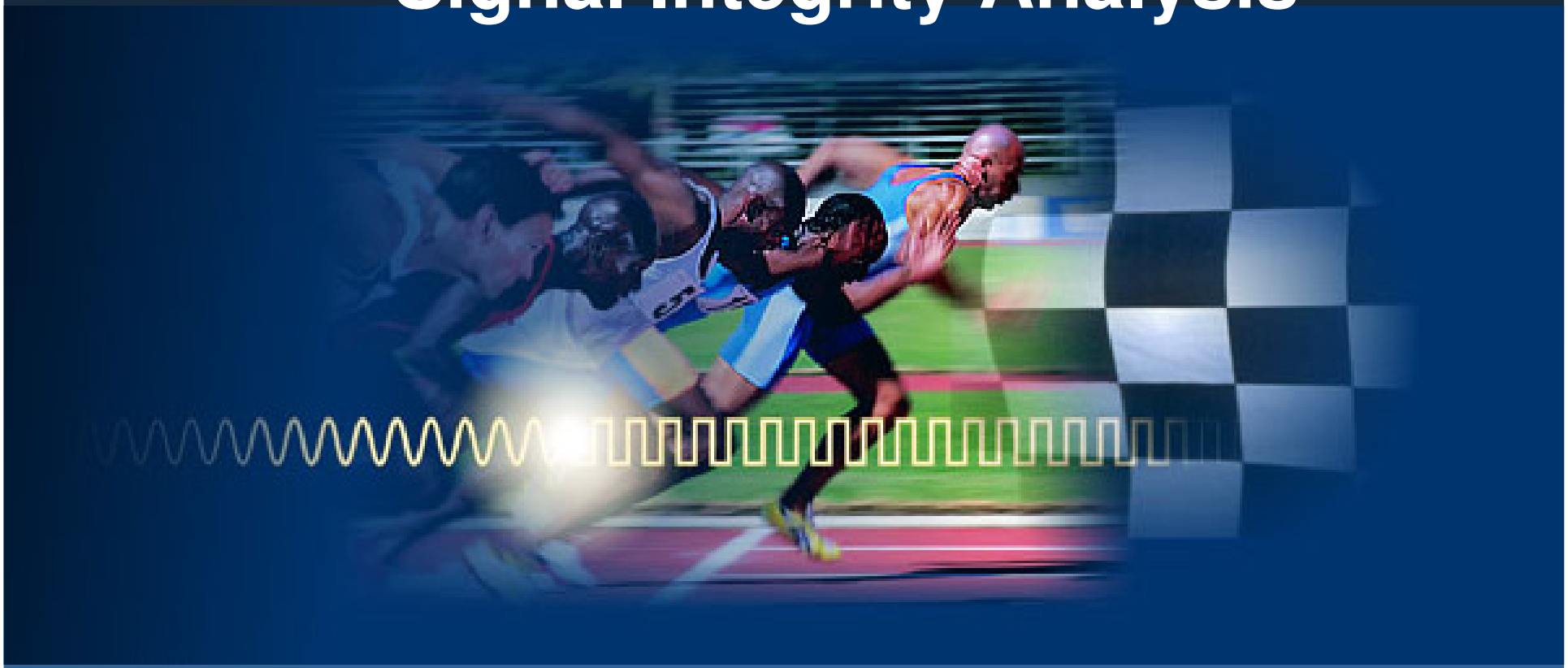
Mixed Signal Channel Modeling for Signal Integrity Analysis



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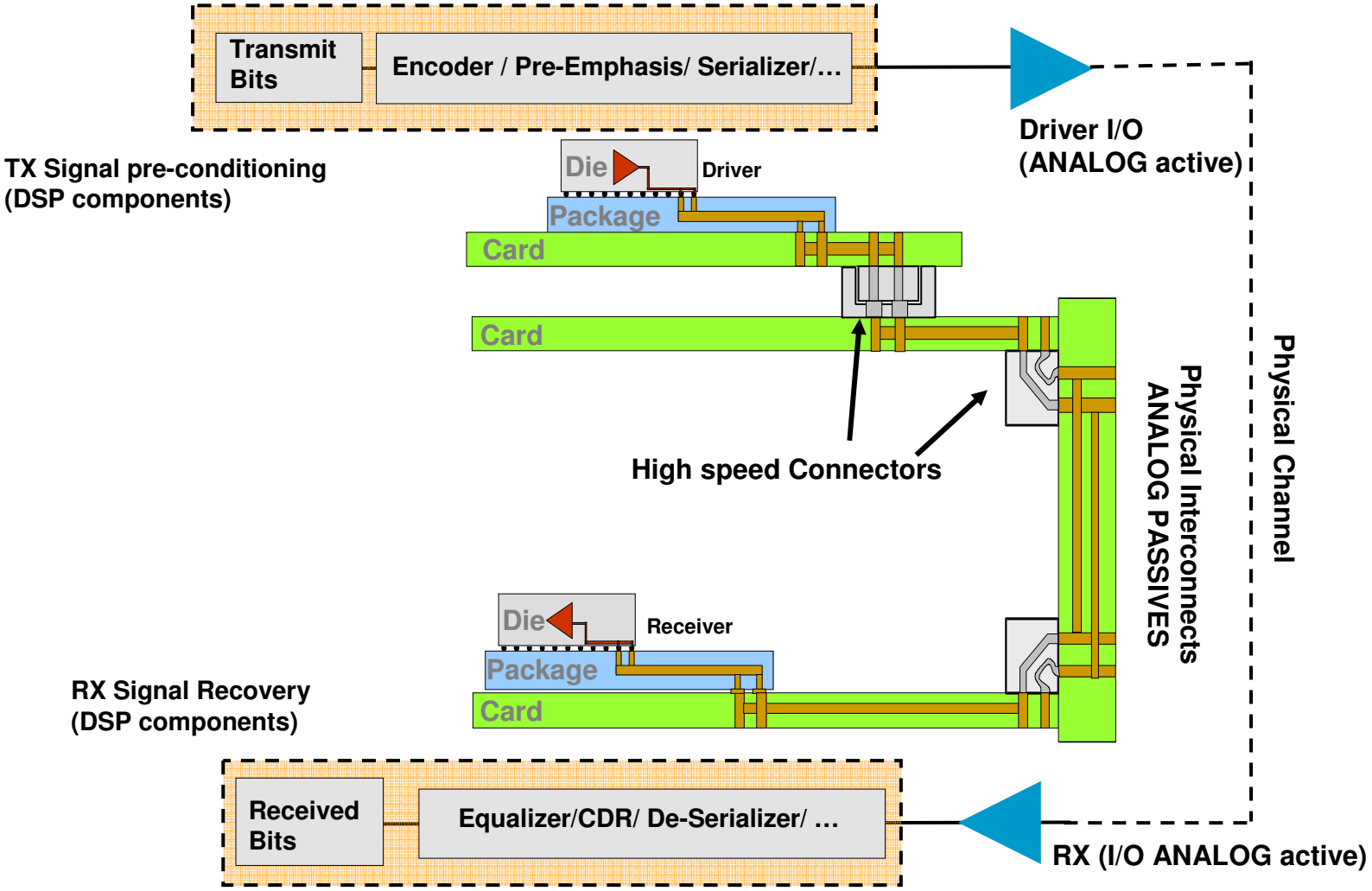
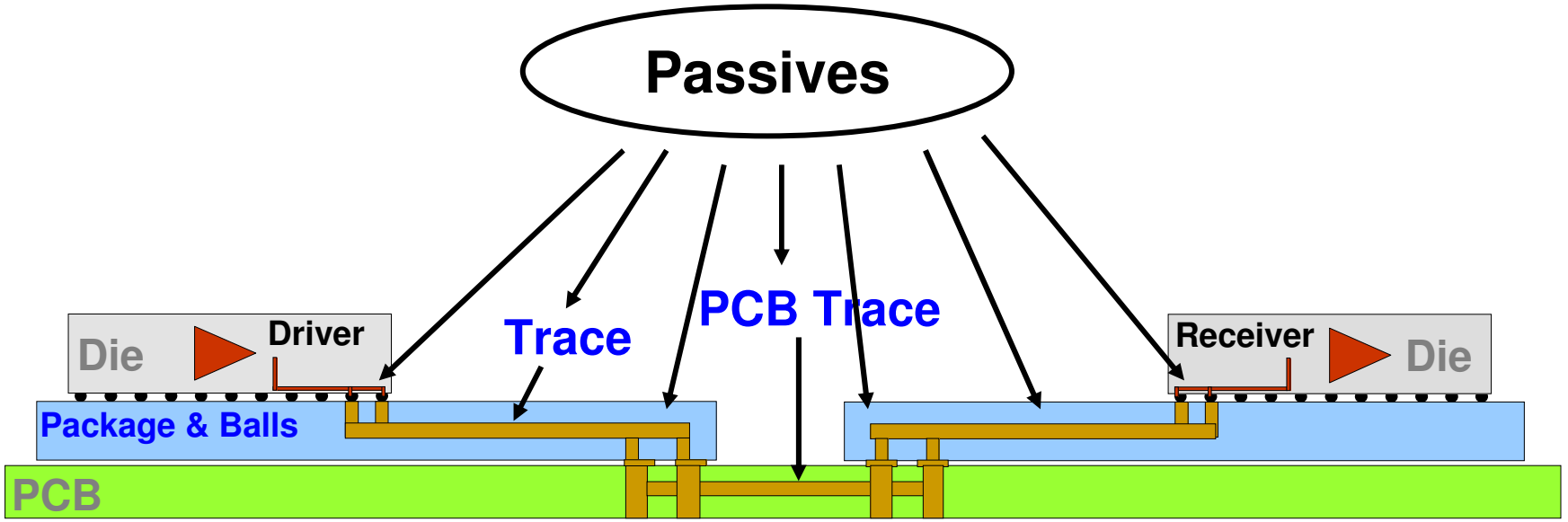
Agenda

- Analog Modeling
- DSP Modeling
- Mixed domain (analog + DSP) co-simulation

Typical Channel (DSP and ANALOG component models)



Modeling Analog devices – Passive components



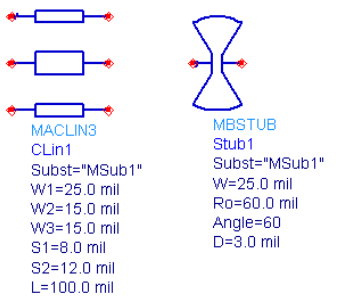
For passive structures

- S-parameters – Can be obtained from **Measurement** or **EM simulation**
- Analytical models – obtained from software package libraries
- IBIS models – where available.
- SPICE models – lumped component based models

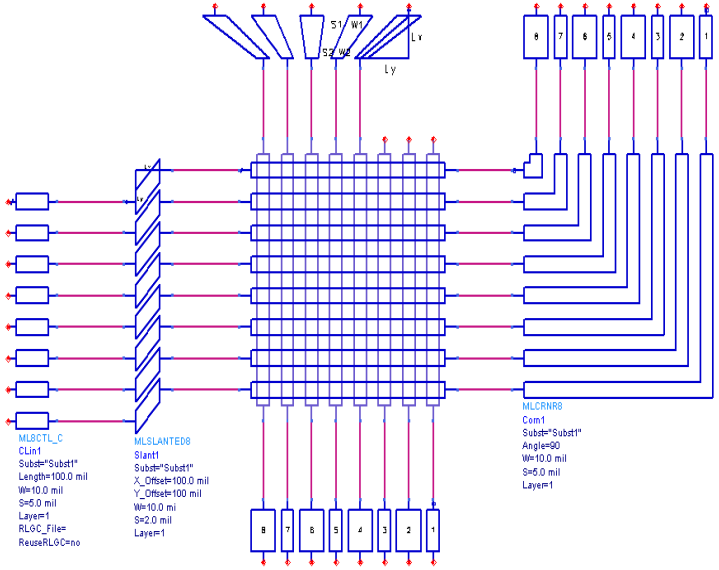
Transmission Line models for PCB traces

Account for impedance, delay, conductor loss, dielectric loss, and crosstalk

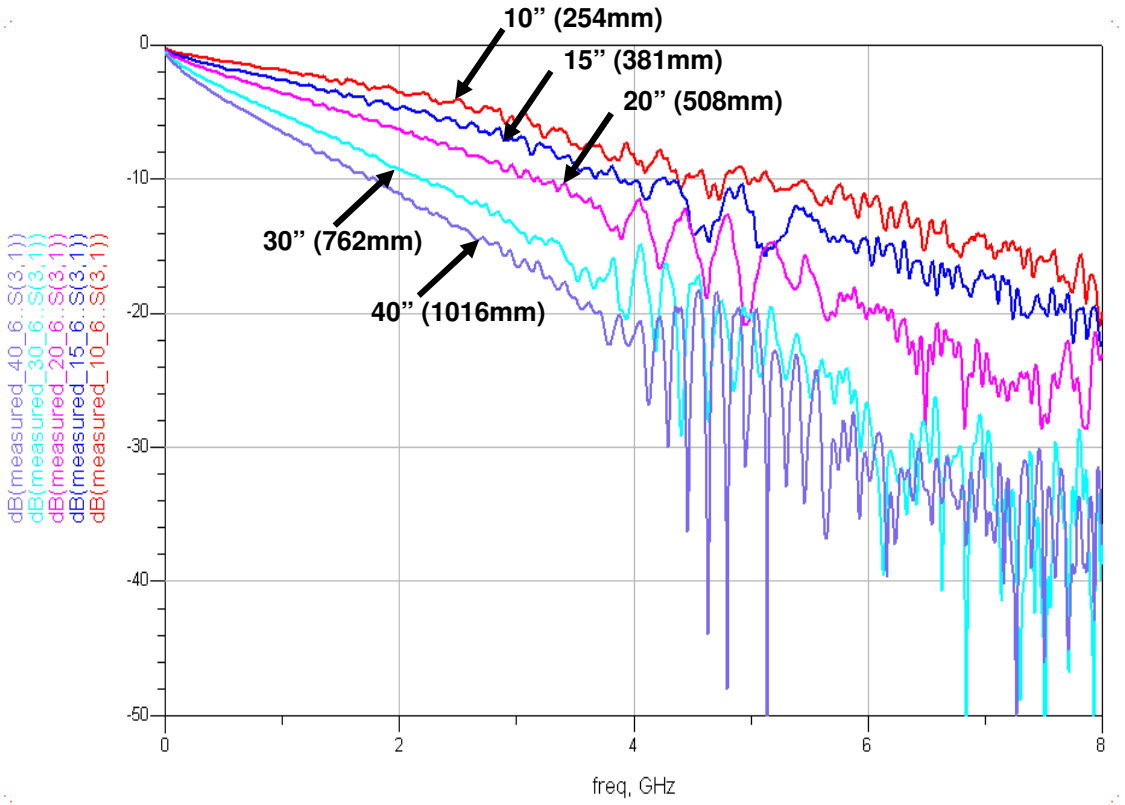
Analytical microstrip, stripline models

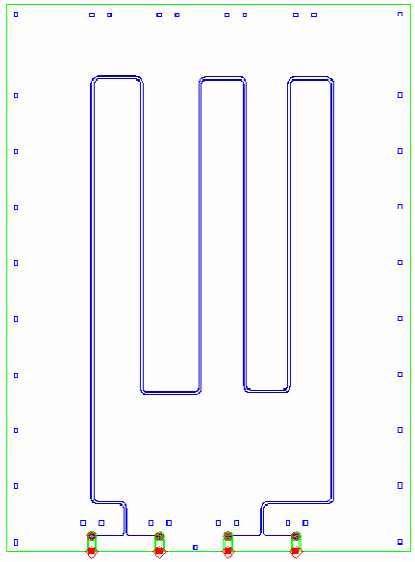


Multilayer Interconnect Models use a built-in field-solver



Measurement based modeling





Touchstone Files

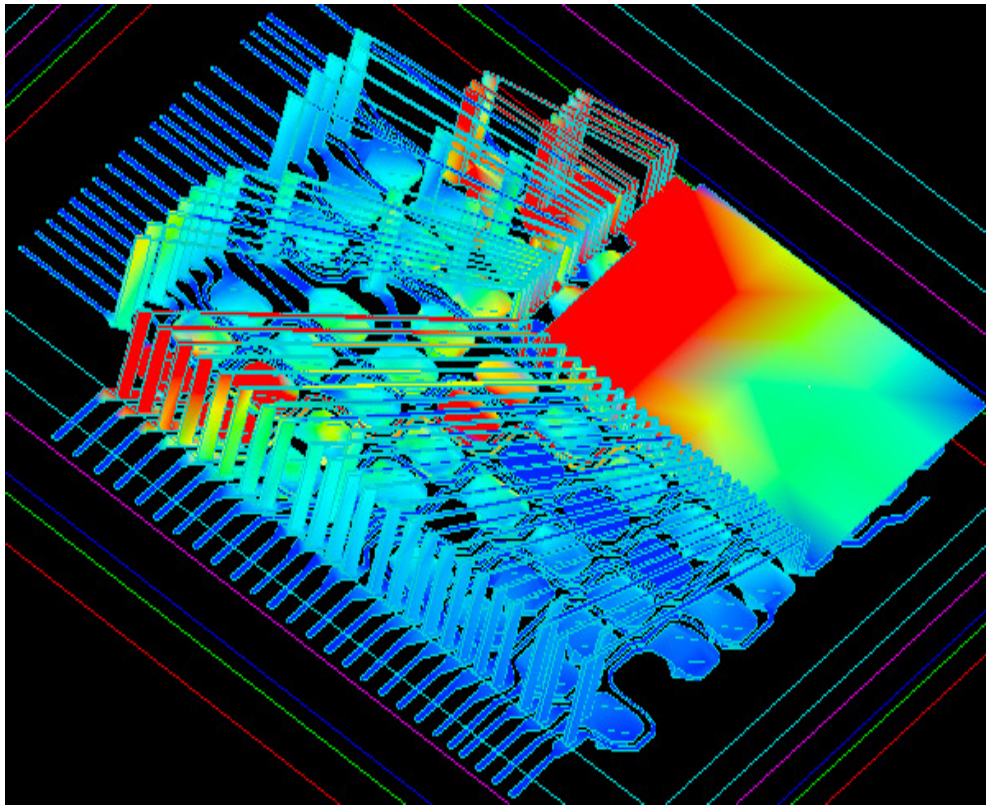
CITI Files

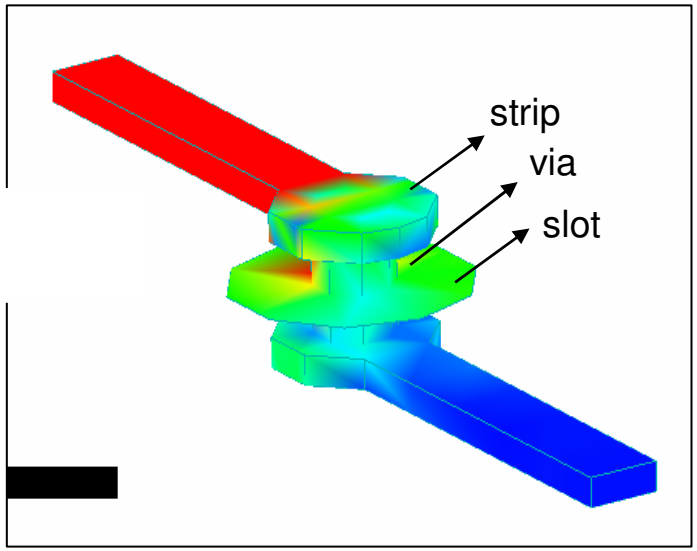
MDIF Files

TDR or VNA Measurements

EM based modeling:
3D Planar EM Simulation

Efficient, accurate simulation of board interconnects



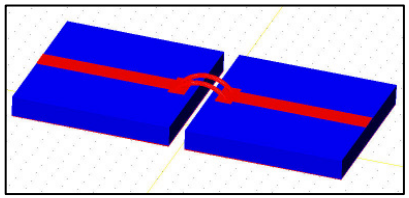


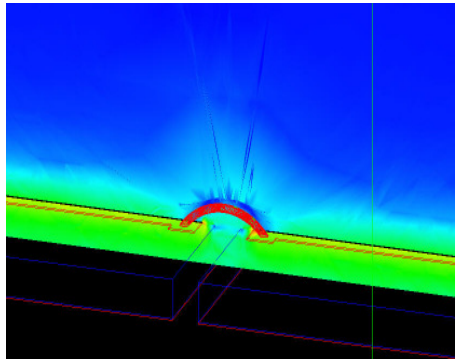
Accurate simulation of Via holes now possible with Method of Moments Planar EM

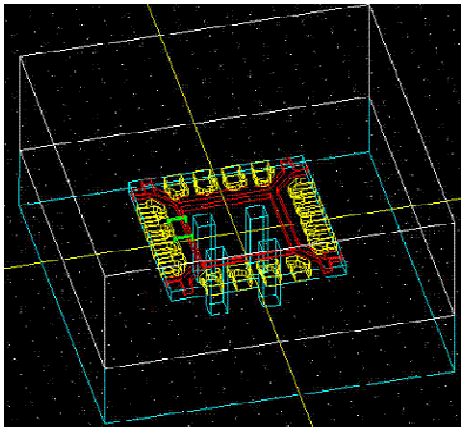
EM Based Models:
3D Full Wave EM simulation

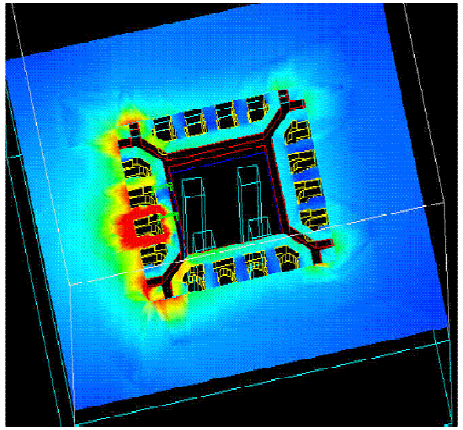
Fast and accurate electromagnetic simulation of arbitrary 3D passive components including:

- Traces, vias, and transitions
- Connectors and packages
- Modeling wire bonds

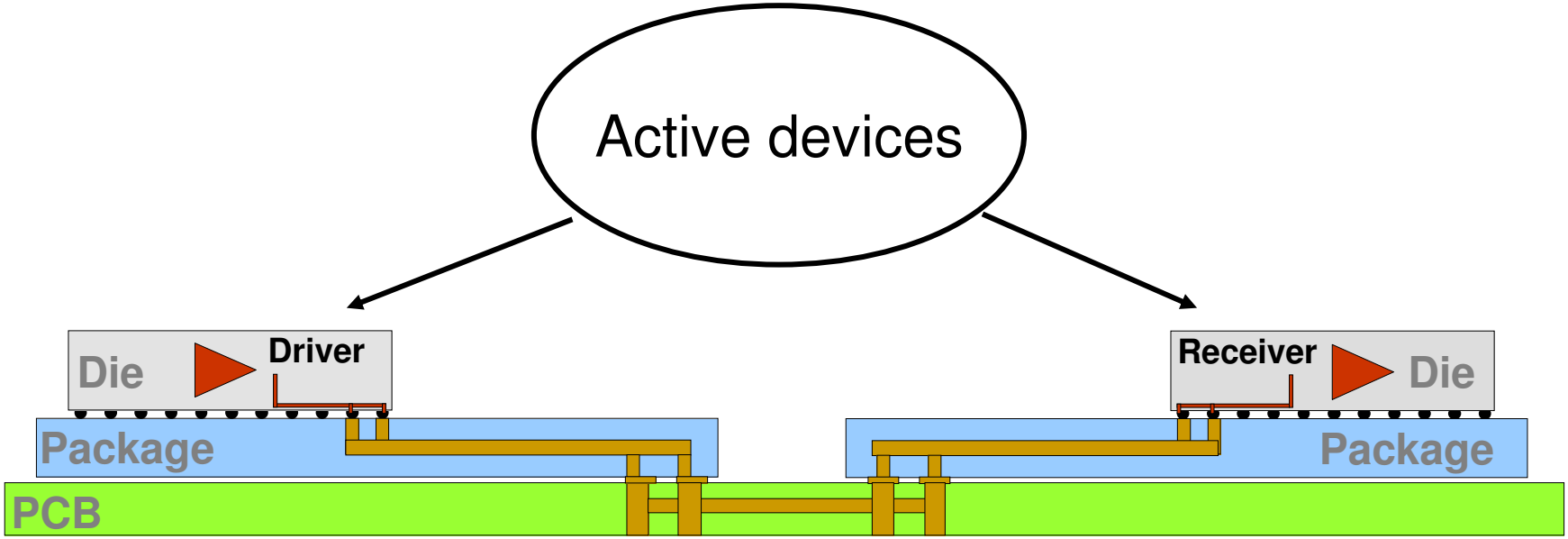








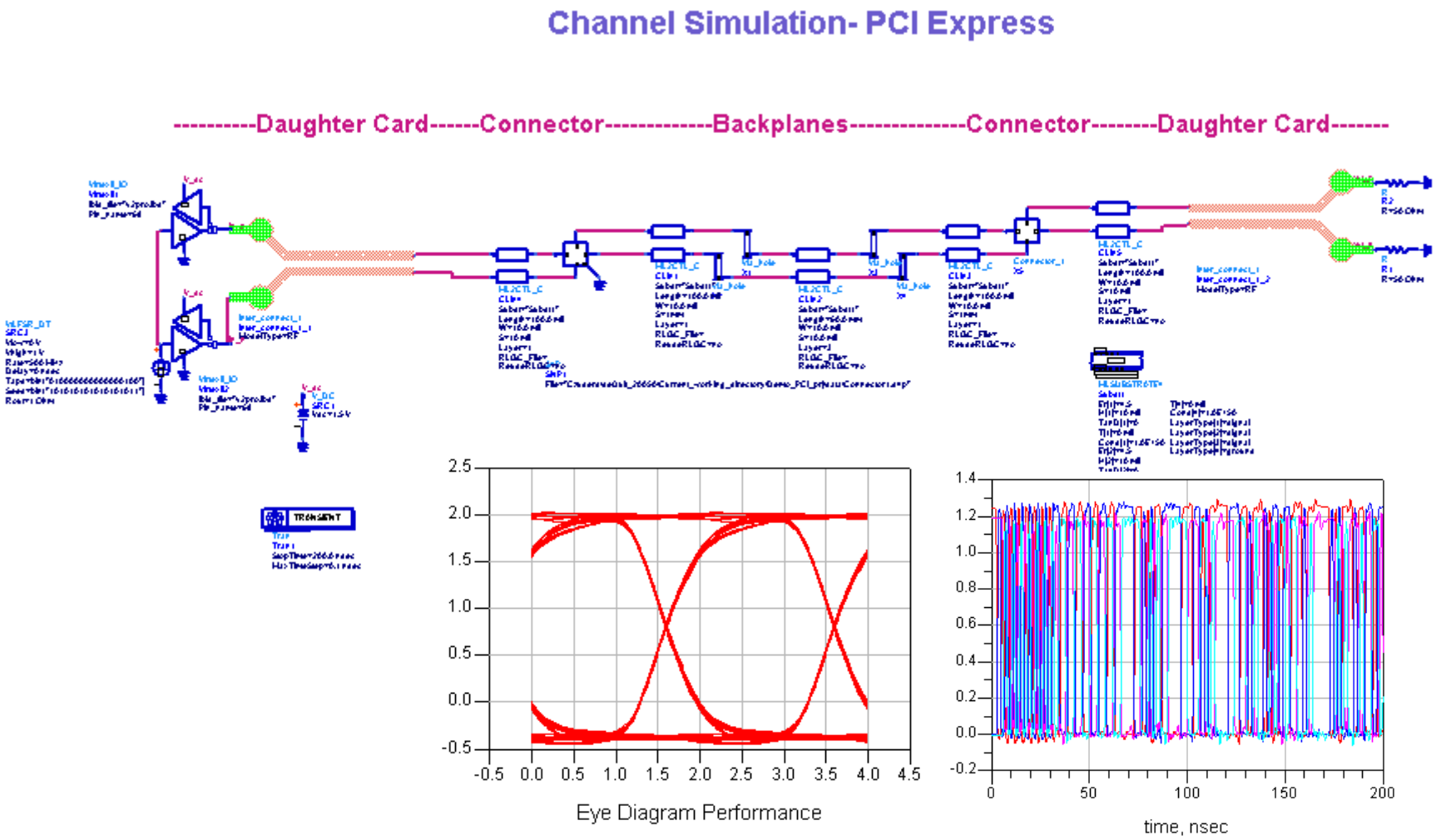
Modeling Analog Active Components



For Analog active devices, IC vendors provide

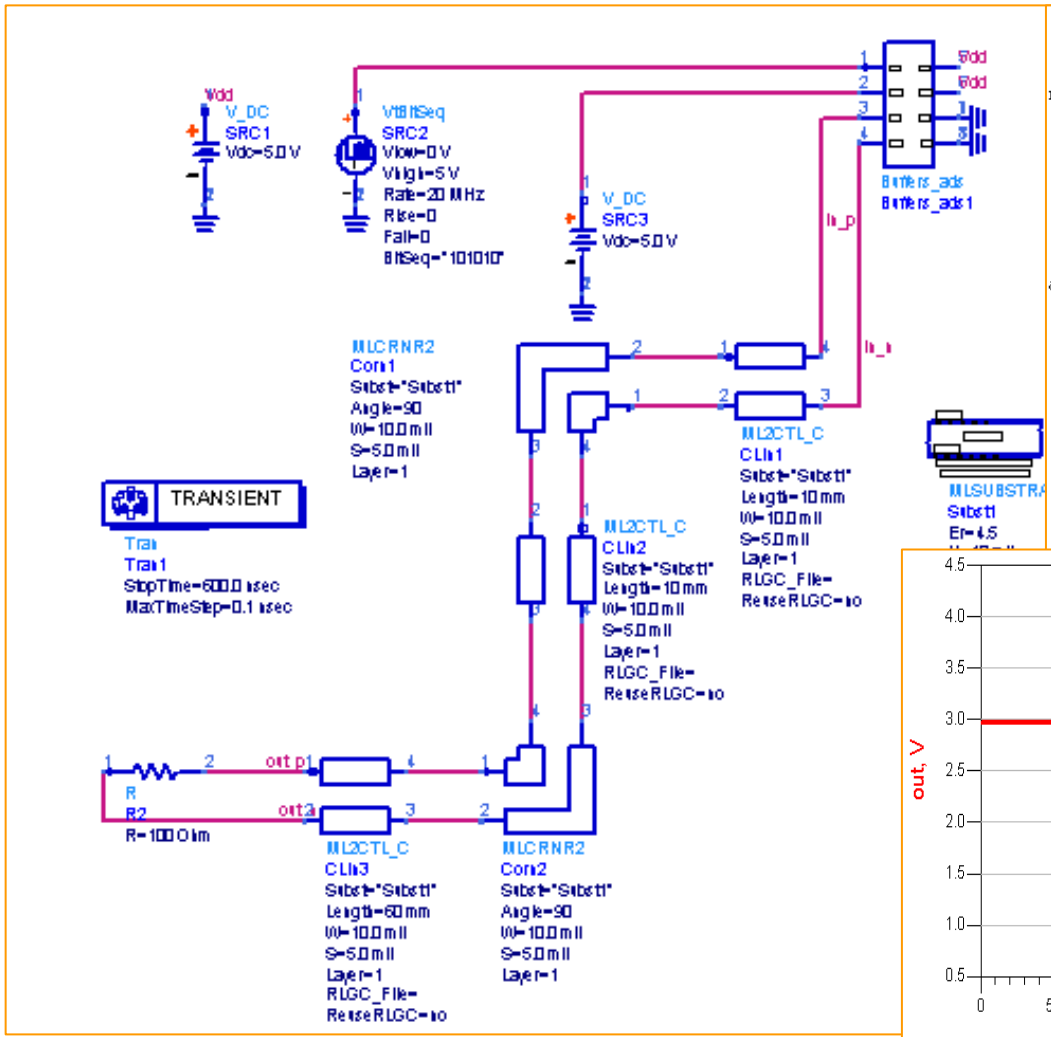
- IBIS – behavioral modeling of I/O buffers
- HSPICE models – transistor level models, can protect vendor IP
- VerilogA – transistor level or behavioral model

I/O Driver + Interconnect Modeling

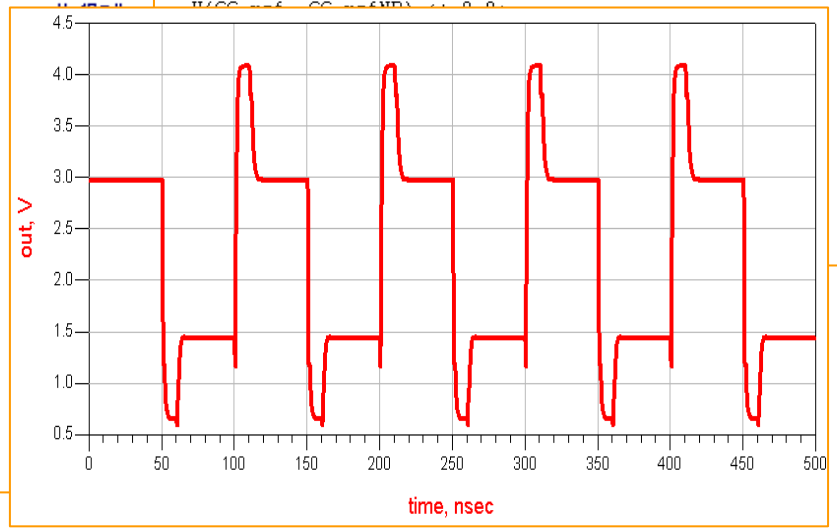


I/O simulation with Xilinx Virtex-II Pro IBIS Models

VerilogA IBIS Macro Models




```
`include "constants.vams"
`include "disciplines.vams"


module Buffers_ads (In_D, En_D, IO_P, IO_N, PC_ref, PU_ref, PD_ref,
   input       In_D, En_D;
   electrical In_D, En_D, Rcv_D;
   electrical IO_P, IO_N, PC_ref, PU_ref, PD_ref, GC_ref, PC_refPB,

   IO_buffer  PosM  (In_PM, En_D, Rcv_PM, IO_P, PC_ref,    PU_ref,
   IO_buffer  NegM  (In_NM, En_D, Rcv_NM, IO_N, PC_ref,    PU_ref,
   IO_buffer  PosB  (In_PB, En_D, Rcv_PB, IO_P, PC_refPB, PU_refPB,
   IO_buffer  NegB  (In_NB, En_D, Rcv_NB, IO_N, PC_refNB, PU_refNB,

analog begin
   V(In_PM)  <+ V(In_D);
   V(In_NM)  <+ V(PU_ref) - V(In_D);
   V(In_NB)  <+ absdelay( V(In_D),              10.0e-9);
   V(In_PB)  <+ absdelay((V(PU_ref)-V(In_D)), 10.0e-9);

   V(PC_ref, PC_refPB) <+ 0.0;
   V(PU_ref, PU_refPB) <+ 0.0;
   V(PD_ref, PD_refPB) <+ 0.0;
   V(GC_ref, GC_refPB) <+ 0.0;

   V(PC_ref, PC_refNB) <+ 0.0;
   V(PU_ref, PU_refNB) <+ 0.0;
   V(PD_ref, PD_refNB) <+ 0.0;
```



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Analog Components of a Channel

Transmission Lines

Via Holes

High Speed Connectors

Package

I/O – IBIS models and Transistor level models

DSP Components in a Channel

Decision Feedback Equalizer

Feed Forward Equalizer

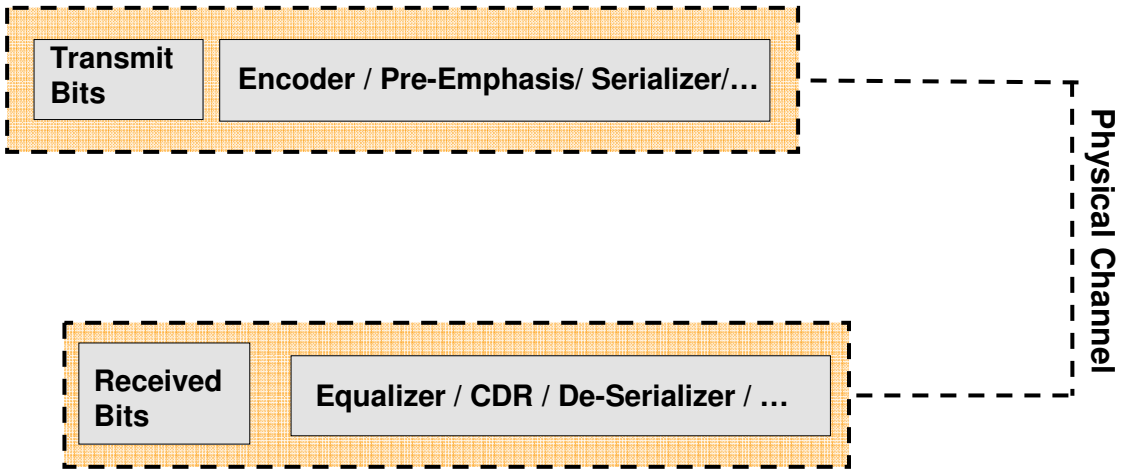
Clock and Data Recovery

Gain Controls

SERDES Models

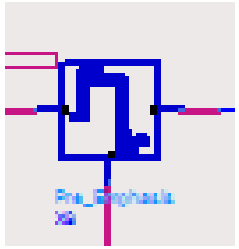
Can I mix DSP and ANALOG models in a single simulation?

Modeling Pre-emphasis and Equalization

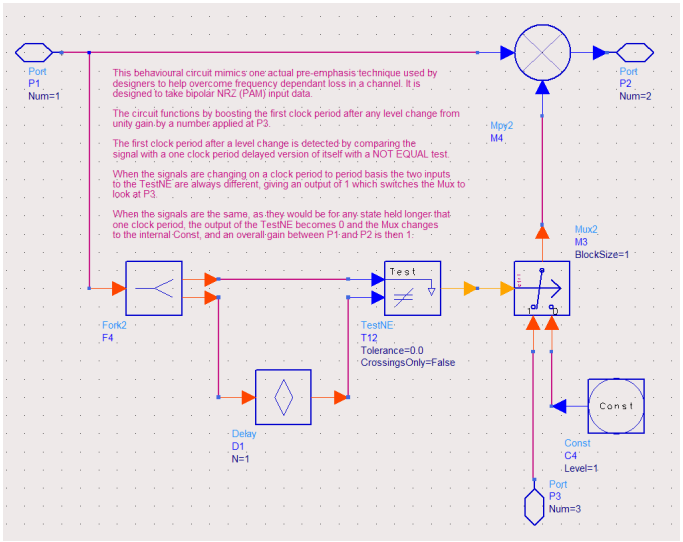


DSP components can be represented in different ways: C/C++, System C, MATLAB, HDL

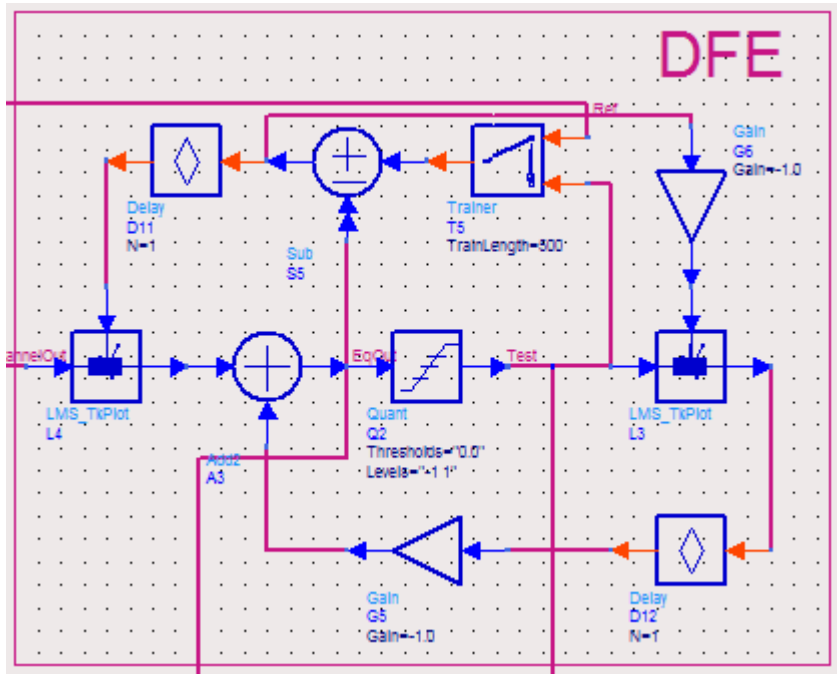
DSP Behavioral Models



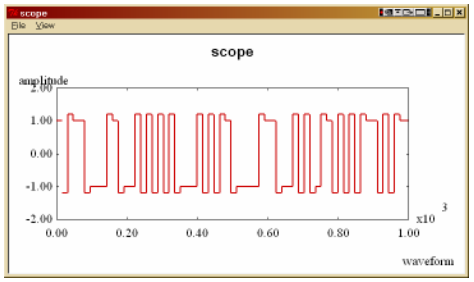
Pre-Emphasis

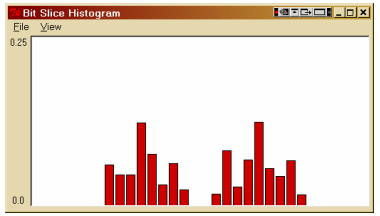


Equalization



DSP and ANALOG co-simulation





PTOLEMY-SPICE CO-SIM SI CHANNEL WITH TX PRE-EMPHASIS AND RX EQUALIZATION

(Using the "drive_lines" channel example)

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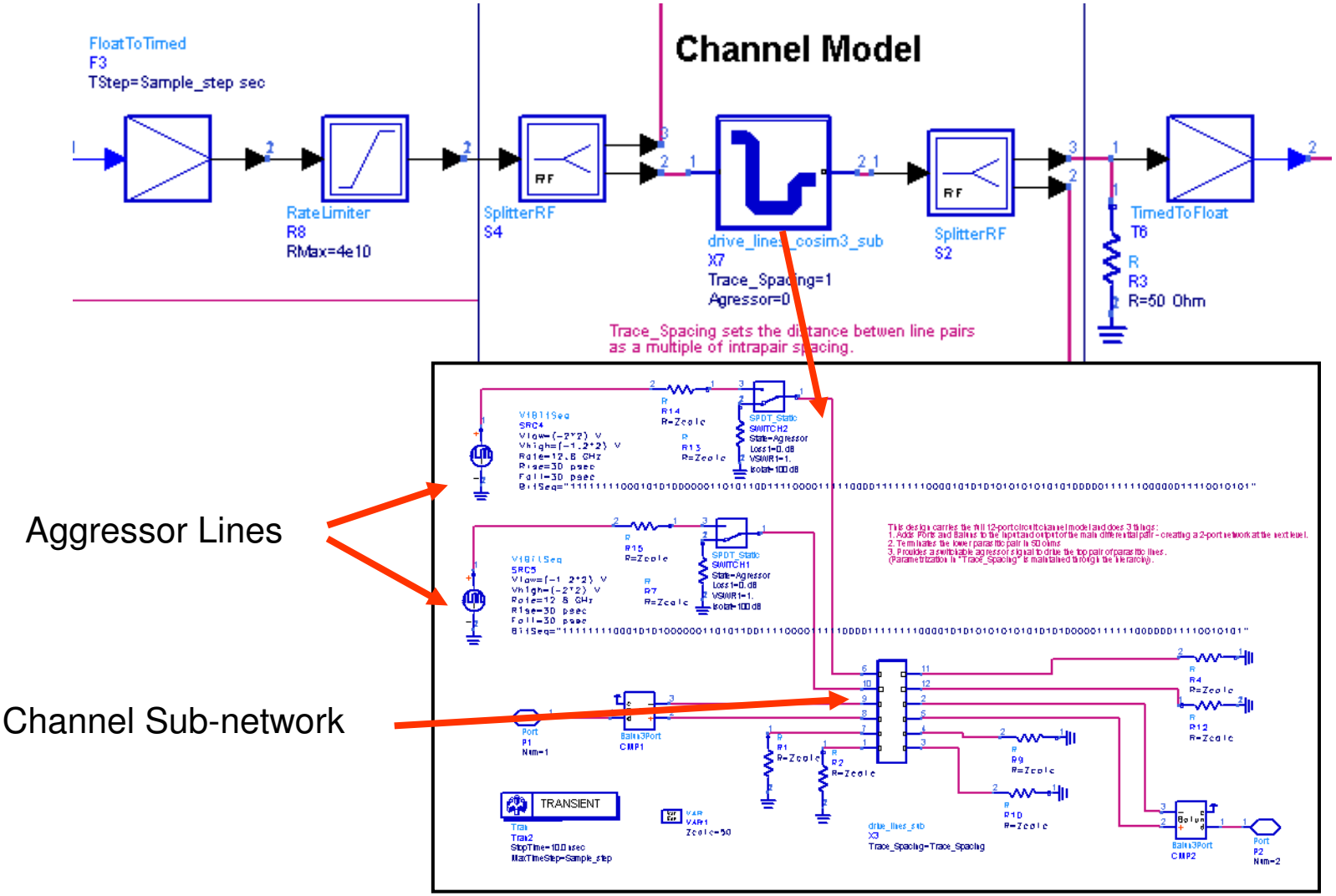
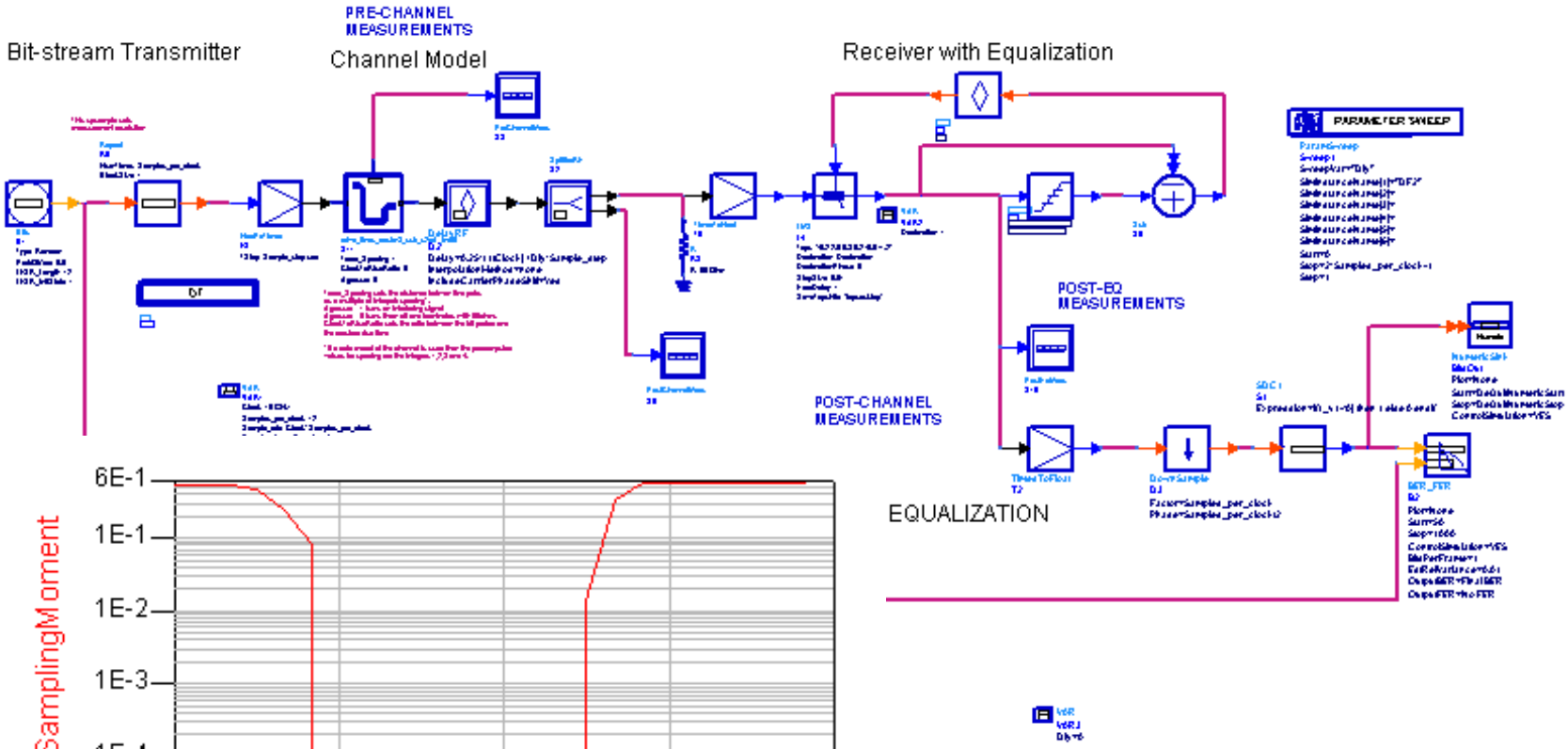
Channel Model



Bit Error Ratio Simulation



BER as a function of sampling position