Size Matters – Recent Experiences with IBIS Files
Size/Complexity Evolution and Implications for Model Users and EDA Tools

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Preface

1. This is NOT one if these *in the good old days* presentation.

2. We like to share experiences and observation we made in the last 12 months which make model usage for the people in the CAD departments (which are often not IBIS experts) more difficult.

3. This is meant as a proposal for discussion between model makers, tool vendors and model users.

4. Of course we recognize technology evolution and that modern high sophisticated and complex silicon defines serious challenges to the model makes (and the model users)!
Looking overall, IBIS environment is very well accepted (that's what we hope to achieve in the early 90ies...)
IBIS in the beginning has been defined when we had rather simple devices:

- SOP and PLCC packages, few models, simple RLC packages
- Lateron processor models, more complex packages
- DIMM modules as EBDs with IBIS 3.x
IBIS Data Usage in today's EDA Tools

- EDA Tools either read IBIS at runtime or they convert into own model formats (ako import and conversion process) or instantiate such models (i.e. HSPICE).

- When using the golden parser (to some extend most EDA tools utilize it) IBIS relevant data structures are created → huge operations in memory will take place.
The Problem (1): IBIS file sizes explode

- Some recent samples:
  - Altera Stratix III:
    - 68.1 MB file size
    - 2359 (generic) pins, 7077 model PLUS model selector variants (OCT variation)
    - Passed IBISCHK (2 minutes on a fast PC), but some IBIS freeware (editor) have problems
    - For the end user excellent XLS documentations allows model selection (but: manual process, error prone)
  - Lattice sc2.ibis
    - More than 80 MB
    - 2163 (generic) pins
    - 'Very 'special' model naming scheme
The Problem (2): Use of Model Selector Statements get a massive Commodity

- Up to 30 model selectors in some cases, problem often not direct visible to model users
  - Micron/Samsung EBDs
  - FPGAs

```
{Model Selector} DQ
DQ_FULL_533   Full-Strength IO Driver with no ODT
DQ_FULL_ODT50_533 Full-Strength IO Driver with 50 Ohm ODT Submodel
DQ_FULL_ODT75_533 Full-Strength IO Driver with 75 Ohm ODT Submodel
DQ_FULL_ODT150_533 Full-Strength IO Driver with 150 Ohm ODT Submodel
DQ_HALF_533   Reduced-Strength IO Driver with no ODT
DQ_HALF_ODT50_533 Reduced-Strength IO Driver with 50 Ohm ODT Submodel
DQ_HALF_ODT75_533 Reduced-Strength IO Driver with 75 Ohm ODT Submodel
DQ_HALF_ODT150_533 Reduced-Strength IO Driver with 150 Ohm ODT Submodel
DQ_FULL_800   Full-Strength IO Driver with no ODT
DQ_FULL_ODT50_800 Full-Strength IO Driver with 50 Ohm ODT Submodel
DQ_FULL_ODT75_800 Full-Strength IO Driver with 75 Ohm ODT Submodel
DQ_FULL_ODT150_800 Full-Strength IO Driver with 150 Ohm ODT Submodel
DQ_HALF_800   Reduced-Strength IO Driver with no ODT
DQ_HALF_ODT50_800 Reduced-Strength IO Driver with 50 Ohm ODT Submodel
DQ_HALF_ODT75_800 Reduced-Strength IO Driver with 75 Ohm ODT Submodel
DQ_HALF_ODT150_800 Reduced-Strength IO Driver with 150 Ohm ODT Submodel
```
The Problem (3): Splitted IBIS files, Separate package
(here large processor model)

Hand Work needed !!!
Observations

- New devices are often modeled by really HUGE IBIS device descriptions with thousands of models.
- New memory modules utilize heavily EBDs (the renaissance of the EBDs, caused by DDRs modules).
- Package models often missing, or implicit set to zero and external package model is referred in SPICE or S-Parameters syntheax → often further handwork.

⇒ IBIS gets less handy for model users (then intended ?)
Conclusion

• The recent development on (some) IBIS device descriptions makes the model usage, especially for less experienced users, more complicated.
• Tools can still handle such devices, but if this development continues, IBIS data handling can become challenging.
• Handwork will lower down the convenience and acceptance in using IBIS and therefore may harm the progress of the standard.