Standard Power Integrity Model (SPIM) and Unified PI Target (UPIT)

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Kinger Cai has been driving I+I strategy for Notebook platforms, and strategic PI design tool evolution in Client Computing Group. Kinger was awarded Ph. D by Shanghai Jiao Tong University in 2001, and MBA degree by W.P. Carey business school in 2008. Kinger works in signal & power integrity domains for 20+ years. Kinger published 30+ papers and holds 7 granted patents.
Agenda

• Industry Platform PI Design Challenges
• Platform PI design Architecture Standardization
  • FastPI – Platform PI design Framework
  • SPIM – Standard Power Integrity Model
  • UPIT – Unified PI design Target
• SPIM with UPIT in FastPI Status Update
• IBIS BIRD Draft Example
• Call to Actions
Platform PI design: Beyond Conventional Methodology

- More flexibility, besides copy exactly from reference design with platform design guideline
- Effective platform PDN optimization, more than what-if simulation
- Efficient platform PI design review and sign-off process
Platform PI design: Collateral, Architecture and Tools

- PI design collateral: Chip vendors to platforms designers
  - Minimal and standardized
  - Sufficient, while IP protected
  - Flexibility, while accuracy guaranteed

- PI design Architecture, Framework and Tool
  - Standard architecture
  - Flexible framework
  - Efficient tool
Platform PI design: FastPI with SPIM and UPIT

FastPI - Platform PI design standard

Package

Board

- **SPIM:** Standardized PI Model, for each power rail in SoC/PKG, to customers
- **UPIT:** Unified PI design Target, an impedance target for each power rail
- **FastPI:** Platform PI design standard, to integrate with industry leading EDA

FastPI supports chip suppliers, EDA vendors and platform designers, with SPIM and UPIT.
Platform PI Design: SPIM- Standard Power Integrity Model

- **SPIM**: Standardized PI Model, for each power rail in SoC/PKG, to customers
- **UPIT**: Unified PI design Target, an impedance target for each power rail
- **FastPI**: Platform PI design standard, to integrate with industry leading EDA
Platform PI Design: SPIM with UPIT (Unified PI Target)

VRM  
L_{b\text{ulk}}  
C_{b\text{ulk}}  
MLCC  
MLCC  
SPIM  
Solder Ball or Socket

Platform Level PI Design

SPIM

VRM Equivalent

Node_E

L_{b\text{ulk}}

Node_D

ict_3

Node_f

S parameter model Node_f

VRM Equivalent

Node_D

ict_3

Node_f

S parameter model Node_f

Node_f

S parameter model Node_f

L_{b\text{ulk}}

R_{b\text{ulk}}

Solder Ball

Solder Ball

C_{b\text{ulk}}

C_{b\text{ulk}}

Solder Ball

Solder Ball

SPIM

Unified PI Target (UPIT)

DC to ~10s MHz

Zone-3  Zone-2  Zone-1

\text{Z(f) Full PDN}
\text{Z(f) excluding die}
\text{z(f) excluding PKG}

\text{PI design Target}
SPIM- Standardized Power Integrity Model

- **Standardized PI model**
  - S parameter, BGA/pin to bump, and Caps
  - Weighted/normalized AC source
  - Impedance target, at observation port
  - Pin(/BGA) awareness

- **Usage model**
  - Directly merged as a virtual PKG database, with physical BRD database
  - Backwards compatible to SPICE simulator
  - IP information protection

- **Development**
  - Promote as industry standard
  - Adopted by major EDA tools
  - Scalable UPIT included

SPIM for platform PI design, while IBIS for platform SI design.
FastPI PI Design Target Definition

• Impedance at Sense Port_S

  - \([S_{pdn}] \Rightarrow [Z_{pdn}], \text{ in FastPI}\)
  - \([V] = [Z_{pdn}][I]\)
  - \([V] = [v_1, v_2, ..., v_N, v_S]^T\)
  - \([I] = [w_1, w_2, ..., w_N, 0]^T\)
  - \(\sum_{i=1}^{N} w_i = 1\), weighted normalization
  - \(Z_S = V_S = \sum_{i=1}^{N+1} (Z_{pdn}(N + 1)_i \times w_i)\)
  - \(Z_S = \sum_{i=1}^{N} (Z_{pdn}(N)_i \times w_i)\)

Impedance target is generally defined at sensing/feedback port.
**UPIT - Unified Power Integrity (design) Target**

- **Extended to cover PD**
  - Conventionally PI covers >1MHz
  - Traditionally PD target defined in TD
  - Unified PD Target in FD

- **Expanded to IO Power rails**
  - Started for computing rails
  - Expanded as Z target, to IO power rails
  - Extrapolated from time domain

- **Correlation for UPIT**
  - Correlated in frequency domain
  - SPIM vs. conventional SPICE
  - Pre-Si simulation vs. Post-Si measurement

*UPIT with SPIM has been well correlated with conventional SPICE, as well as post-Si measurement.*
Platform PI Design: SPIM with UPIT in FastPI

- SPIM and UPIT has become one of the standard PI collaterals
- FastPI has been fully supported by two leading EDA vendors
- Proposing to make it 1st PI standard in the industry
### IBIS BIRD Draft Example, for SPIM with UPIT included in IBIS

<table>
<thead>
<tr>
<th>SPIM 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>[SPIM] SPIM-1</td>
</tr>
<tr>
<td>VCC_Net VCC1</td>
</tr>
<tr>
<td>VSS_Net VSS</td>
</tr>
<tr>
<td>[Port Group]</td>
</tr>
<tr>
<td>A1_1</td>
</tr>
<tr>
<td>VCC1</td>
</tr>
<tr>
<td>VSS</td>
</tr>
<tr>
<td>A1_2</td>
</tr>
<tr>
<td>VCC1</td>
</tr>
<tr>
<td>VSS</td>
</tr>
<tr>
<td>A1_3</td>
</tr>
<tr>
<td>VCC1</td>
</tr>
<tr>
<td>VSS</td>
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<tr>
<td>A1_4</td>
</tr>
<tr>
<td>VCC1</td>
</tr>
<tr>
<td>VSS</td>
</tr>
<tr>
<td>...</td>
</tr>
</tbody>
</table>

| U1_1 |
| VCC1 | 2082 2207 |
| VSS | 2179 2180 |

| U1_2 |
| VCC1 | 2085 2210 |
| VSS | 2182 2183 |

...  

[SnP Model] SnP_model_1  
[Snp File Name] Icelake_VCC1_PKG.s58p  
[END SnP Model]  

[UPIT] UPIT-1  
[OB Port] OB_VCC1  
[S1P File Name] Icelake_VCC1_OB_TargetZ.s1p  
[END UPIT]  

[END SPIM]  

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Call to Action:

• Call to form a platform PI design standardization WG
• Call chip vendors to support FastPI architecture
• Call EDA vendors to support FastPI framework
• Call platform designers to adopt SPIM and UPIT
• Call to submit IBIS BIRD for SPIM with UPIT
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