IBIS Based Behavior Modeling for Current Mode Buck Converter

Anfeng Huang, Jingdong Sun, Hongseok Kim, Jun Fan, Chulsoon Hwang

Missouri S&T EMC Laboratory

Zhiping Yang, Yimajing Yan, Hanfeng Wang, Songping Wu, Shuai Jin, Zhenxue Xu

Google

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Objective

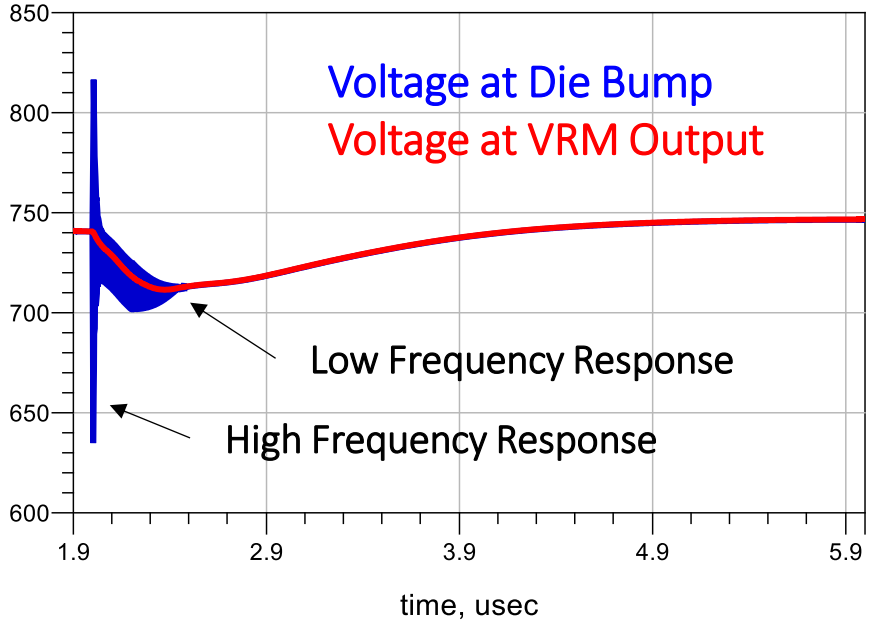
- System-Level Power simulation Coverage
  - **DC simulations**, including IR drop;
  - **Transient response**, i.e. transient power noise;
  - AC simulations, i.e. PDN impedance;
  - System power consumption and efficiency;
  - Power/thermal co-simulation

Outline

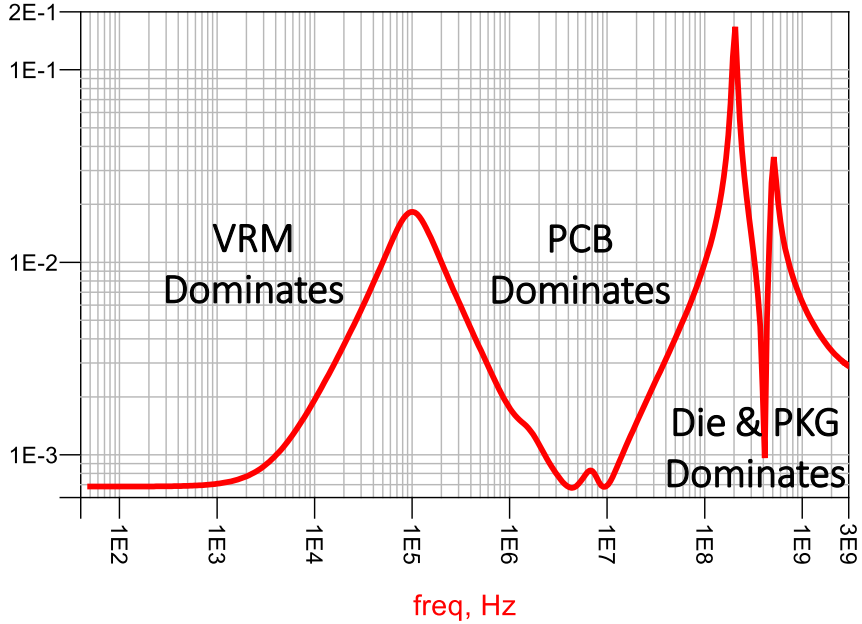
- Background
  - Influence of voltage regulator module (VRM) on the power distribution network (PDN) design.
  - Introduction to current mode buck converter
- Proposed IBIS Model for Current Mode Buck Converter
- Validation
- Conclusion and future work
- Acknowledgement

Time / Frequency Domains Comparison

- VR model is required to capture the low frequency response during switching.
- The SI related performances e.g. eye-diagram could not be accurately simulated if the power line noise is neglected.



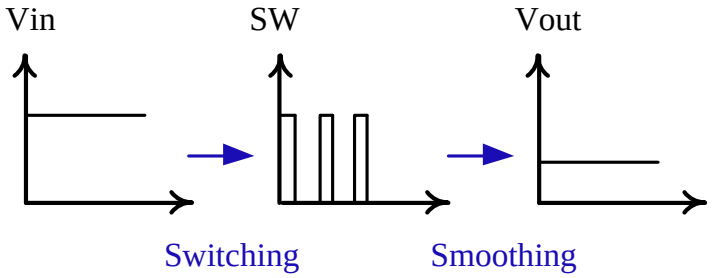
Time Domain – Voltage Droop

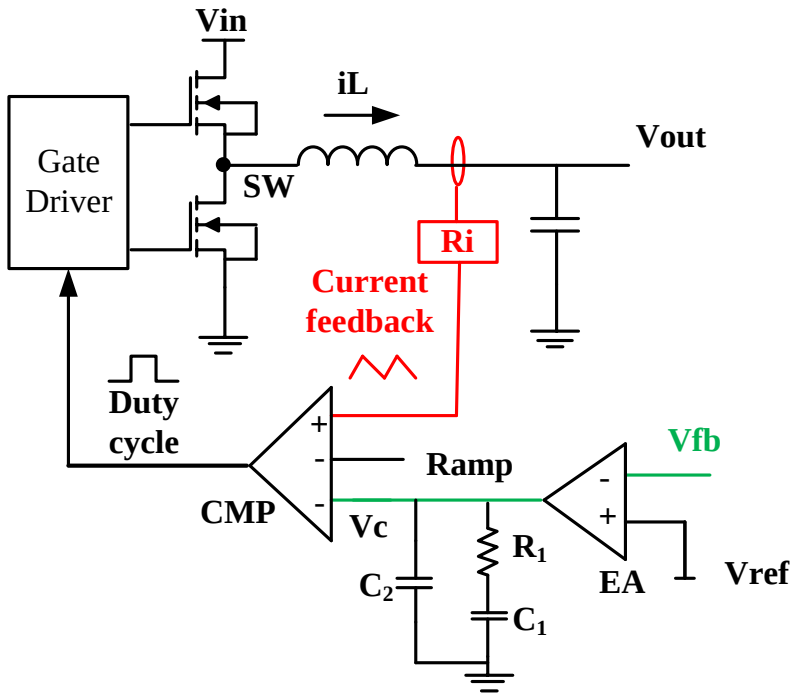


Frequency Domain – Impedance

Introduction to Current Mode Buck Converter

- Current mode buck converter
  - Current information is used in feedback controller.
- Influence of feedback control loop
  - Steady state output variance under different input and loading conditions;
  - Voltage droop and recovery time.
- Method of control
  - PWM (Pulse width modulation) control;
  - PFM (Pulse frequency modulation) control.





Outline

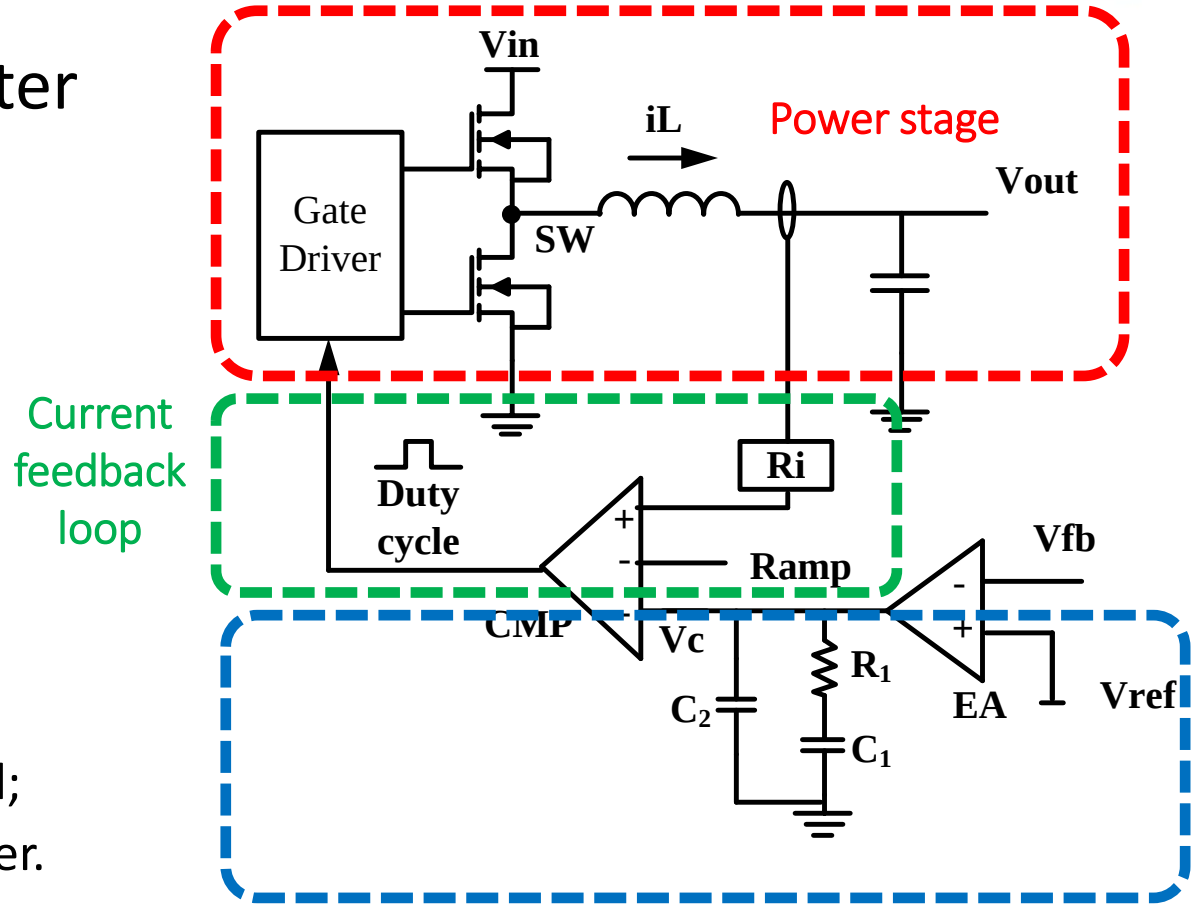
- Background
- Proposed IBIS Model for Current Mode Buck Converter
  - Modeling Method
  - Summary of key parameters and equations in proposed model
  - Discussion
- Validation
- Future work

Existing Modeling Method and Proposal

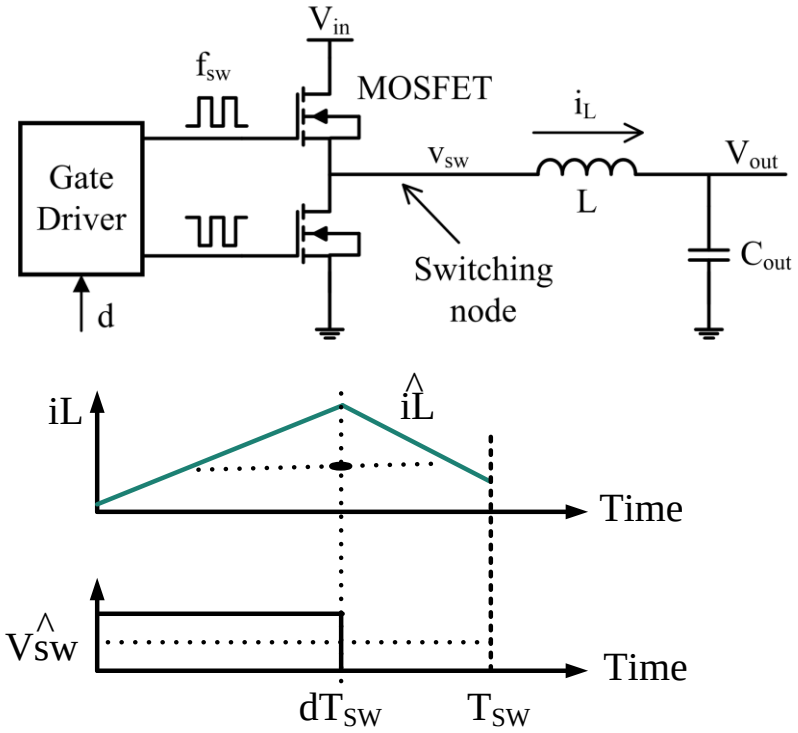
- Existing modeling method:
  - VRM device model directly provided by the vendor, typically encrypted because of the IP concerns;
  - Limitations:
    - Not compatible with IBIS simulator;
    - Simulation speed and convergence concerns exist due to switching nature.
- Proposal:
  - Equation based averaged model with same behavior;
  - Advantages:
    - Equivalent transfer function other than exact circuit implementation is provided in the model (naturally encrypted);
    - Much faster than ordinary model with switching behavior.

Modeling Methodology for Buck Converter

- Analytical equation for power converter
  - Focusing on the averaged behavior;
  - PWM control buck is used for demonstration.
- Sub-circuit blocks
  - Power Stage
  - Current feedback Loop
    - Only continuous current mode is supported;
    - Need modification to support PFM controller.
  - Voltage feedback Loop



Power Stage



$$\hat{V_{SW}} = d(V_{in} - r_{on,H}\hat{i_L}) - (1-d)r_{on,L}\hat{i_L}$$

$$V_{out} = \hat{V_{SW}} - r_L\hat{i_L}$$

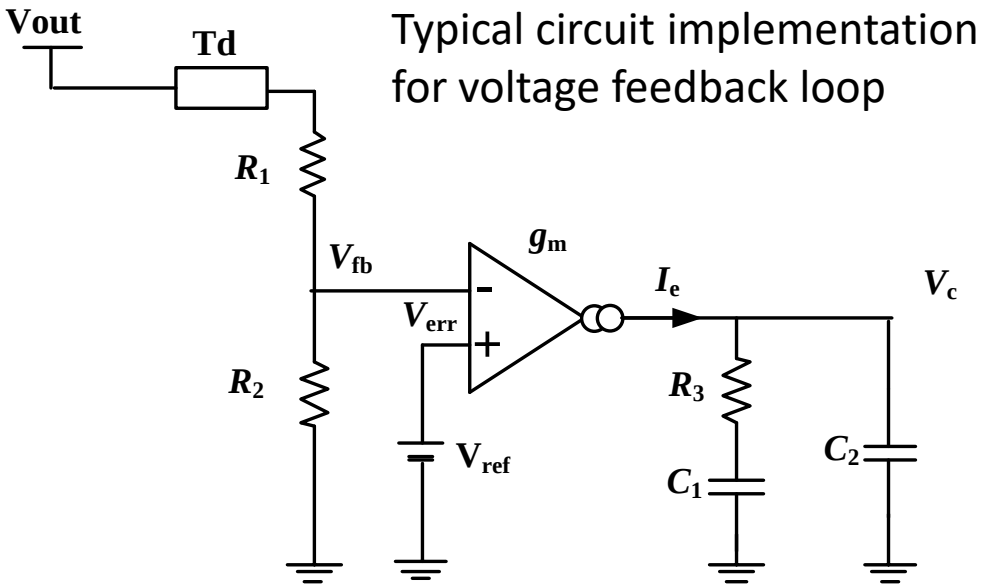
- Parameters definition
  - $\hat{i_L}$: averaged inductor current.
  - f_{SW}: switching frequency
  - d: the duty cycle.
  - $\hat{V_{SW}}$:averaged voltage on switching node.
  - r_L, L : ESR and inductance of inductor.
  - C_{out}: capacitance of capacitor.
  - $r_{on,H}, r_{on,L}$: On resistance of high and low side MOSFETs.
  - V_{in}: Input Voltage.

Note :
Key parameters of proposed IBIS model are marked in red;

Only consider the loss caused by on resistance of MOSFETs and inductor. Loss of capacitor is relatively small and could be neglected.

Voltage Feedback Loop

- Parameters definition in typical circuit implementation
  - V_{fb}: feedback voltage calculated from V_{out}.
  - V_{ref}: internal reference voltage.
  - g_m: transconductance of error amplifier.
  - R_1, R_2: Resistive divider network.
  - $R_3, C_1, C_2,$: compensation circuits.
  - V_c: compensated voltage from error amplifier.
  - T_d : control delay due to remote sensing



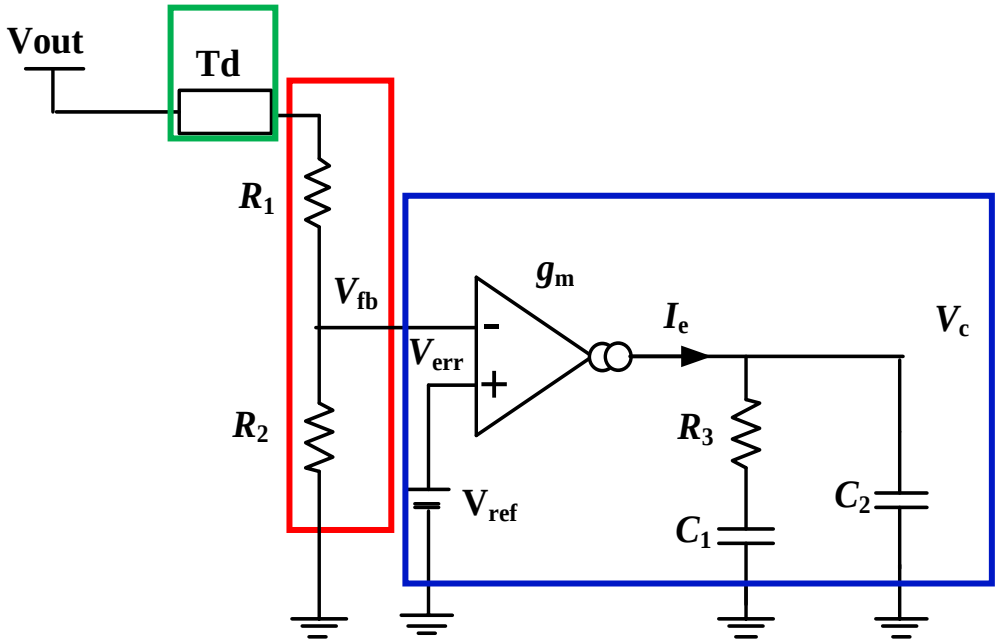
Typical circuit implementation for voltage feedback loop

The transfer function of the voltage feedback circuit could be calculated as:

$$V_{err} = V_{ref} - \frac{R_1}{R_1 + R_2} V_{out} \times e^{-sT_d}$$

$$\frac{V_c}{V_{err}} = -g_m \times \frac{1 + R_3 C_1 s}{(C_1 + C_2)s + R_3 C_2 C_1 s^2}$$

Voltage Control Loop – Transfer Function



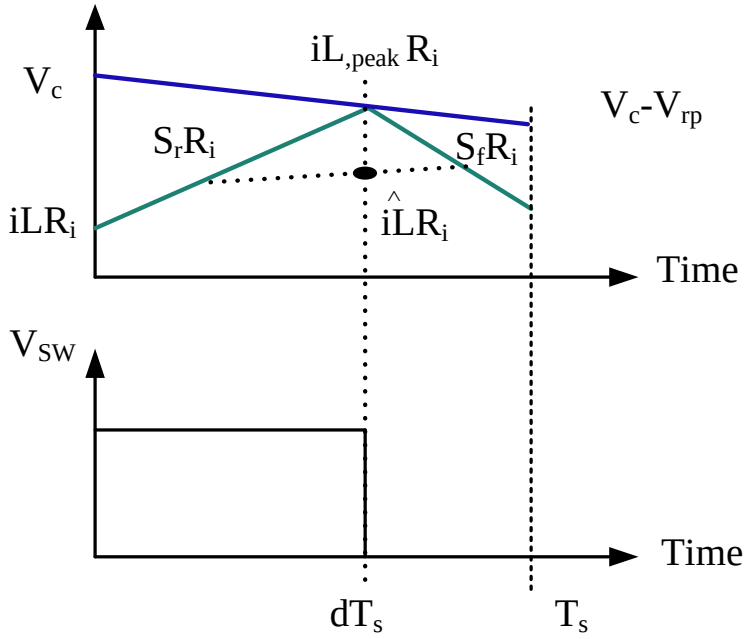
Different types of compensators are supported by specifying multiple zeros and poles.

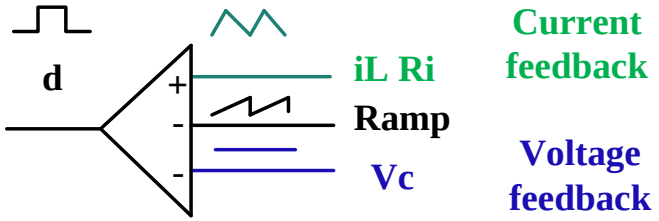
- Parameters definition in proposed IBIS model
  - T_d : control delay due to remote sensing.
  - V_{ref}: internal reference voltage.
  - K_{div}: dividing ratio of resistive network.
  - K_{dc}: dc gain of error amplifier.
  - ω_{zn}: frequency of nth zero.
  - ω_{pn}: frequency of nth pole.

$$V_{err} = V_{ref} - V_{out} \times K_{div} \times e^{-sT_d}$$

$$\frac{V_c}{V_{err}} = -K_{dc} \times \frac{s - \omega_z}{(s - \omega_{p1})(s - \omega_{p2})}$$

Current Feedback Loop (CCM)





- Parameters Definition
  - $\widehat{i_L}$: averaged inductor current.
  - R_i: total current sensing gain.
  - V_{rp}: ramp voltage for compensation.
  - S_r, S_f: rising and falling slopes of i_L.
  - T_s: switching period time.
  - d: the duty cycle.

$$S_r = \frac{V_{in} - \widehat{i_L}(r_{on,H} + r_L) - V_{out}}{L},$$

$$S_f = \frac{-\widehat{i_L}(r_{on,L} + r_L) - V_{out}}{L},$$

$$\Delta S \triangleq S_r - S_f,$$

$$d = \frac{1}{2} + \frac{V_{rp}}{T_s \Delta S R_i} - \sqrt{\left(\frac{1}{2} + \frac{V_{rp}}{T_s \Delta S R_i}\right) - \frac{2}{T_s \Delta S}\left(\frac{V_c}{R_i} - \hat{i_L}\right)}$$

Note : Key parameters of proposed IBIS model are marked in red;

Discussion

- The proposal is valid only for current mode buck converter
  - The structure of control circuit should be known to build the average model;
  - The proposal could be extended to support other controllers.

- Only PWM controller is discussed, but the model could be easily modified for PFM controller.
  - Substitute $d = \frac{T_{on}}{T_{sw}}$ into previous equations;
  - The equations for PFM controller could be found in backup slides.

Summary of Key Parameters

Device physical parameters (from vendor)

Type of controller:

- PWM or PFM

Power stage:

- On resistance of high and low side MOEFETs: $r_{on,H}, r_{on,L}$

Voltage feedback loop:

- Internal reference voltage: V_{ref}
- DC gain of error amplifier : K_{dc}
- Frequency of nth zero : ω_{zn}
- Frequency of nth pole: ω_{pn}

Current feedback loop:

- total current sensing gain : R_i
- ramp voltage for compensation : V_{rp}

System controlled parameters (from designer)

- Input voltage : V_{in}
- Output current profile: I_{Load}
- Switching frequency : f_{SW}
- control delay due to remote sensing: T_d

Optional parameters (from vendor or designer)

- Dividing ratio of resistive network: K_{div}
- Output inductance: L
- ESR of output inductor: r_L
- Output capacitor: C_{out}

Summary of Equations

Power stage

$$\hat{V_{SW}} = d(V_{in} - r_{on,H}\hat{i_L}) - (1-d)r_{on,L}\hat{i_L}$$

$$V_{out} = \hat{V_{SW}} - r_L\hat{i_L}$$

Voltage feedback loop

$$V_{err} = V_{ref} - V_{out} \times K_{div} \times e^{-sT_d}$$

$$\frac{V_c}{V_{err}} = -K_{dc} \times \frac{s - \omega_z}{(s - \omega_{p1})(s - \omega_{p2})}$$

Current feedback loop

$$S_r = \frac{V_{in} - \hat{i_L}(r_{on,H} + r_L) - V_{out}}{L}, \qquad \Delta S \triangleq S_r - S_f,$$

$$S_f = \frac{-\hat{i_L}(r_{on,L} + r_L) - V_{out}}{L},$$

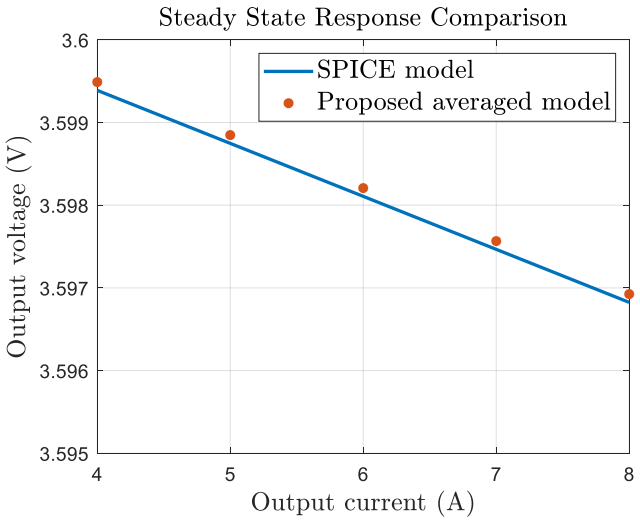
$$d = \frac{1}{2} + \frac{V_{rp}}{T_s \Delta S R_i} - \sqrt{(\frac{1}{2} + \frac{V_{rp}}{T_s \Delta S R_i}) - \frac{2}{T_s \Delta S}(\frac{V_c}{R_i} - \hat{i_L})}$$

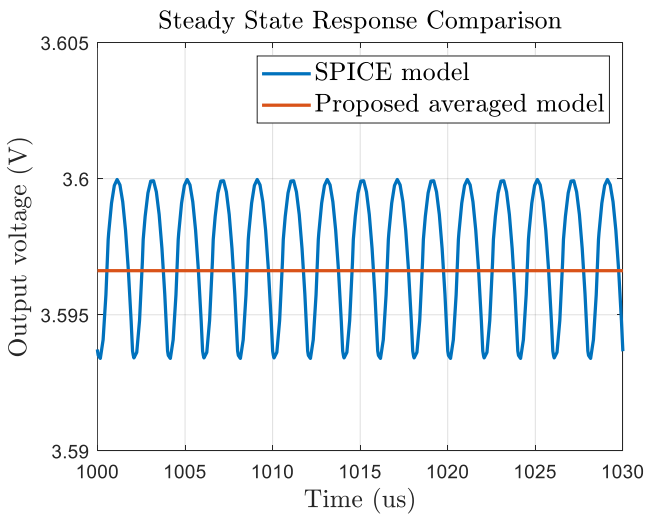
The current mode buck converter could be well-modeled with combination of equations and circuit elements (inductor and capacitors).

Outline

- Background
- Proposed IBIS Model for Current Mode Buck Converter
- Validation
- Future work

Example: Steady State Output Voltage (PWM)



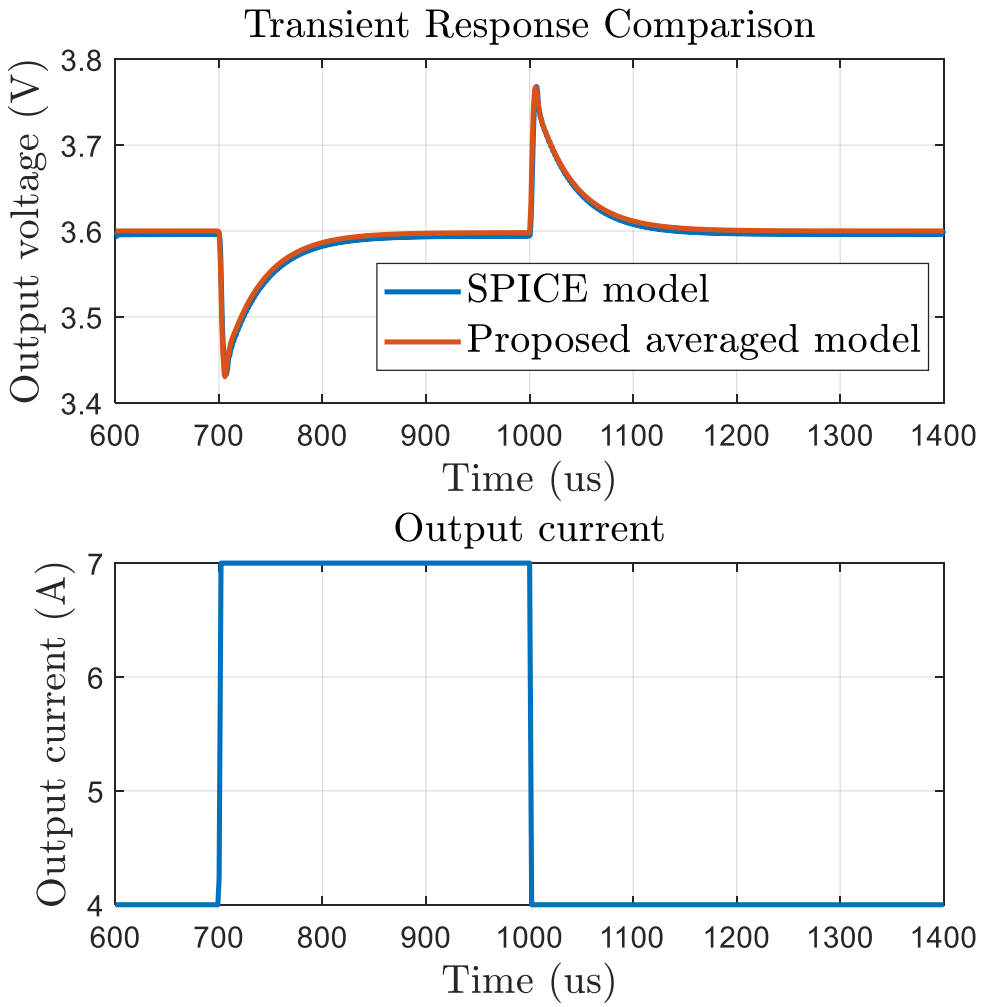


- The simulation results are compared with results obtained from SPICE model with real switching behavior.
  - Left: averaged output voltage vs. output current;
  - Right: waveforms of output voltage (The proposed model is an averaged model).
- Good agreement is achieved.

Device Parameters		Value	System Parameters	Value
Control	Mode	PWM	V_{in}	12 V
Power stage	$r_{on,H}$	8.2 mohm	I_{Load}	4 A
	$r_{on,L}$	5.5 mohm	K_{div}	0.25
Voltage feedback loop	V_{ref}	0.9 V	f_{SW}	500 kHz
	K_{dc}	625	L	5 uH
	ω_{z1}	4.3 kHz	r_L	3 mOhm
	ω_{p1}	49.3 Hz	C_{out}	44 uF
	ω_{p2}	180 kHz	T_d	10 ns
Current feedback loop	R_i	0.1		
	V_{rp}	20 mV		

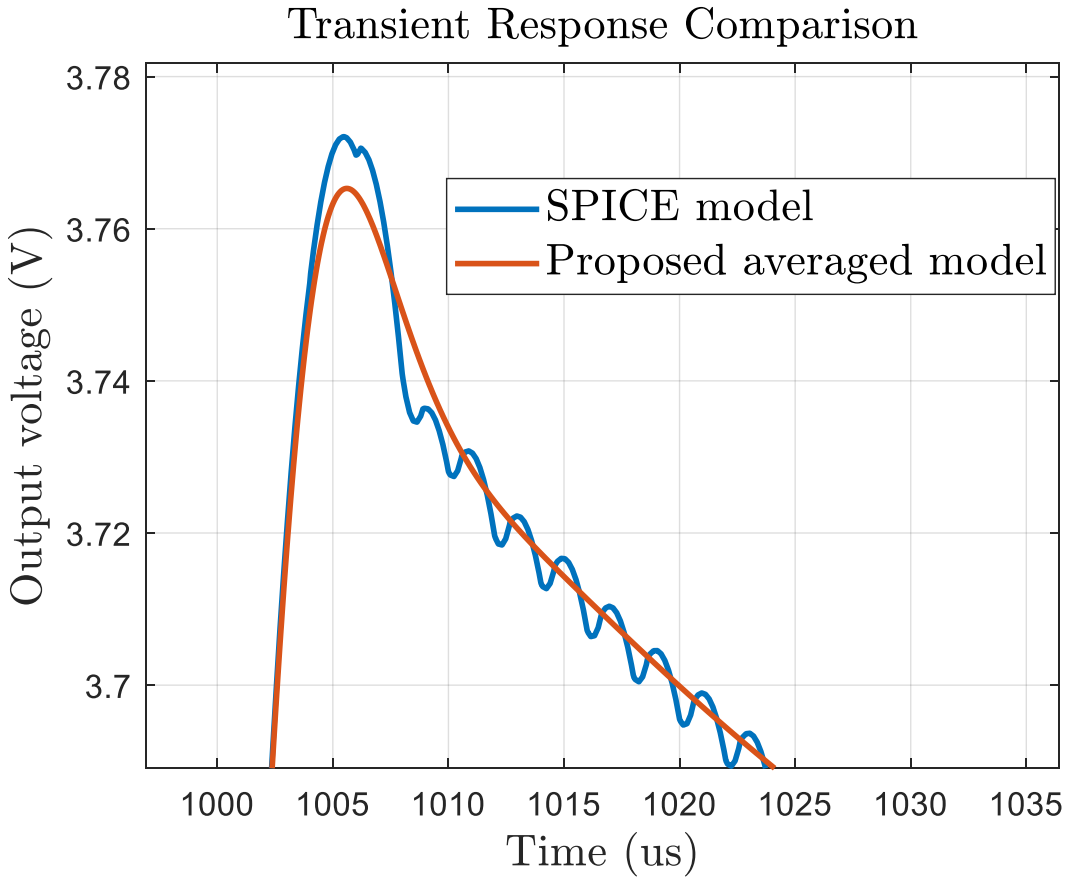
Example: Transient Output Voltage (PWM)

- The transient responses are also compared:
  - Rising edge: 4A->7A , rise time: 2us
  - Falling edge: 7A->4A, fall time: 2us
- The voltage drop generated during load transient could be accurately captured by the average model:
  - Rising edge: $\Delta V = 4.8\text{mV}$
  - falling edge: $\Delta V = 4.3\text{mV}$

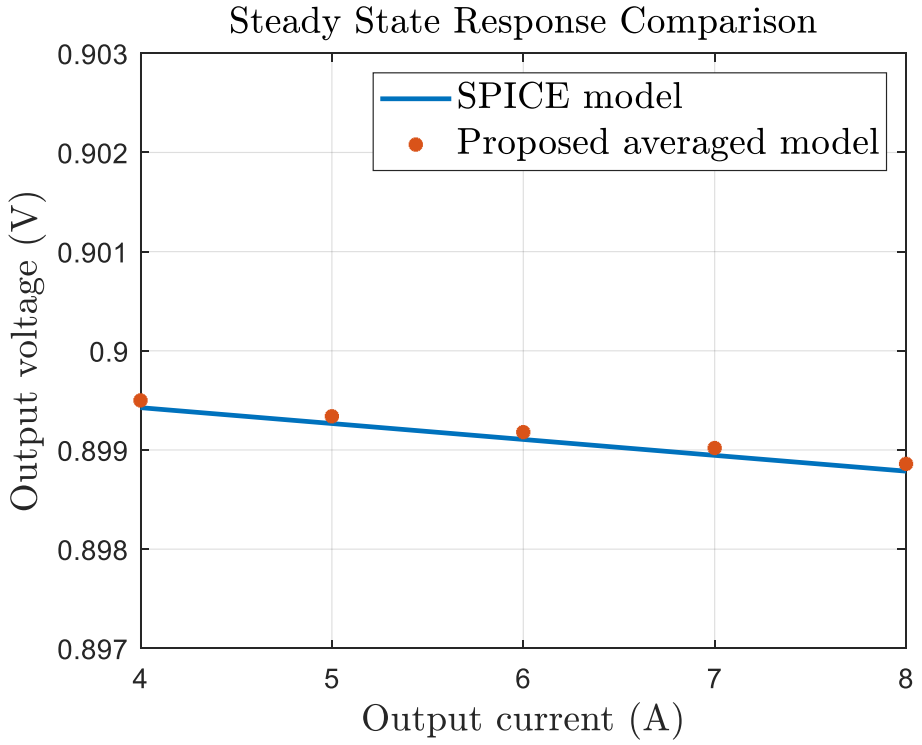


Example: Transient Output Voltage (PWM)

- The zoomed in results are demonstrated for further explanation;
  - The rise time of output voltage is well matched.
- The relatively large difference is due ripples generated by switching.
  - Smaller voltage difference would be observed if the SPICE simulation results are filtered.



Example: Steady State Output Voltage (PFM)

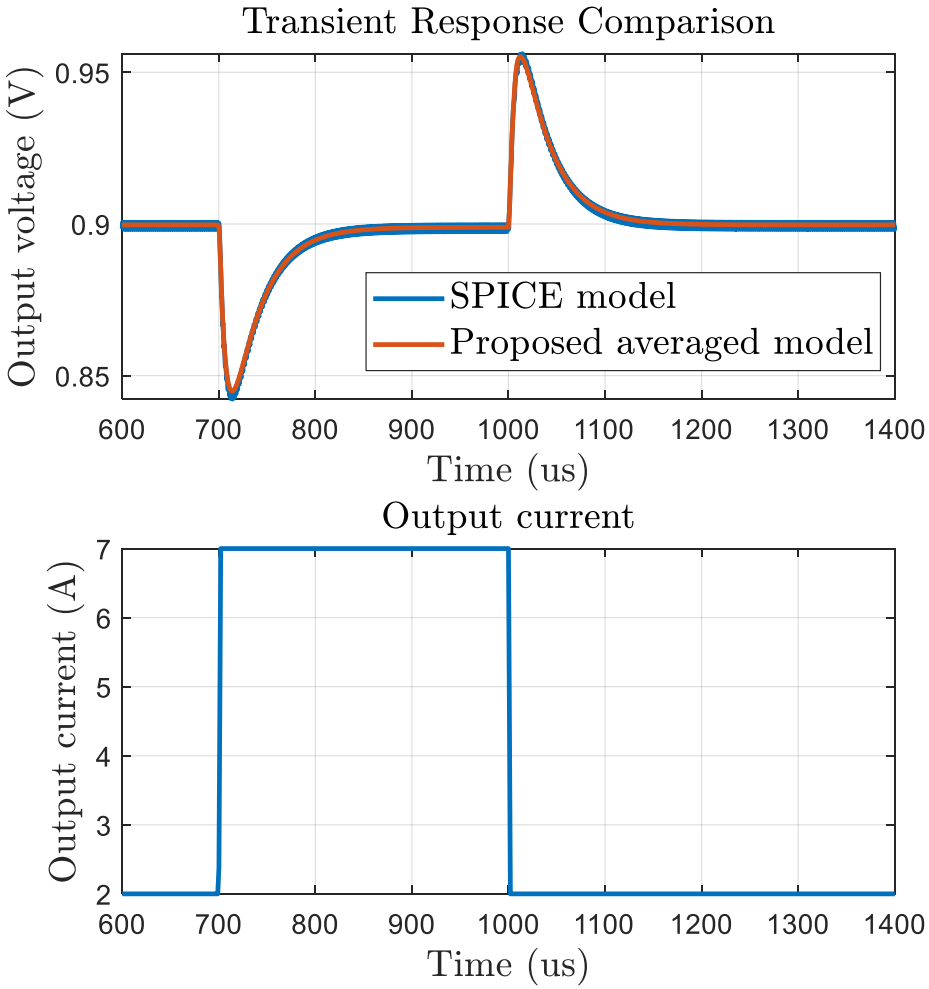


- The simulation results are also well matched.

Device Parameters		Value	System Parameters	Value
Control	Mode	PFM	V_{in}	12 V
Power stage	$r_{on,H}$	10 mohm	I_{Load}	4 A
	$r_{on,L}$	10 mohm	K_{div}	1
Voltage feedback loop	V_{ref}	0.9 V	f_{SW}	400 kHz
	K_{dc}	625	L	800 nH
	ω_{z1}	4.3 kHz	r_L	1 mOhm
	ω_{p1}	49.3 Hz	C_{out}	440 uF
	ω_{p2}	180 kHz	T_d	15 ns
Current feedback loop	R_i	0.1		
	V_{rp}	30 mV		

Example: Transient Output Voltage (PFM)

- The transient responses are also compared:
  - Rising edge: 2A->7A , rise time: 2us
  - Falling edge: 7A->2A, fall time: 2us
- The voltage drop generated during load transient could be accurately captured by the average model:
  - Rising edge: $\Delta V = 3.4\text{mV}$
  - falling edge: $\Delta V = 4.1\text{mV}$



Simulation Speed Comparison

- One of the advantage of the proposed model is simulation speed.
  - Stop time: 2ms

Simulator	Features	Type of model	Maximum time step	Elapsed time
Simplis	Does not support S-parameters block and IBIS model	PWM (SPICE)	N/A	4 s
		PFM (SPICE)	N/A	4 s
ADS	ADS presently supports the IBIS 4.2 specification	PWM(SPICE)	10 ns	21 s
		PFM(SPICE)	10 ns	45 s
		PWM (Proposed)	10 ns	3.3 s
		PFM (Proposed)	10 ns	4.6 s

Conclusion and Future Work

- The waveforms of averaged model are well matched with SPICE model.
- The proposed model can be used to evaluate the steady state and transient response of buck converter.

- Future work
  - Discontinuous current mode operation;
  - AC simulations, i.e. PDN impedance
  - Include loss simulation capability (DC loss and switching loss)
    - Ref: IBIS based buck converter dc modeling (DesignCon IBIS Summit Santa Clara, California January 31, 2020)

Acknowledgement

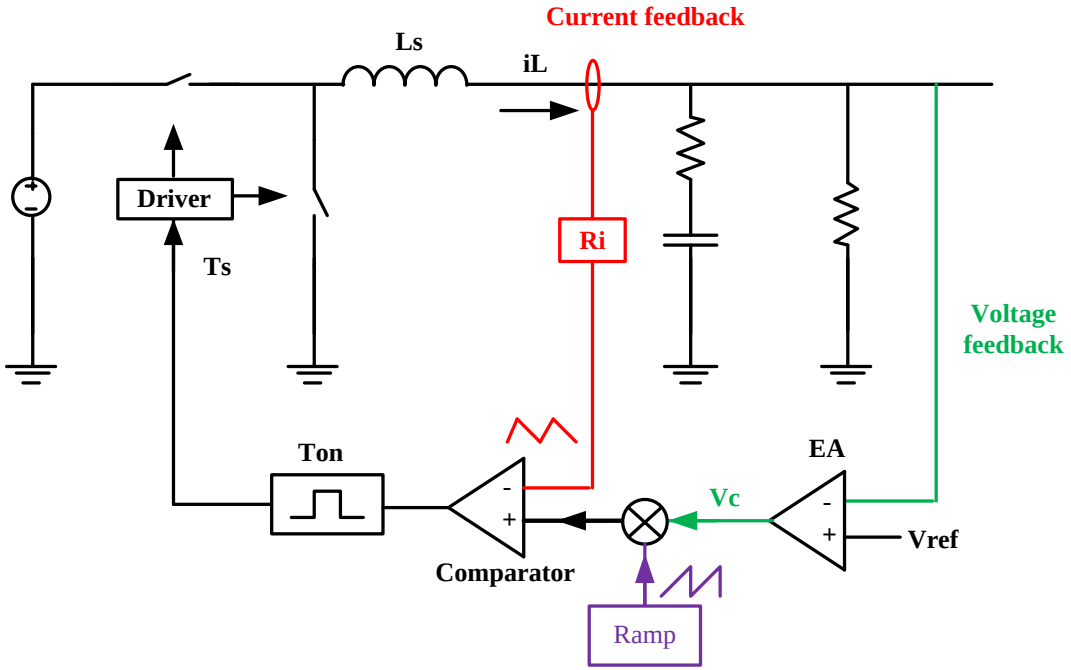
- The modeling for PWM based buck converter is originally published in follows:

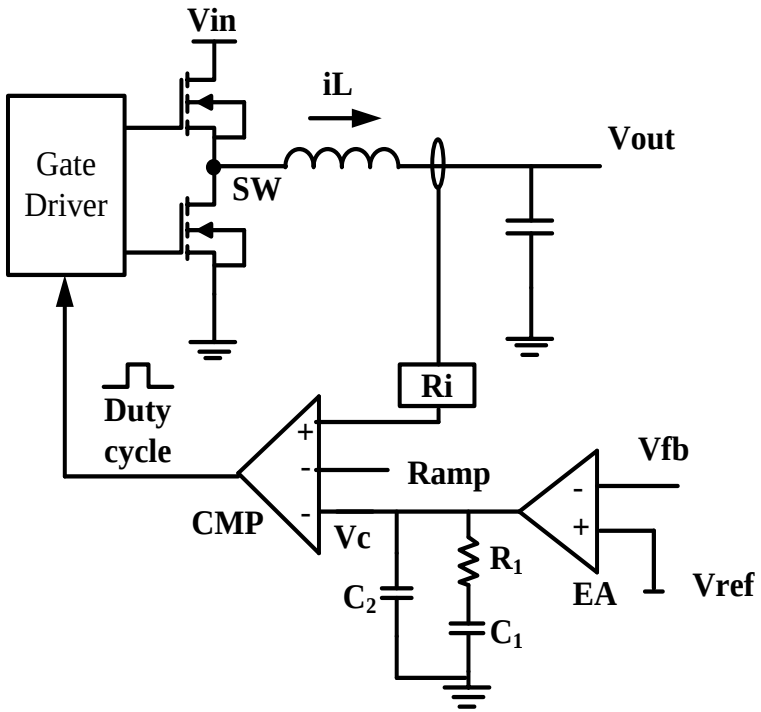
Jingdong Sun, Yimajian Yan, Hanfeng Wang, Emil Chen, Ken Wu and Jun Fan. “Topology-based Accurate Modeling of Current-Mode Voltage Regulator Modules for Power Distribution Network Design.”, under review.

The END

Backup

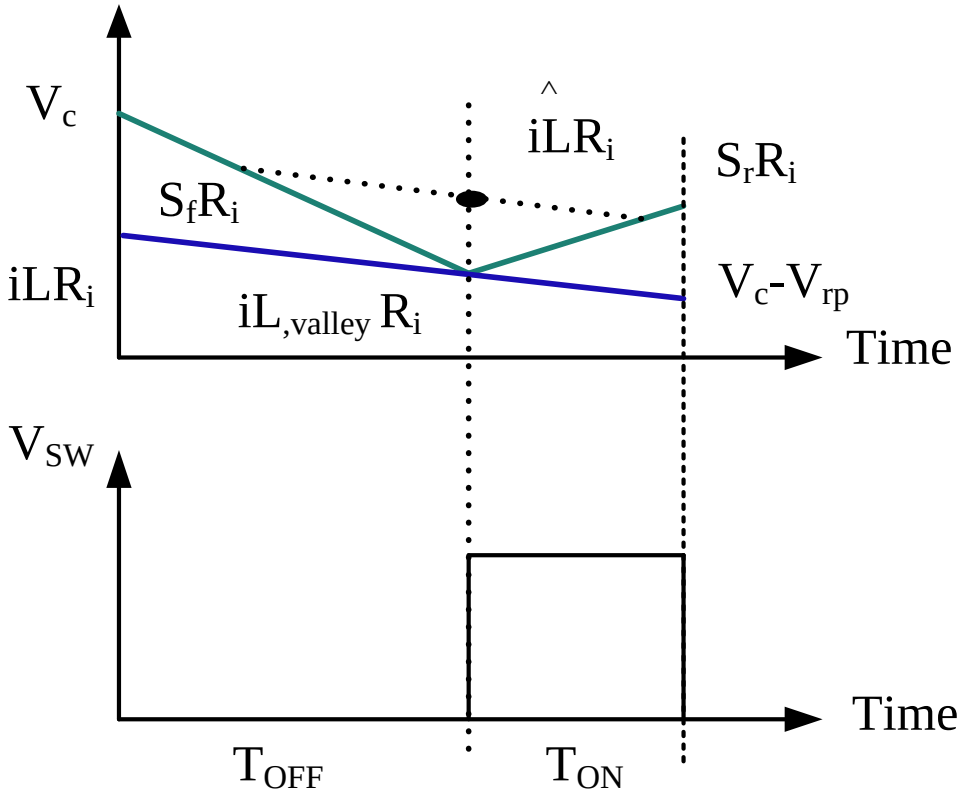
PFM Controller





- The current PFM controller has almost the same structure as PWM one;
- The current loop comparator has opposite polarity due to on generator is used;
  - Only the current feedback loop is different.

Equation for PFM Controller



- The switching period could be calculated according to the waveforms.

$$i_{L,valley} - \hat{i_L} + (1 - \frac{T_{ON}}{T_{sw}})T_{ON}(S_r - S_f) = 0$$

$$D_s = (S_r - S_f)$$

$$T_{sw} = \frac{T_{on}(D_s R_i T_{on} + 2V_{rp})}{-2\hat{i_L} R_i + D_s R_i T_{on} + 2V_c}$$