IBIS Based Buck Converter DC Modeling

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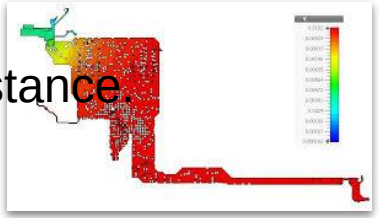
Objective

System-Level Power Simulation Coverage

- **System level DC simulations**, including IR drop, DC resistance.
- AC simulations, i.e. PDN impedance
- Transient load response, i.e. transient power noise
- **System power consumption and efficiency**
- Power/thermal co-simulation



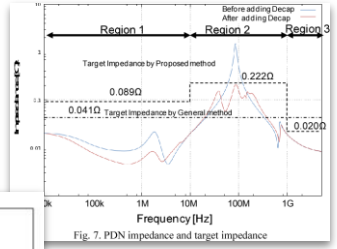
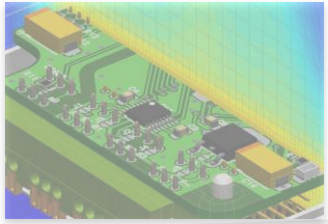
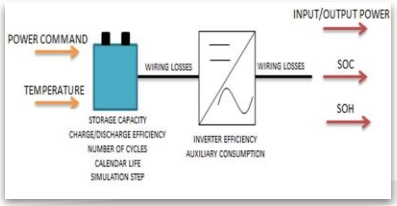
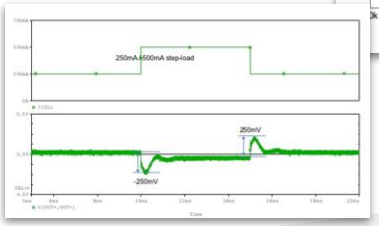


Fig. 7. PDN impedance and target impedance



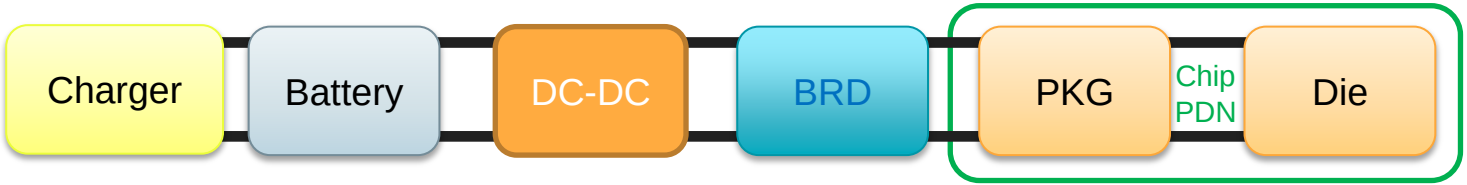




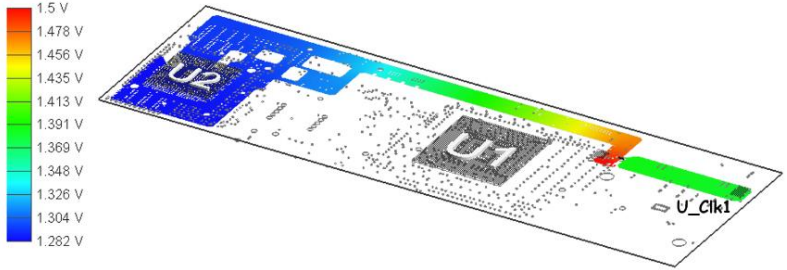
Outline

- Background: DC simulation common methodology
- Proposed buck converter IBIS Model
- Validation by measurement
- Conclusion
- Future work

Background: DC Simulation Common Methodology



- Charger & Battery not modeled. Model from DC-DC to Die IR drop.
- DC-DC model as voltage source
- BRD & all the passive components on board as a resistance network
- PKG resistance network
- Die as current sink/load

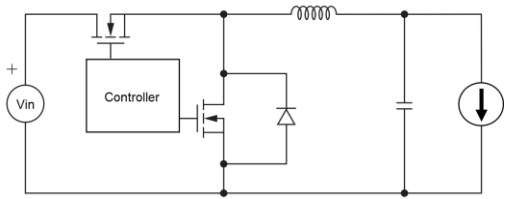


Common DC Simulation Shortcomings and Proposal

- Shortcomings
  - No DC-DC converter information. No power consumption or power efficiency information.
  - Have to readout and key in current load and voltage source values for all the rails manually. Easy to make a mistake.
- Proposal
  - **DC-DC converter vendor to provide detailed chip model in IBIS format to model switching and conduction power loss**.
- Advantage
  - System power consumption and efficiency can be evaluated.
  - With the DC-DC converter IBIS model available, DC simulation for all power rails can be set up automatically.
  - Efficient to optimize the PCB layout.

Introduction to Buck Converter

- Buck converter is composed of two switches, one inductor and capacitors.



- Buck converter is step down DC-DC converter. It converts high voltage to low voltage and serves as voltage source to the sink IC. It is a type of switching mode power supply (SMPS). It provides much higher power efficiency than a linear regulator.

Proposed Buck Converter IBIS Model Standard Format

The proposed IBIS model includes the following key parameters.

Device physical parameters (from vendor)

Inductor

1) Inductance: L
2) Inductor ESR: R_{L_ESR}

High side switch

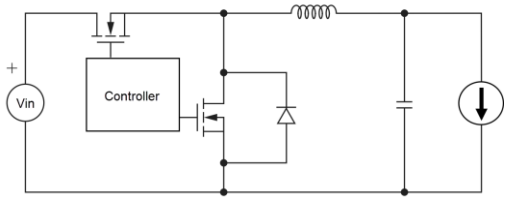
1) Resistance when high side MOSFET is on: R_{on_HS}
2) Rising time and falling time of high side MOSFET: t_{on_HS} and t_{off_HS}
3) FET gate charge on high side MOSFET: $Q_{FET\_G\_HS}$
4) MOSFET output capacitance on high side: C_{oss_HS}

Low side switch

1) Resistance when low side MOSFET is on: R_{on_LS}
2) FET gate charge on low side MOSFET: $Q_{FET\_G\_LS}$
3) Low side body diode charge: $Q_{body\_diode\_LS}$
4) Low side body diode threshold voltage: V_{th}
5) MOSFET output capacitance on low side: C_{oss_LS}

System controlled parameters (from designer)

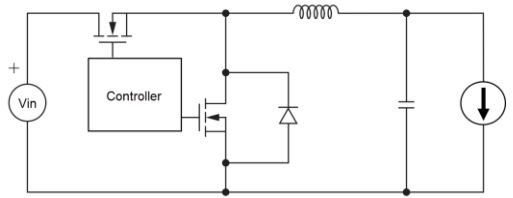
1) **Input voltage: V_{in}**
2) **Output voltage: V_o**
3) **Output current: I_o**
4) **Switching frequency: freq**
5) **Gate drive voltage: V_{gs}**
6) **Dead time for rising and falling: t_{r_dead} and t_{f_dead}; the dead time is the time to turn off both FETs to avoid shunt through current from power directly to ground.**



Referenced Power Consumption Calculation

- The proposed IBIS model parameters are shown in the previous slide. The simulation tool defines how to use these parameters to calculate the power consumption in their own solver. The referenced equations to calculate buck converter power consumption in CCM are shown in the following pages.

- The buck converter power loss mainly comes from three parts: inductor conduction loss, FET conduction loss and FET switching loss. The loss from capacitors are relatively small and are not included. The PCB DCR loss can be obtained from the EDA tool.

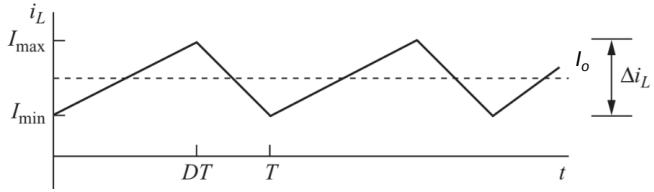


Continuous Current Mode

Non-ideal Buck Converter DC Modeling (1)

The following formulas are for the CCM mode.

- **Inductor conduction loss: $P_{L\_ESR}= I_{L\_rms}^2*R_{L\_ESR}$**



where $I_{L\_rms}=sqrt(I_o^2+I_{L\_delta}^2/12)$ **and** R_{L_ESR} **is the inductor ESR;**

I_o **is the load current;**

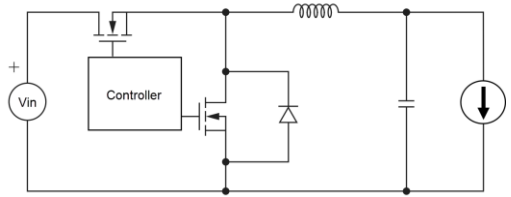
$I_{L\_delta}=(V_{in}-V_o)*D/freq/L$;

V_{in} **and** V_o **are input and output voltage for the buck converter, respectively;**

D is duty cycle equal to V_o/V_{in};

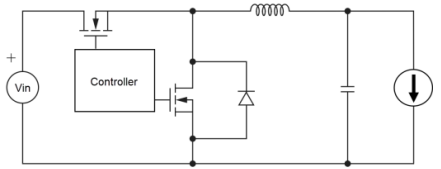
freq is the switching frequency;

L is the inductance.



Non-ideal Buck Converter DC Modeling (2)

- **High side MOSFET conduction Loss**: $P_{CL\_HS}= I_{rms\_HS}^2*R_{on\_HS}$



where R_{on_LS} **is conduction resistance on high side FET and** $I_{rms\_HS}=sqrt(D)*I_{L\_rms}$

- **High side switching loss**: $P_{SL\_HS}=0.5*V_{in}*(I_{L\_min}*t_{on\_HS}+I_{L\_max}*t_{off\_HS})*freq$

where V_{in} **is input voltage;** I_{L_min} **and** I_{L_max} **are minimum inductor current** $(I_o-0.5*I_{delta})$ **and maximum inductor current**$(I_o+0.5*I_{delta})$**, respectively;** t_{on_HS} **and** t_{off_HS} **are rising time and falling time, respectively.**

- **High side Gate Drive Loss**: $P_{GDL\_HS}=V_{GS}*Q_{FET\_G\_HS}*freq$

where V_{GS} **is the gate drive voltage;** $Q_{FET\_G\_HS}$ **is the high side MOSFET gate charge.**

- **High side FET Coss Loss**: $P_{CL\_HS}=0.5*C_{oss\_HS}*V_{in}^2*freq$

where C_{oss_HS} **is the high side MOSFET output capacitance.**

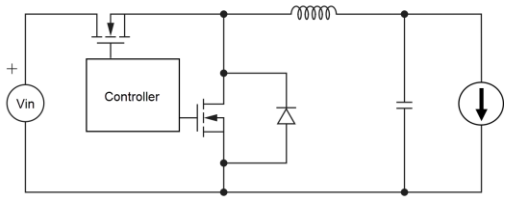
Non-ideal Buck Converter DC Modeling (3)

- **Low side MOSFET conduction Loss:** $P_{CL\_LS} = I_{rms\_LS}^2 * R_{on\_LS}$

where $I_{rms\_LS} = sqrt(1-D) * I_{L\_rms}$;

I_{L_rms} **is the inductor rms current;**

R_{on_LS} **is conduction resistance on low side FET.**



Non-ideal Buck Converter DC Modeling (4)

- **Low side body diode reverse recovery loss**: $P_{BDRRL\_LS}=V_{in}*Q_{body\_diode\_LS}*freq$

where $Q_{body\_diode\_LS}$ **is reverse distributed charge when high side MOSFET is on and reverse bias is applied.**

- **Low side body diode conduction loss**: $P_{BDCL\_LS}=V_{th}*(I_{L\_min}*t_{r\_dead}+I_{L\_max}*t_{f\_dead})*freq$

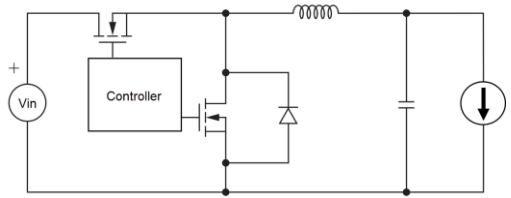
where V_{th} **is the diode threshold voltage, 0.7V.** t_{r_dead} **and** t_{f_dead} **are the dead time for rising and falling, respectively.**

- **Low side gate drive loss**: $P_{GDL\_LS}=V_{GS}*Q_{FET\_G\_LS}*freq$

where $Q_{FET\_G\_LS}$ **is the low side MOSFET gate charge.**

- **Low side FET Coss loss**: $P_{CL\_LS}=0.5*C_{oss\_LS}*freq*V_{in}^2$

where C_{oss_LS} **is the low side MOSFET output capacitance.**



Summary of Buck Converter Power Consumption

The total power loss is the summation of the inductor DCR loss, the FET conduction loss and the FET switching loss.

Inductor conduction loss	$P_{L\_ESR} = I_{L\_rms}^2 * R_{L\_ESR}$
High side MOSFET conduction loss	$P_{CL\_HS} = I_{rms\_HS}^2 * R_{on\_HS}$
High side switching loss	$P_{SL\_HS} = 0.5 * V_{in} * (I_{L\_min} * t_{on\_HS} + I_{L\_max} * t_{off\_HS}) * freq$
High side Gate Drive Loss	$P_{GDL\_HS} = V_{GS} * Q_{FET\_G\_HS} * freq$
High side FET Coss Loss	$P_{CL\_HS} = 0.5 * C_{oss\_HS} * V_{in}^2 * freq$
Low side MOSFET conduction loss	$P_{CL\_LS} = I_{rms\_LS}^2 * R_{on\_LS}$
Low side body diode reverse recovery loss	$P_{BDRRL\_LS} = V_{in} * Q_{body\_diode\_LS} * freq$
Low side body diode conduction loss	$P_{BDCL\_LS} = V_{th} * (I_{L\_min} * t_{r\_dead} + I_{L\_max} * t_{f\_dead}) * freq$
Low side gate drive loss	$P_{GDL\_LS} = V_{GS} * Q_{FET\_G\_LS} * freq$
Low side FET Coss loss	$P_{CL\_LS} = 0.5 * C_{oss\_LS} * freq * V_{in}^2$

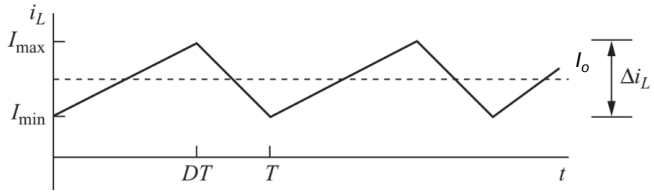
Criteria for CCM and DCM

The boundary for CCM and DCM is:

$$I_{L\_ripple} = \frac{1}{2} * I_{L\_delta}$$

$$= (V_{in} - V_o) * D / freq / L / 2;$$

- **CCM: $I_o > I_{L\_ripple}$**
- **DCM: $I_o < I_{L\_ripple}$**



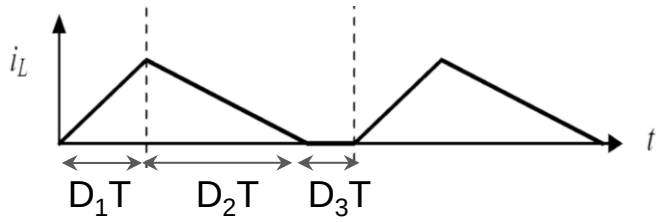
$I_{o\_boundary} = (V_{in} - V_o) V_o / (2 V_{in} * L * freq)$

When I_o is larger than $I_{o\_boundary}$ it is in CCM; otherwise, it is in DCM.

Discontinuous Current Mode

Non-ideal Buck Converter DC Modeling (1)

The following formulas are for the DCM mode.



- **Inductor conduction loss: $P_{L\_ESR} = I_{L\_rms}^2 * R_{L\_ESR}$**

where **$I_{L\_rms} = I_{L\_pk} * sqrt((D_1+D_2)/3)$ and R_{L_ESR} is the inductor ESR;**

$I_{L\_pk} = sqrt(V_o * I_o * 2(V_{in}-V_o)/V_{in}/L/freq)$, is the peak inductor current; Note: the efficiency is assumed to be 100% for the peak current calculation.

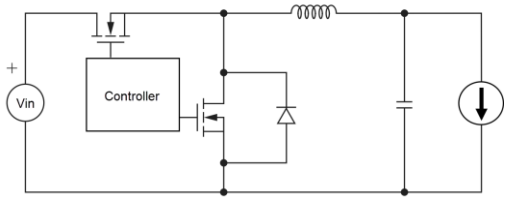
V_{in} and V_o are input and output voltage for the buck converter, respectively; I_o is the load current;

$D_1 = I_{L\_pk}/(V_{in}-V_o) * L * freq$;

$D_2 = I_{L\_pk}/V_o * L * freq$;

freq is the switching frequency;

L is the inductance.



Non-ideal Buck Converter DC Modeling (2)

- **High side MOSFET conduction Loss**: $P_{CL\_HS} = I_{rms\_HS}^2 * R_{on\_HS}$

where R_{on_LS} is conduction resistance on high side FET and $I_{rms\_HS} = sqrt(D_1/3) * I_{L\_pk}$;

- **High side switching loss**: $P_{SL\_HS} = 0.5 * V_{in} * I_{L\_pk} * t_{off\_HS} * freq$

where V_{in} is input voltage; I_{L_pl} is peak inductor current; t_{off_HS} is the FET falling time.

- **High side Gate Drive Loss**: $P_{GDL\_HS} = V_{GS} * Q_{FET\_G\_HS} * freq$

where V_{GS} is the gate drive voltage; $Q_{FET\_G\_HS}$ is the high side MOSFET gate charge.

- **High side FET Coss Loss**: $P_{CL\_HS} = 0.5 * C_{oss\_HS} * V_{in}^2 * freq$

where C_{oss_HS} is the high side MOSFET output capacitance.

Non-ideal Buck Converter DC Modeling (3)

- **Low side MOSFET conduction Loss**: $P_{CL\_LS} = I_{rms\_LS}^2 * R_{on\_LS}$

where $I_{rms\_LS} = sqrt(D_2/3) * I_{L\_pk}$; R_{on_LS} is conduction resistance on low side FET.

- **Low side body diode conduction loss**: $P_{BDCL\_LS} = V_{th} * I_{L\_pk} * t_{f\_dead} * freq$

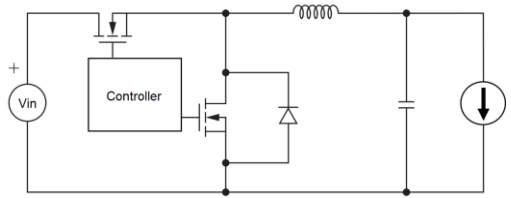
where V_{th} is the diode threshold voltage, 0.7V. t_{r_dead} and t_{f_dead} are the dead time for rising and falling, respectively.

- **Low side gate drive loss**: $P_{GDL\_LS} = V_{GS} * Q_{FET\_G\_LS} * freq$

where $Q_{FET\_G\_LS}$ is the low side MOSFET gate charge.

- **Low side FET Coss loss**: $P_{CL\_LS} = 0.5 * C_{oss\_LS} * freq * V_{in}^2$

where C_{oss_LS} is the low side MOSFET output capacitance.



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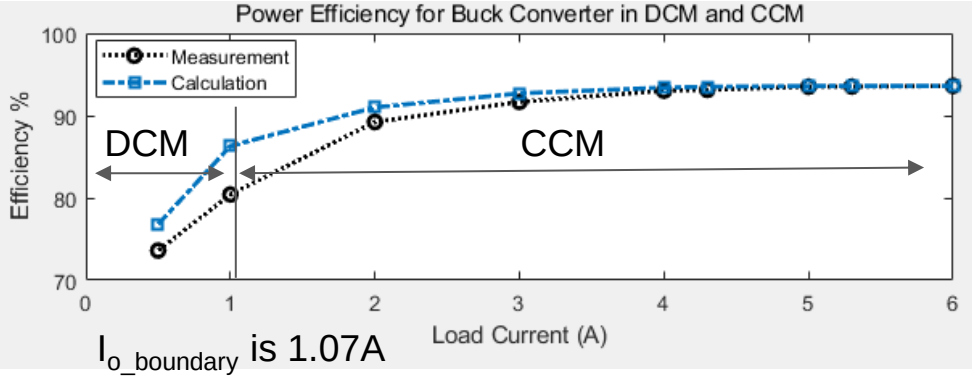
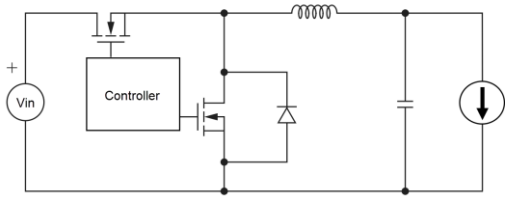
High side MOSFET conduction loss	$P_{CL\_HS} = I_{rms\_HS}^2 * R_{on\_HS}$
High side switching loss	$P_{SL\_HS} = 0.5 * V_{in} * I_{L\_pk} t_{off\_HS} * freq$
High side Gate Drive Loss	$P_{GDL\_HS} = V_{GS} * Q_{FET\_G\_HS} * freq$
High side FET Coss Loss	$P_{CL\_HS} = 0.5 * C_{oss\_HS} * V_{in}^2 * freq$
Low side MOSFET conduction loss	$P_{CL\_LS} = I_{rms\_LS}^2 * R_{on\_LS}$
Low side body diode conduction loss	$P_{BDCL\_LS} = V_{th} * I_{L\_max} * t_{f\_dead} * freq$
Low side gate drive loss	$P_{GDL\_LS} = V_{GS} * Q_{FET\_G\_LS} * freq$
Low side FET Coss loss	$P_{CL\_LS} = 0.5 * C_{oss\_LS} * freq * V_{in}^2$

Example: Power Consumption of a Buck Converter

The calculated power loss matches with the measurement.



$I_{o\_boundary}$ is 1.07A



Device Parameters		Value
Inductor	L	2.2 uH
	R_{L_ESR}	21 mohm
High side switch	R_{on_HS}	7 mohm
	t_{on_HS}	3.4 ns
	t_{off_HS}	2.4 ns
	$Q_{FET\_G\_HS}$	8.9 nQ
	C_{oss_HS}	300 pF
Low side switch	R_{on_LS}	2.1 mohm
	$Q_{FET\_G\_LS}$	33 nQ
	$Q_{body\_diode\_LS}$	5 nC
	V_{th}	0.7 V
	C_{oss_LS}	1100 pF

System Parameters	Value
V_{in}	20 V
V_o	7.7 V
I_o	1 A
freq	1000 kHz
t_{r_dead}	20 ns
t_{f_dead}	20 ns
V_{gs}	5 V

Other parameters on the board	Value
R_{before_buck}	66 mohm
R_{after_buck}	6 mohm
$I_{controler\_quiescent}$	30 mA

Conclusion

- The calculated power efficiency is validated with measurement.
- The proposed model can be used to evaluate the power loss and power efficiency of buck converter working in CCM and DCM.

The END