Next Generation IBIS-AMI Modeling

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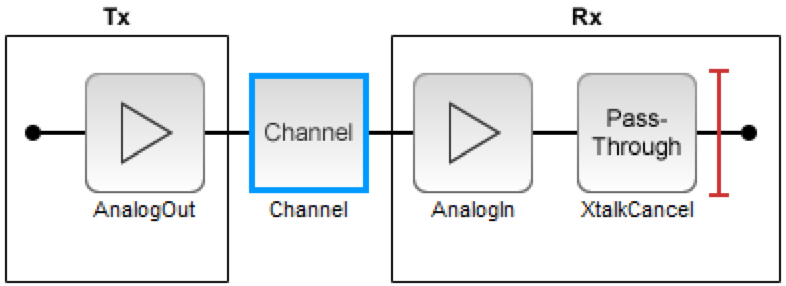
Overview

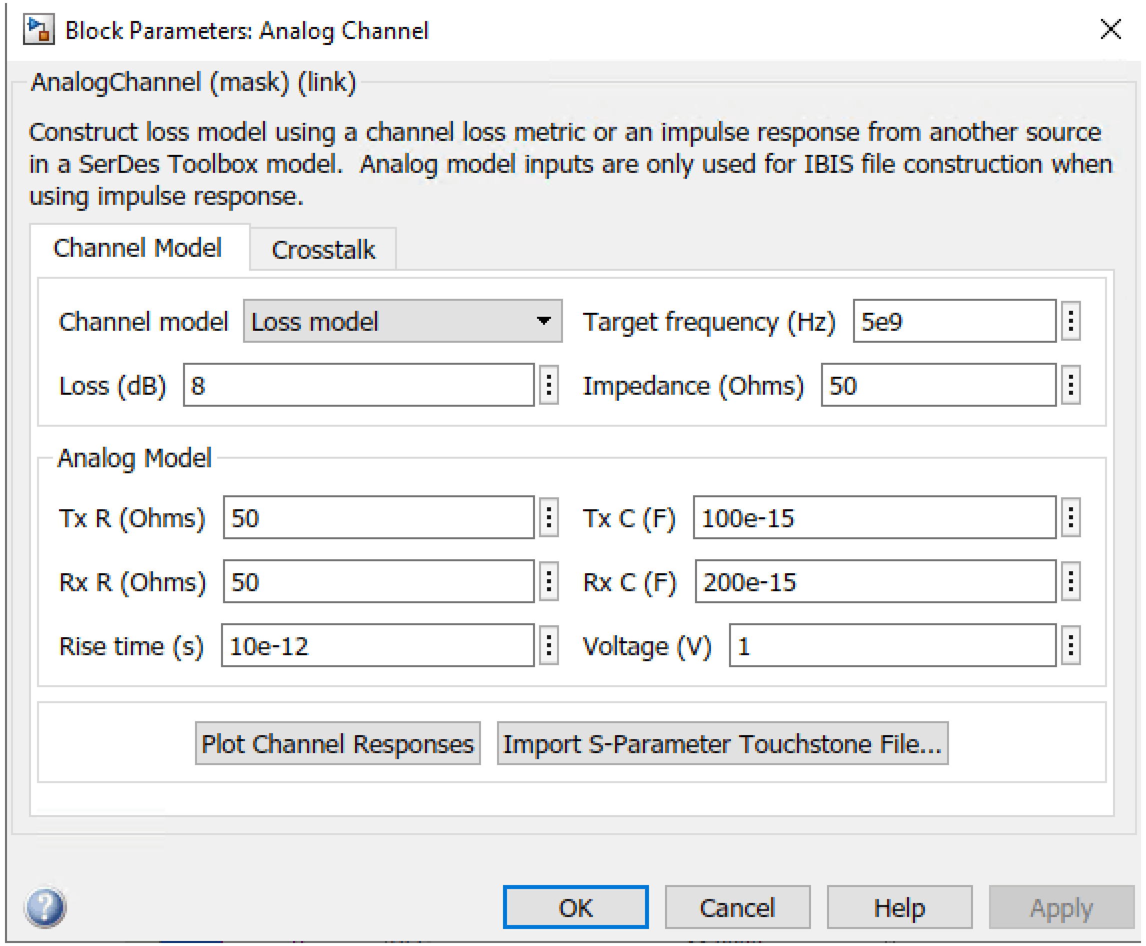
- Crosstalk Cancelation
- Training Algorithms
- BIRD205 Rx_Decision_Time
- BIRD213 Extending IBIS-AMI for PAMn Analysis
- BIRD204 Clock Forwarding
- Architectural 112G PAM4 ADC-Based SerDes Model

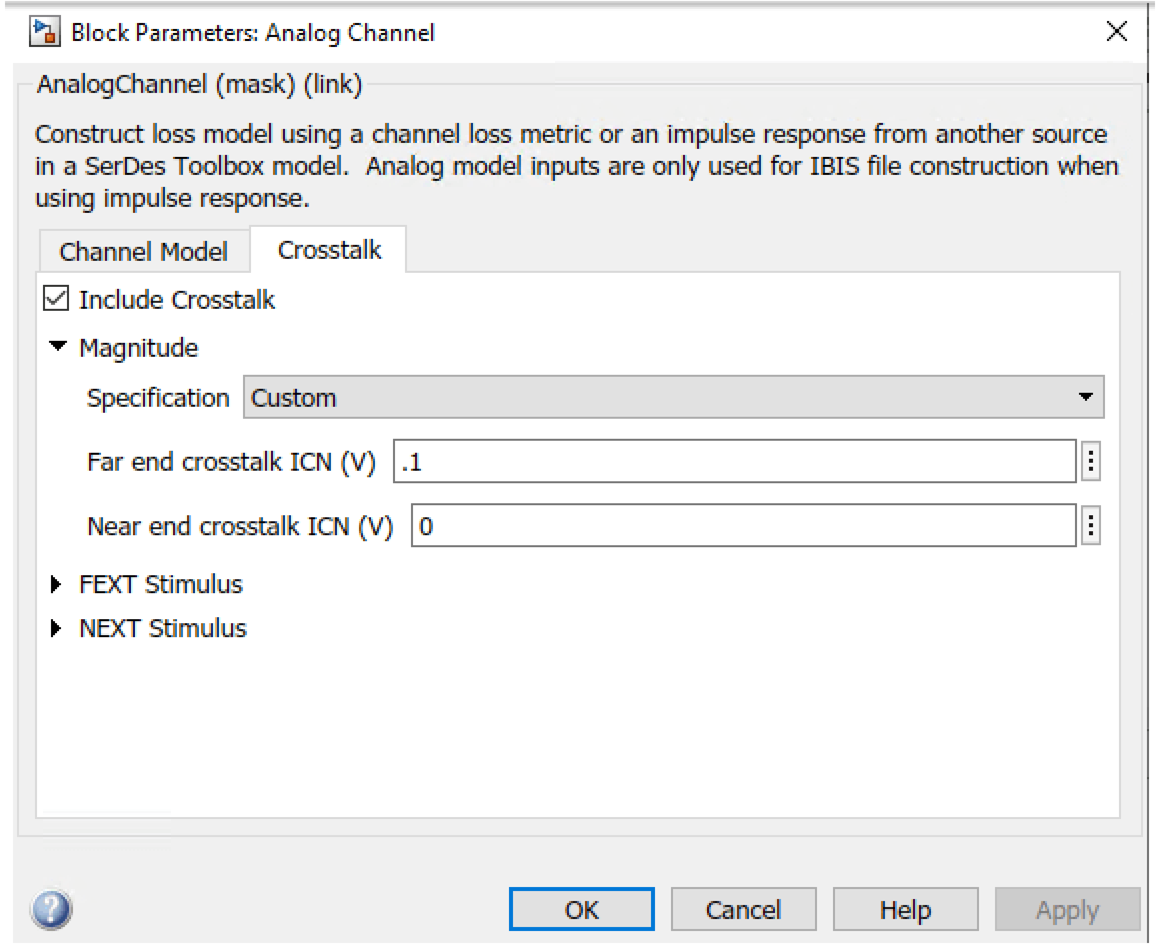
Crosstalk Cancelation

This is a topic for discussion in future IBIS meetings.

Crosstalk Cancelation
Ideal Lossy Coupled Channel







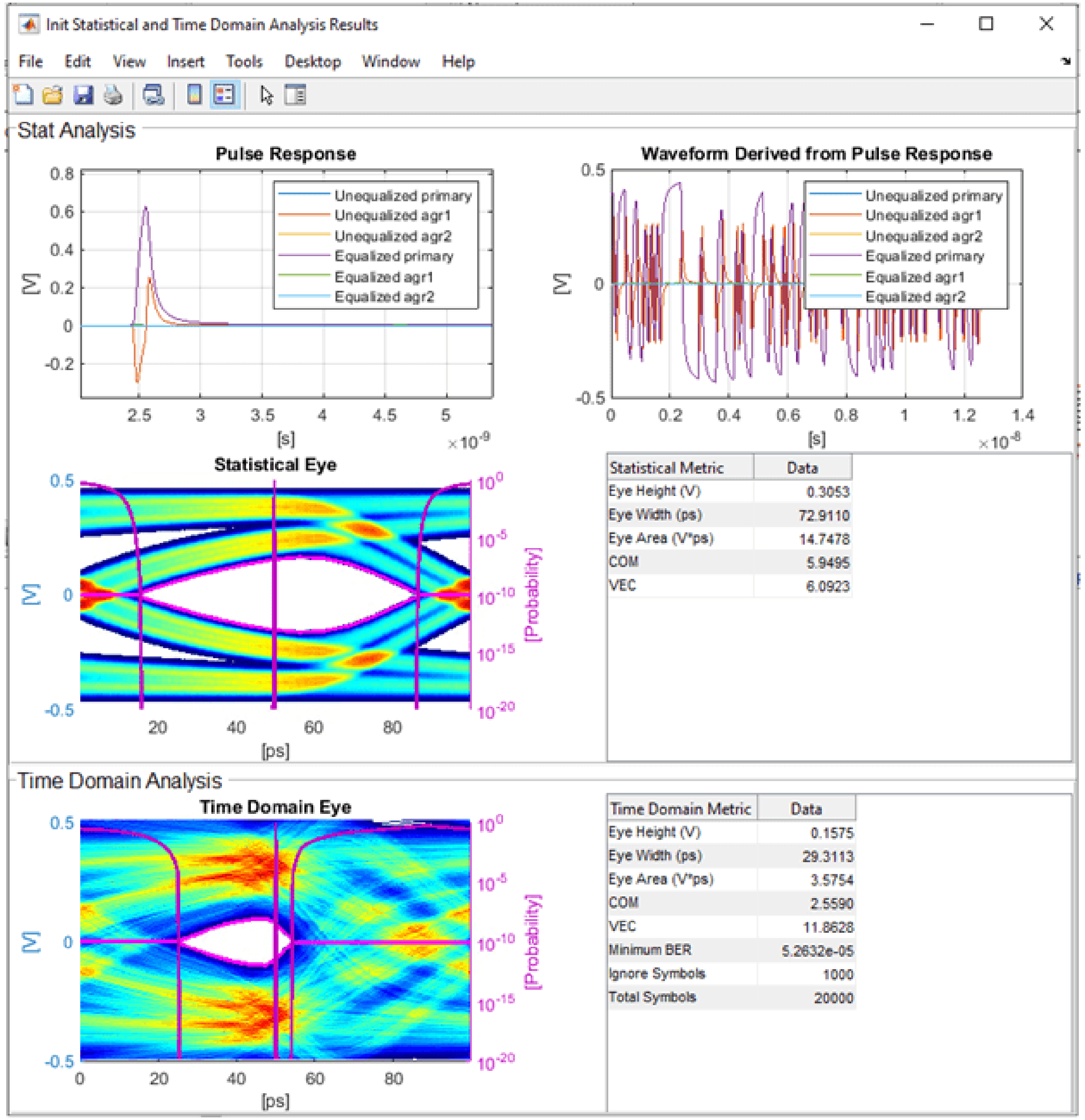
This Prototype will only Cancel Strict FEXT Crosstalk

- FEXT normally refers to aggressor signals traveling in the same direction as the victim signal.
- IEEE802.3 has a stricter definition of FEXT.
  - The signals must travel in the same direction
  - The victim and aggressor Tx must be in the same chip
  - The victim and aggressor Rx must be in the same chip
  - The victim and aggressor channels must be routed the same way

Crosstalk cancelation applies a filter to the aggressor waveform, then scales and delays it to maximize cancelation of the aggressor crosstalk waveform.

The filter in this example is a derivative. Model makers should use a CTLE generated from a transfer function of the actual filter

Time domain cancelation will require a BIRD to pass aggressor waveforms into the Rx AMI_GetWave



Does Crosstalk Cancelation Require a BIRD?

- Impulse response of aggressor channel is assumed to be the same as the impulse response of the victim channel (consistent with FEXT).
- This prototype used Model_Specific parameters to determine which column(s) in the impulse_matrix should be cancelled.
- Time Domain crosstalk cancelation would require additional waveform inputs to Rx AMI_GetWave

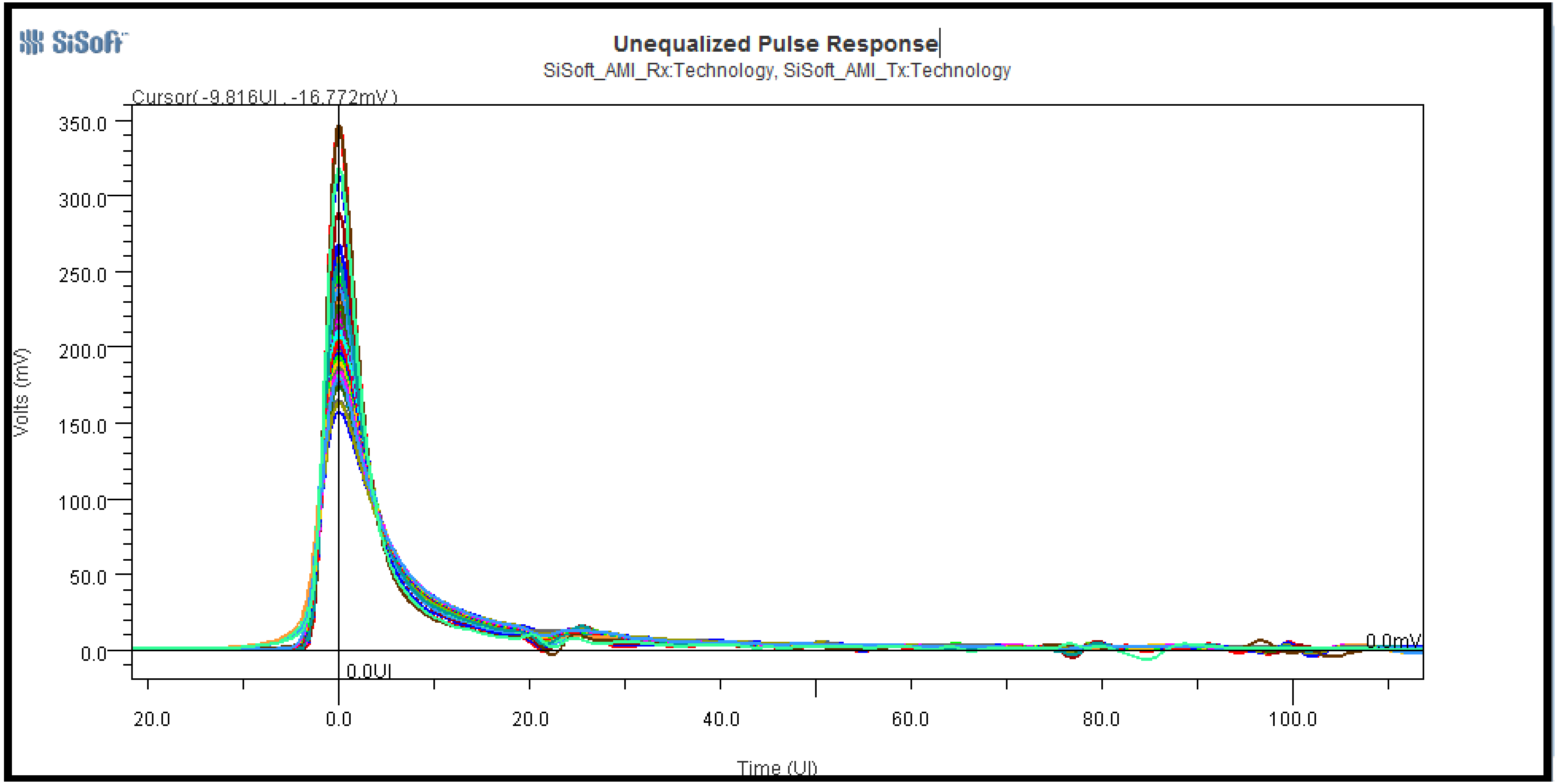
Training Algorithms

IBIS 7.1 contains support for both Statistical and Time Domain Back Channel Optimization. This example compares several optimization search algorithms that can be used in both hardware implementation of training, and software implementation using IBIS models.

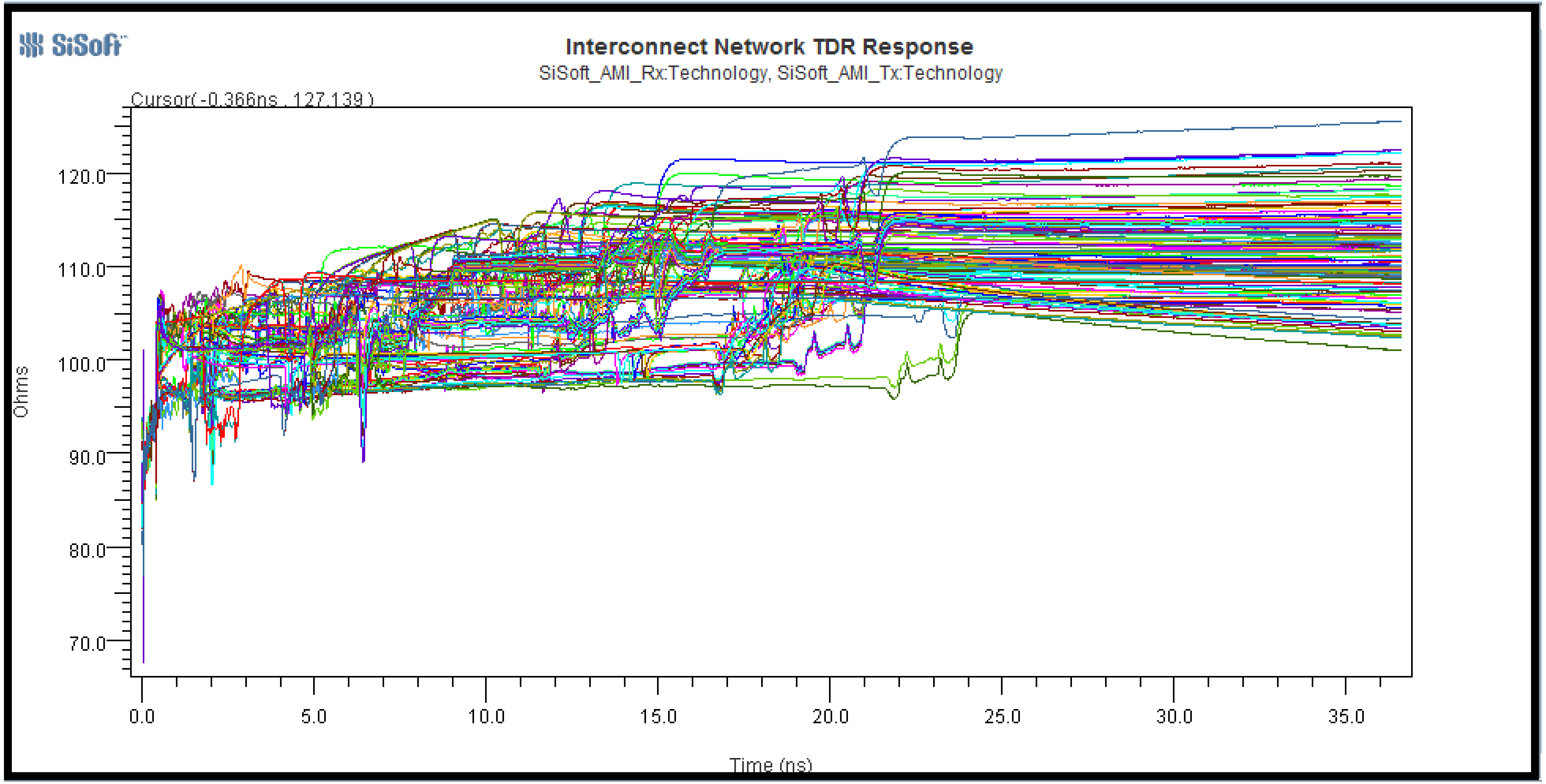
Comparing Training Algorithms on PAM4 802.3ck Channels

- I chose 65 channels from the IEEE 802.3ck site
  - https://www.ieee802.org/3/ck/public/tools/index.html
  - Upen Kateri’s channels, 17-Jul-2018
  - Nathan Tracy’s channels, 16-Jan-2019
  - Rich Mellitz’s cabled backplane channels, 15-Aug-2018
- Package model from the same site
  - 90ohm package, 30mm long with 50ohm ports

65 Un-equalized Pulse Responses



65 TDR



SiSoft
Interconnect Network TDR Response
SiSoft_AMI_Rx:Technology, SiSoft_AMI_Tx:Technology
Cursor(-0.366ns , 127.139)
120.0
110.0
100.0
90.0
80.0
70.0
Ohms
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
Time (ns)

Tx and Rx Models

- Tx
  - 5 Tap FFE
    - 2 pre-cursor taps
    - 2 post cursor taps
- Rx
  - CTLE
    - Peaking Gain 0 to 40 dB in 1 dB steps
  - AGC
  - 30 Tap FFE
    - 2 pre-cursor taps
    - 27 post cursor taps
  - 1 Tap DFE

Comparing Different Search Algorithms Using 1 of the 65 Channels. COM is Essentially Zero if no Equalization

Method	Time (Seconds)	# Sims	Time / Sim	Area (V*S / UI)	WxH (V*S /UI)	Mean Eye Height	Eye Height	Width (ps)	Metric COM	Fixed CTLE	DFE	-2	-1	Main	1	2	3	4
ga	1387.68	40103	0.0346	5.1318	9.46271	0.5088	0.382	24.78	12.0637	13	-0.233	0.041	-0.233	1	-0.053	0.024	0.1	-0.02
Genetic	810.901	20150	0.0402	5.1192	9.30212	0.5041	0.378	24.61	12.0357	13	-0.212	0.041	-0.232	1	-0.092	0.043	0.094	-0.04
surrogateopt	1390.19	2002	0.6944	4.9803	8.5693	0.4781	0.353	24.31	11.6114	13	-0.239	0.028	-0.168	1	-0.15	0.075	0.091	-0.06
fmincon	82.6598	2324	0.0356	4.9877	8.6149	0.4902	0.369	23.36	12.1244	13	-0.216	0.04	-0.201	1	-0.134	0.0627	0.1	-0.05
simulannealbnd	2253.01	65003	0.0347	5.0082	9.11279	0.5139	0.381	23.9	11.7629	13	-0.201	0.06	-0.275	1	-0.045	0.0228	0.098	-0.03
adaptFFE	5.20286	153	0.034	4.63	9.26569	0.5076	0.366	25.34	11.0693	13	-0.167	0.096	-0.334	1	-0.062	0.0204	0.098	-0.02
patternsearch	106.261	3073	0.0346	3.2817	4.79681	0.5448	0.269	17.86	5.90035	13	-0.384	-0.03	0.128	1	-0.032	0.051	0.076	-0.01

CTLE was fixed, all other Taps treated as floats because of limitations of some of the search algorithms.

Genetic is the only algorithm in this list that can be implemented in the firmware of the processor controlling training.

adaptFFE is a proprietary method specifically developed for optimizing FFE equalizers

ga, surrogateopt, fmincon, simulannealbnd and patternsearch are MATLAB optimization methods.

E.g., Search in browser for "MATLAB ga" for a description of ga.

Are Existing Back Channel BIRDs Sufficient?

- Training a channel turns out to be a more complex problem than just optimizing tap settings.
- DDR5 interfaces also require training driver and ODT IBIS model analog settings.
- The implementation of training in this example was implemented in a simulator specifically written to evaluate training algorithms.

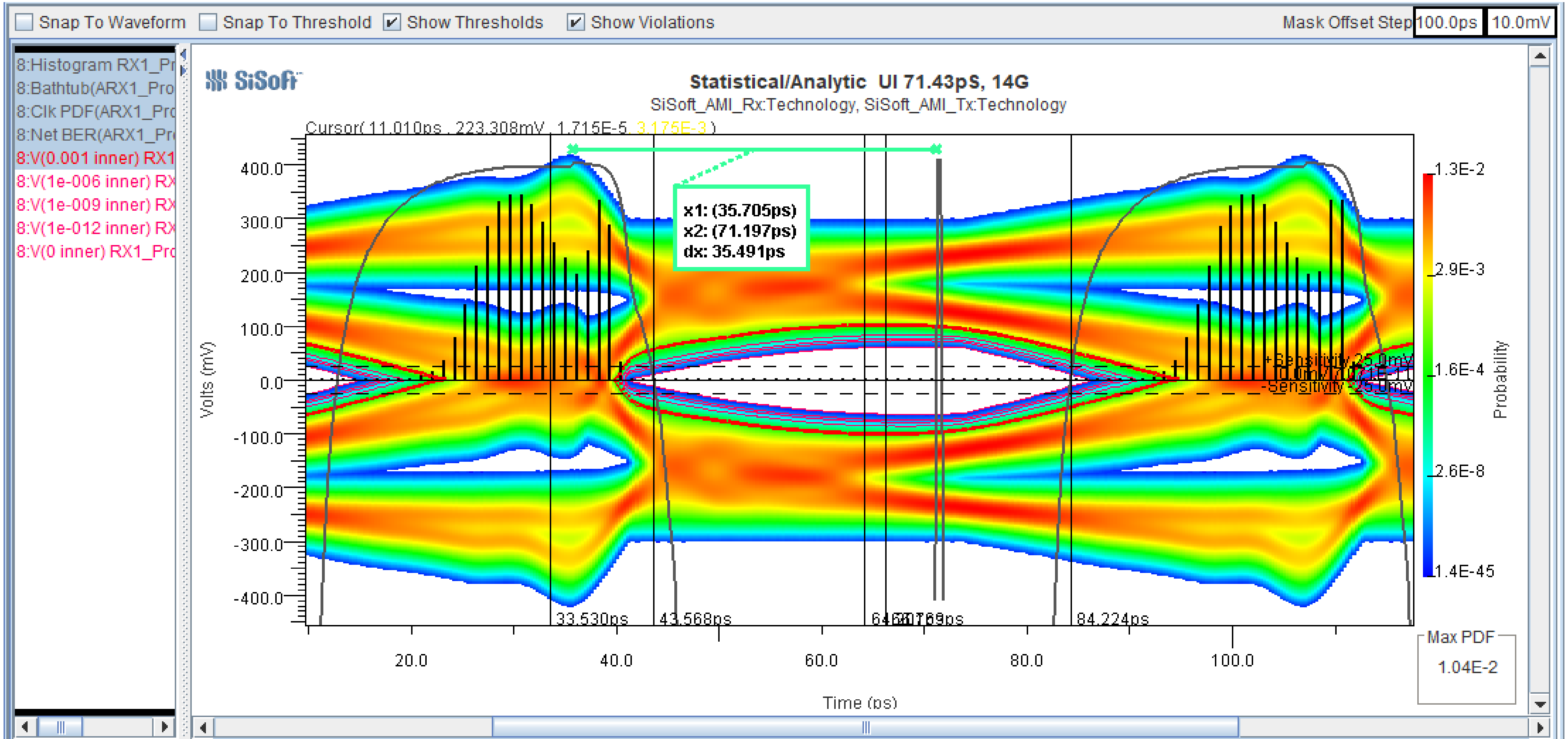
BIRD205 Rx_Decision_Time

BIRD 205 has been approved for IBIS 7.1

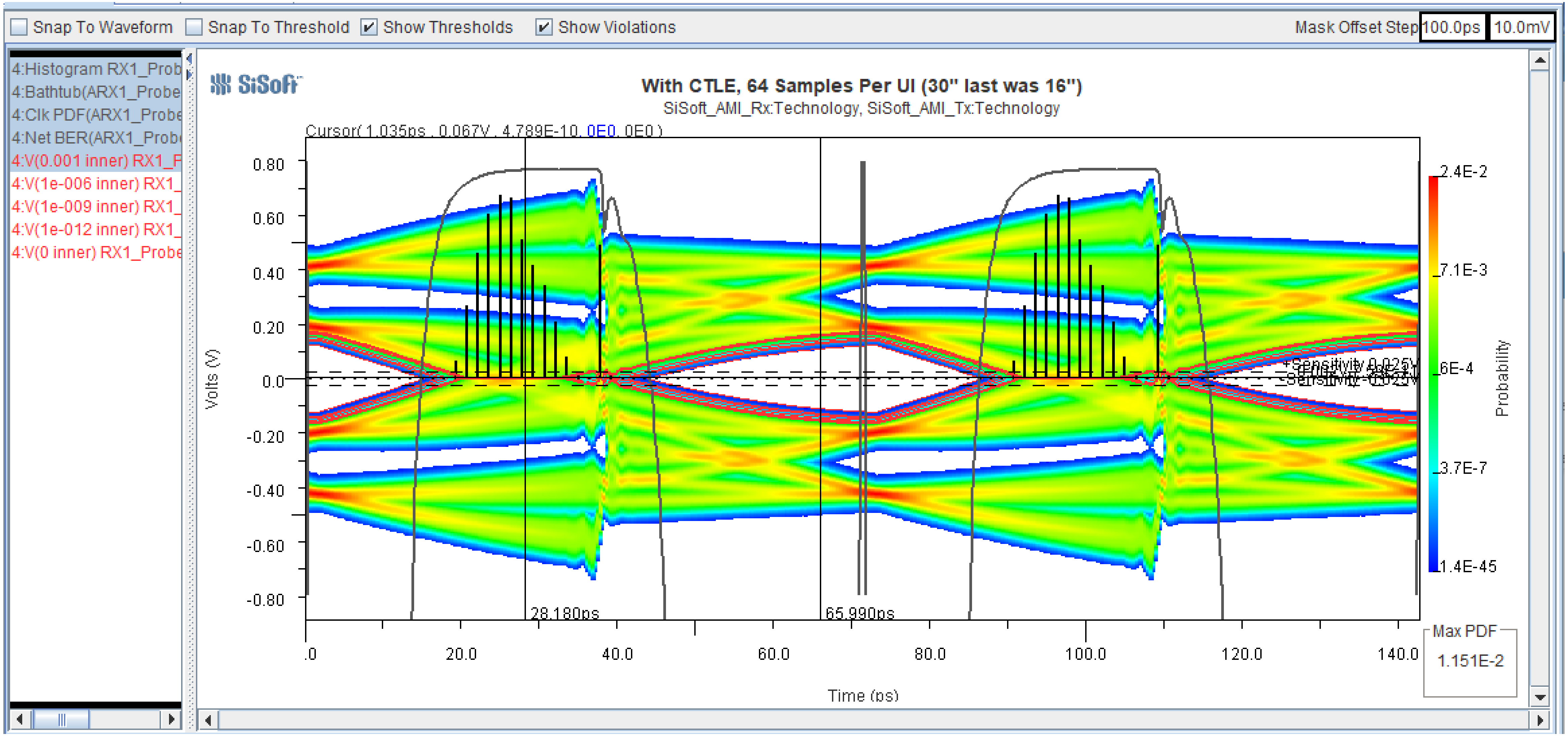
Rx_Decision_Time is a New Reserved AMI Parameter for Statistical Simulations

- EDA tools have used several methods to determine this time location in the eye to sample the data
  - Bang-Bang, ½ UI after the median of the jitter PDF (assumes a Bang-Bang CDR)
  - Tmid (center of the 1e-3 eye contour)
  - Hula Hoop
  - …
- Hardware often adjust the sample point generated from Bang-Bang, Alexander or Mueller-Muller phase detectors to achieve significant SNR and BER improvements.
- DDR5 shifts the DQS/DQ phase left and right until errors are detected, typically to find the 1e-3 or 1e-5 eye contour tear ducts.

Shift Clock Time to Right Does Not Affect Right Inner Contour
Shift Clock to Left Does Affect Left Inner Contour
Errors Occur When Contour is Below Rx_Receiver_Sensitivity



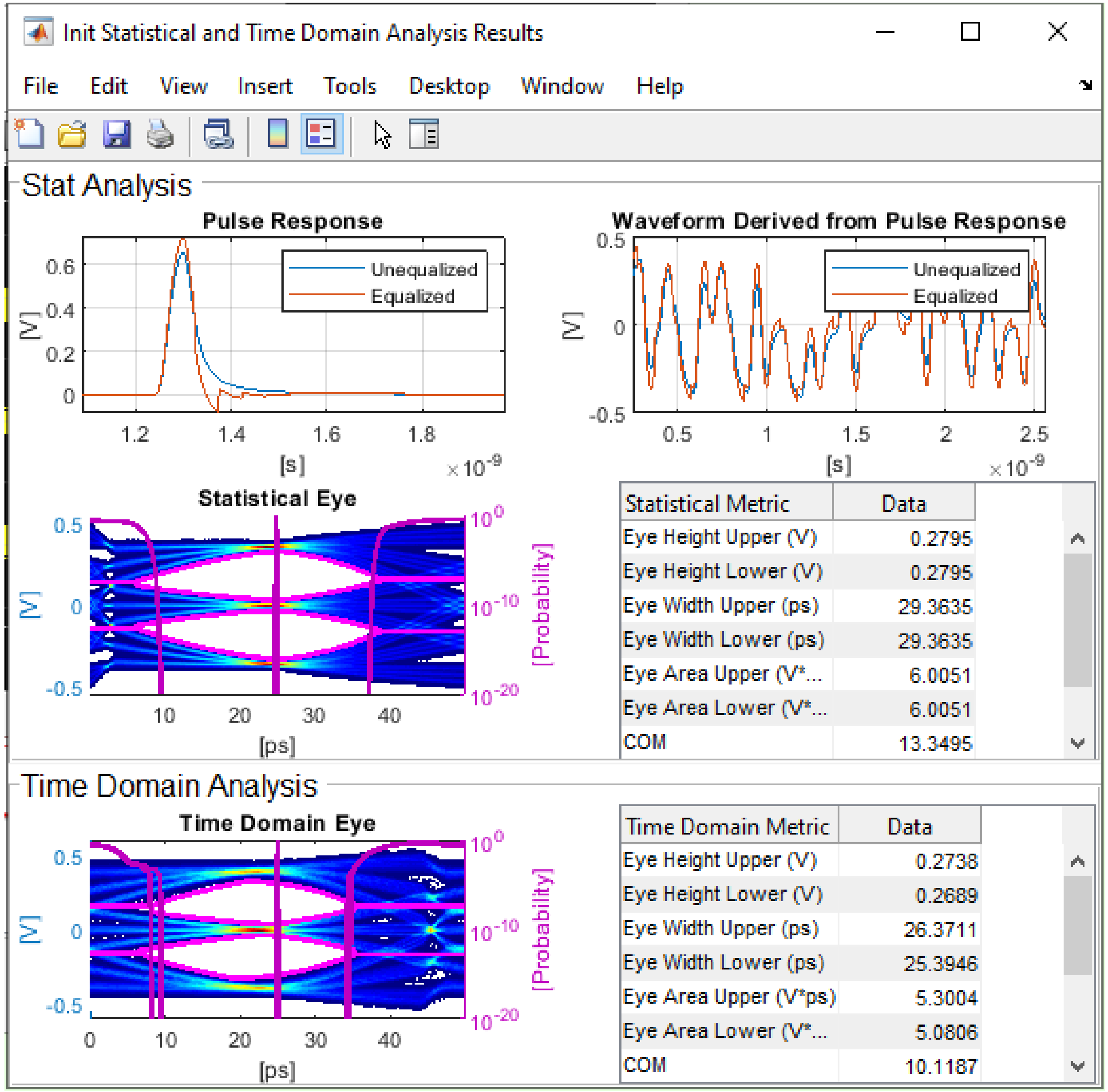
30” (last was 16”) with CTLE and 64 Samples Per UI
Note Smaller Affect on Left Eye Tear Duct Time



BIRD213 Extending IBIS-AMI for PAMn Analysis

- This BIRD has not yet been approved, planned for after IBIS 7.1

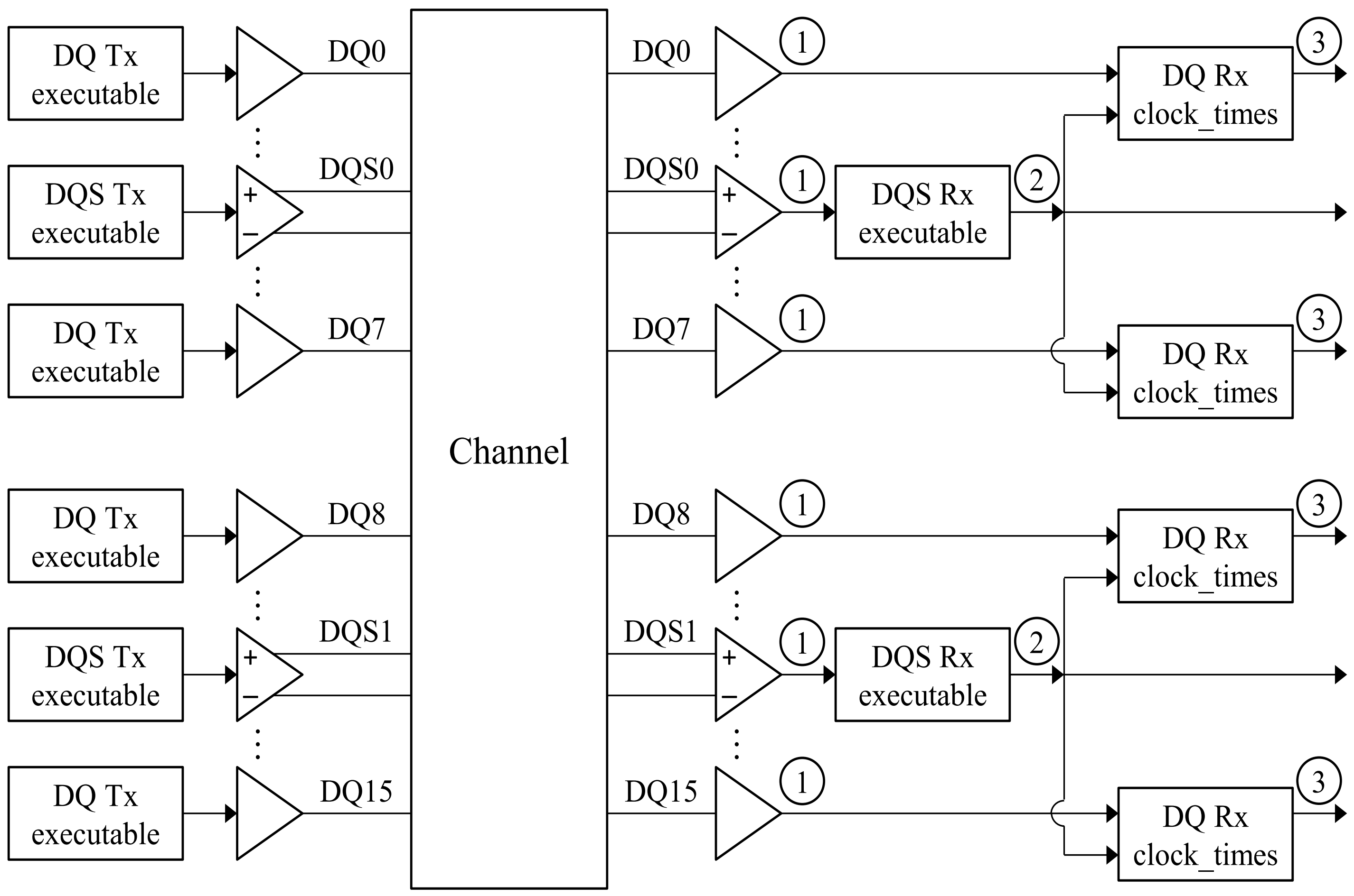
PAM3 Example



BIRD204 Clock Forwarding Modeling

BIRD204 has been approved for IBIS 7.1

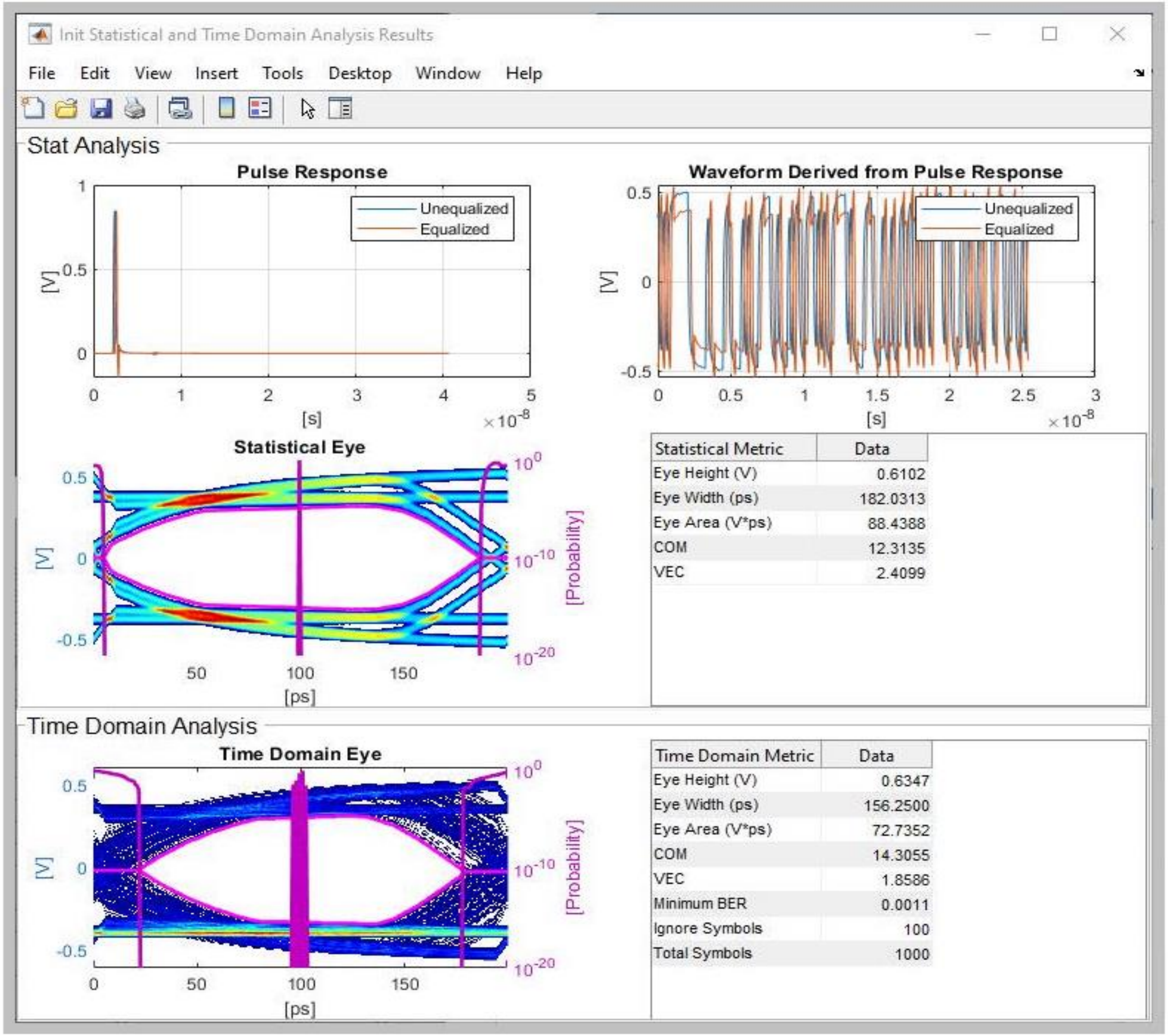
Clock Forwarding Example



Step 1: compute analog channel output according to IBIS 5.1-7.0 (crosstalk taken into account)
Step 2: compute output of all DQS Rx executable models according to IBIS 5.1-7.0
Use either DQS Rx clock_times or wave output values as DQ Rx clock_times input values
Step 3: compute output of all DQ Rx executable models

Simulation Results

Note that Clock Forwarding only affects the Time Domain Results

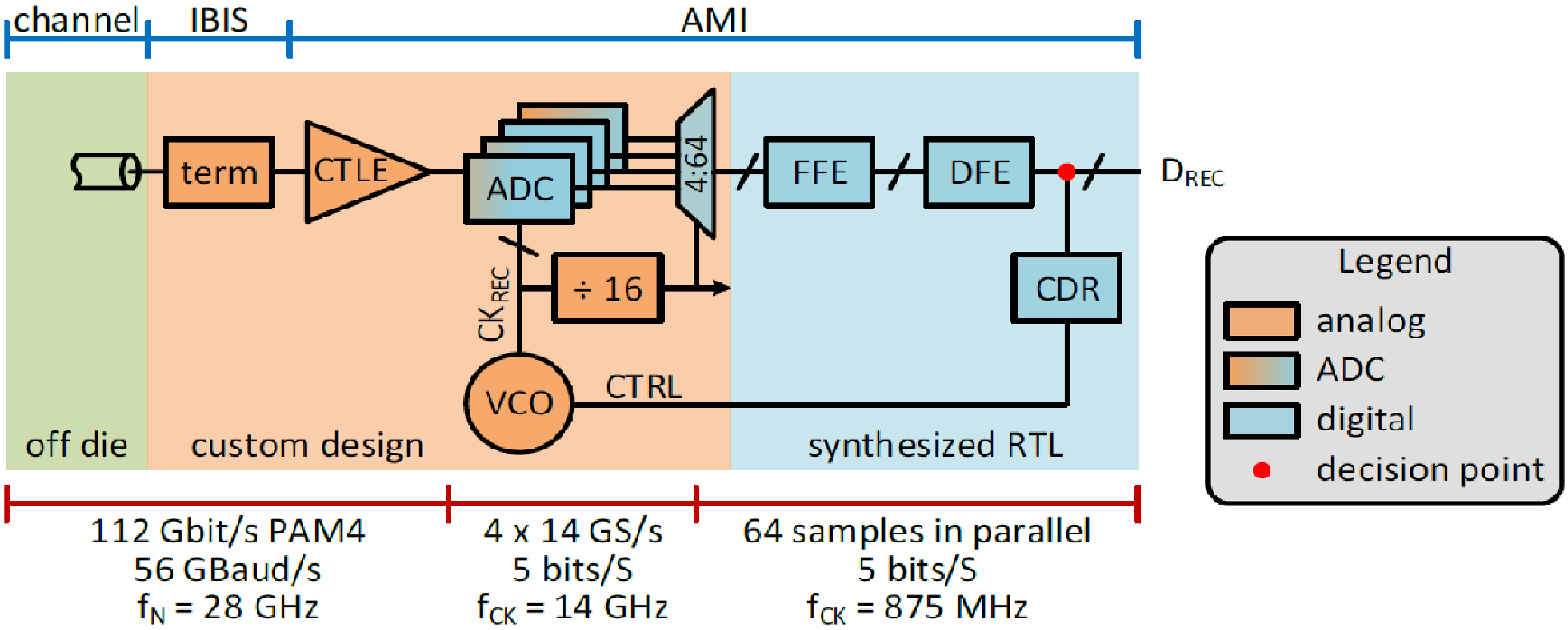


PAM4 Rx with ADC (Analog to Digital Converter)

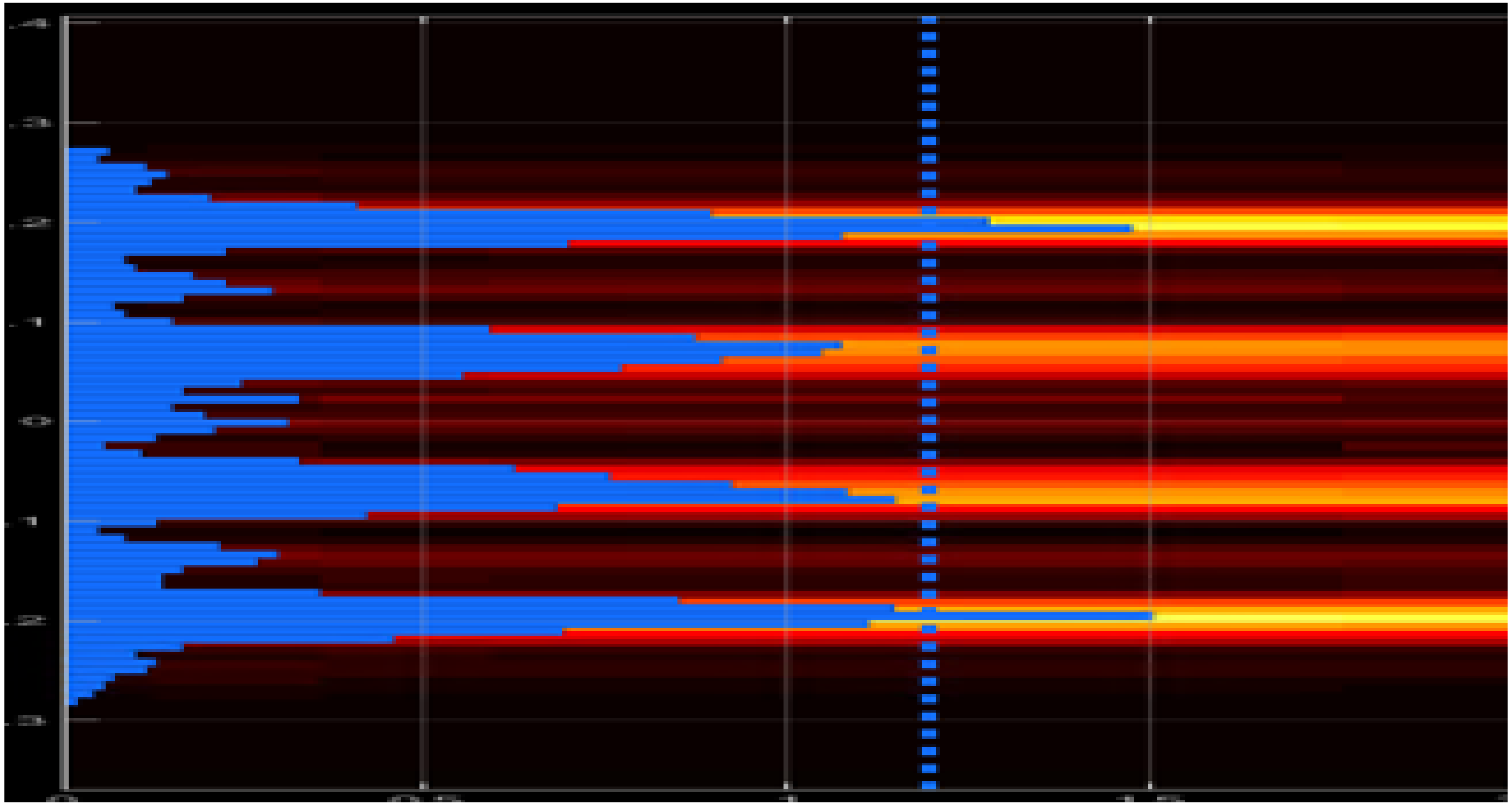
Architectural 112G PAM4 ADC-Based SerDes Model

- This example describes an IBIS-AMI 7.0 model for an IEEE 802.3ck receiver with a 112G PAM4 time-interleaved ADC-Based SerDes.
- The receiver model is composed of an analog front end (AFE) with CTLE and amplifier blocks. The time-interleaved ADC is further parallelized by a demux before DSP processing by the FFE and DFE. The baud-rate CDR controls the VCO which drives the ADC. This model is summarized in the following diagram.

Rx Model Description



Histogram of Vertical Slice of the Eye Diagram.
(The Output Waveform has a Single Value for Each UI)



Does ADC Based SerDes Require a BIRD?

- Output waveform has one value per UI, and may not be sufficient to evaluate performance
- Signal to Noise is used to evaluate performance and could be reported as an optional AMI Reserved_Parameter (Usage Out, Type Float).