GDDR6X IBIS Modeling

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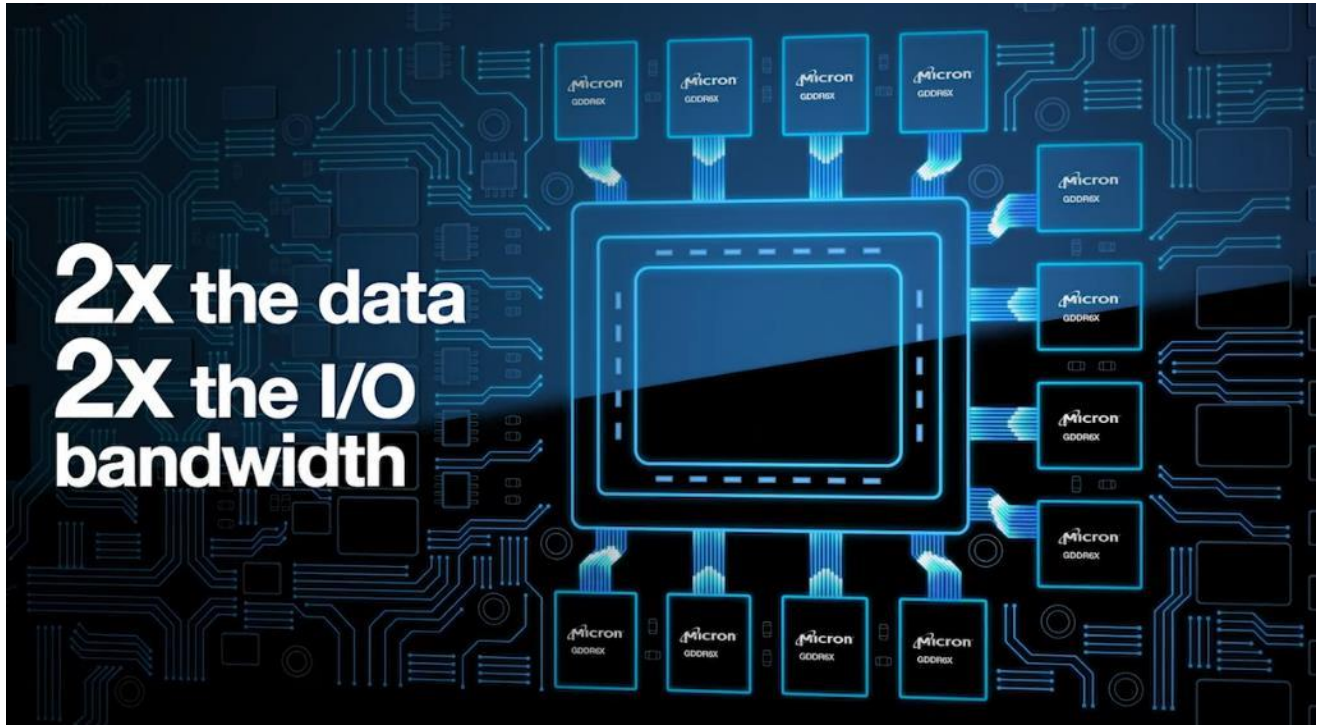
What's New?

- Micron introduced new Graphics DDR memory – GDDR6X
  - https://www.micron.com/products/ultra-bandwidth-solutions/gddr6x
  - Micron Technical Brief
- First use of single-ended PAM4 I/O signaling
- Pushes single-ended I/O speeds beyond 16 Gb/s, targeting up to 32 Gb/s



PAM4 Benefit – Beyond 16 Gb/s

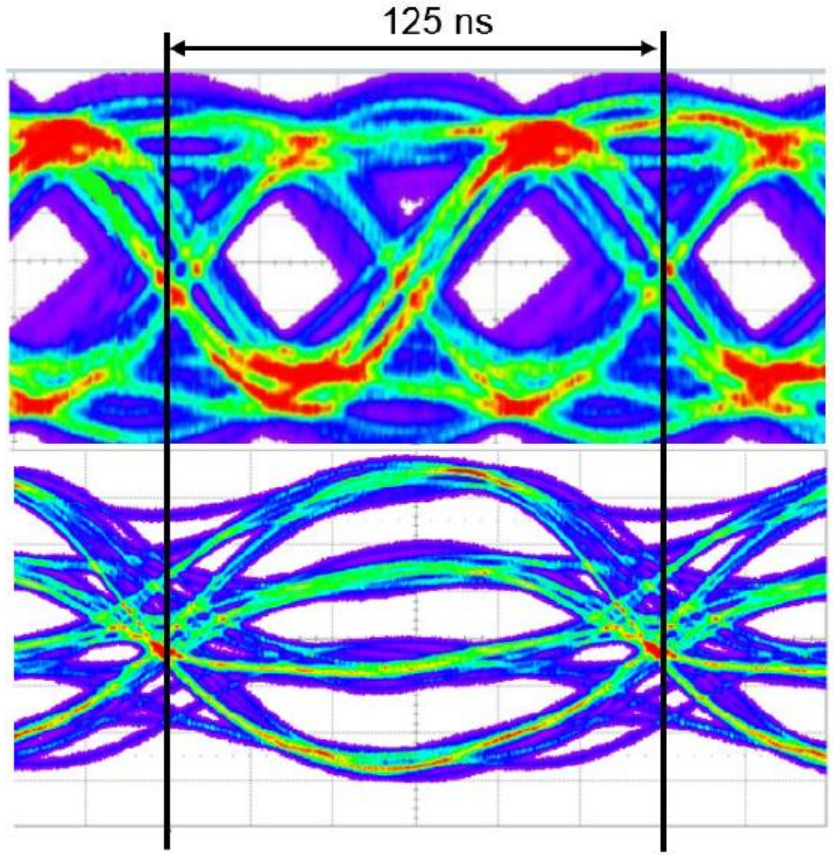
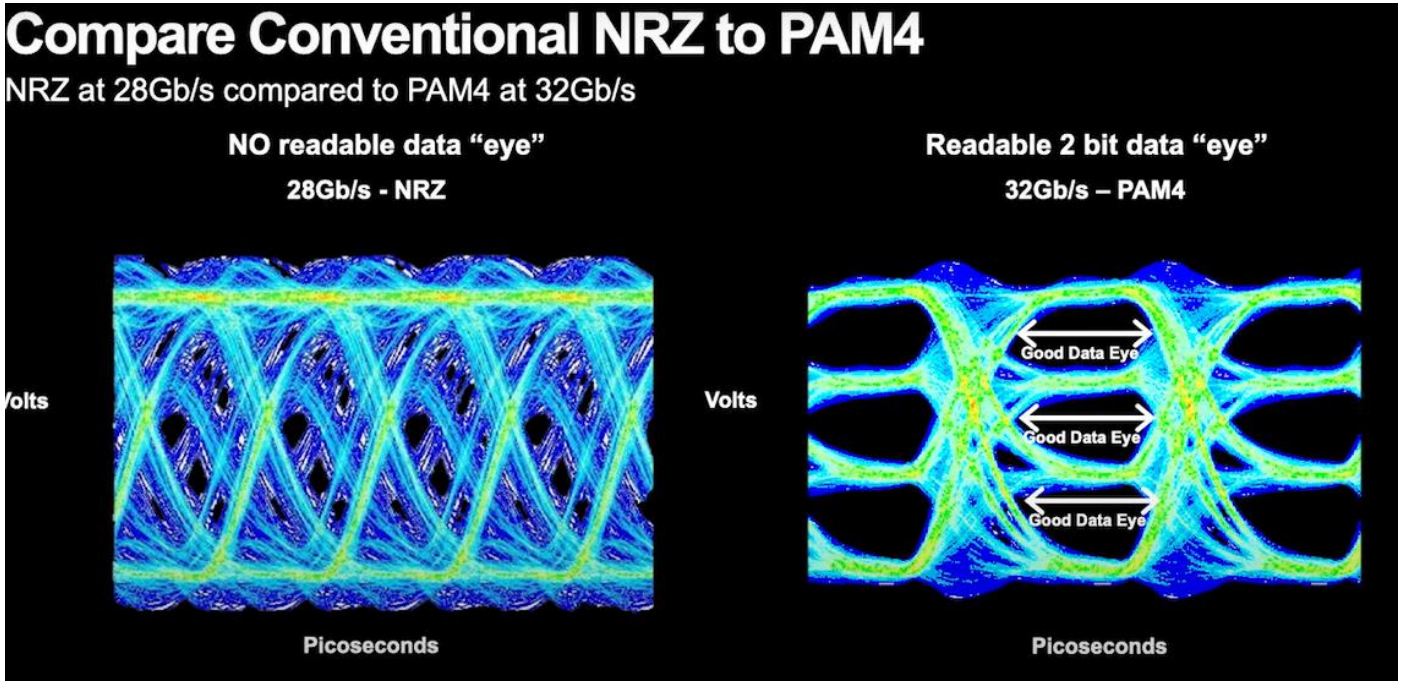


Figure 2: Data Eye Comparison Between GDDR6 (top) and GDDR6X (bottom) That Shows the Timing for a 2 Bits Data Transfer at 16Gb/s



Tx/Rx Specs

- Tx/Rx Equalization
- VDD/VDDQ @ 1.25V or 1.35V
- Datarate (today): 19Gb/s, 21 Gb/s, >21 Gb/s (per pin)
- Data is gray-coded
- V_{REFD} level internal per pin (64 steps), 3 sub-receivers per pin
- 40 and 48 Ω ODT

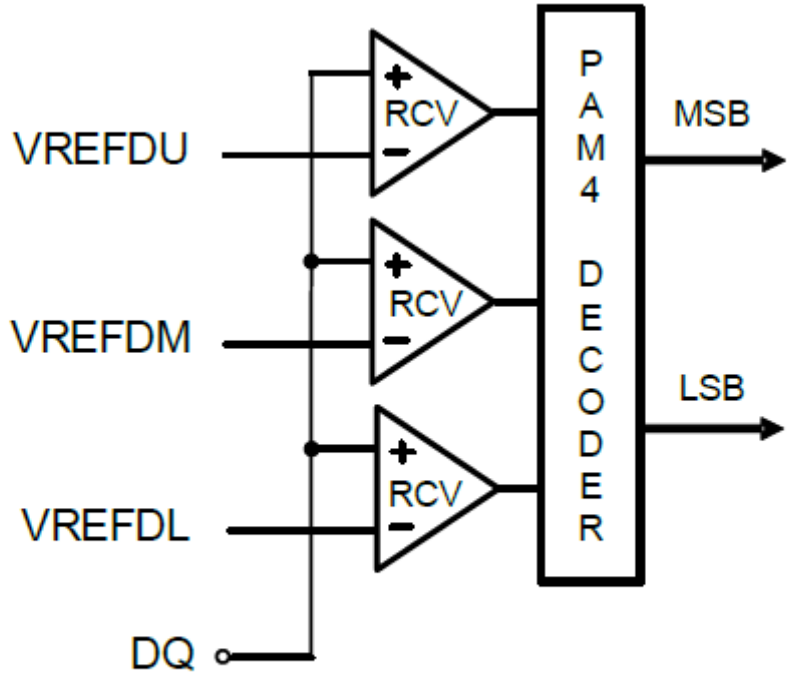


Figure 4: PAM4 Receiver

Tx Impedances

- Tx implemented with 60 and120 Ω PU/PD legs

Logical	Symbol	Physical
10	+3	
11	+1	
01	-1	
00	-3	

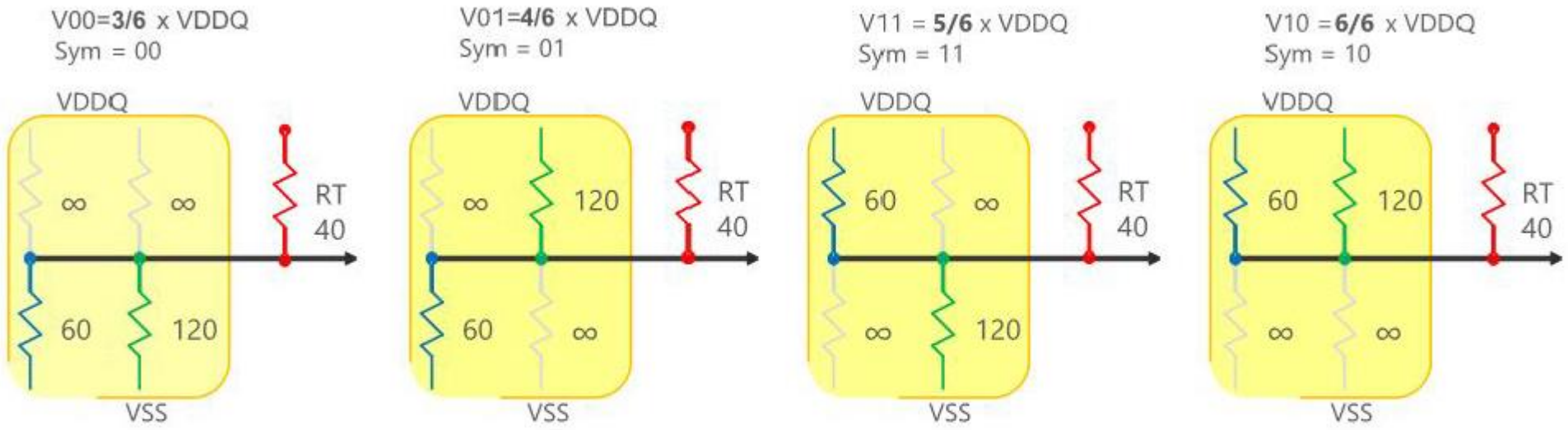
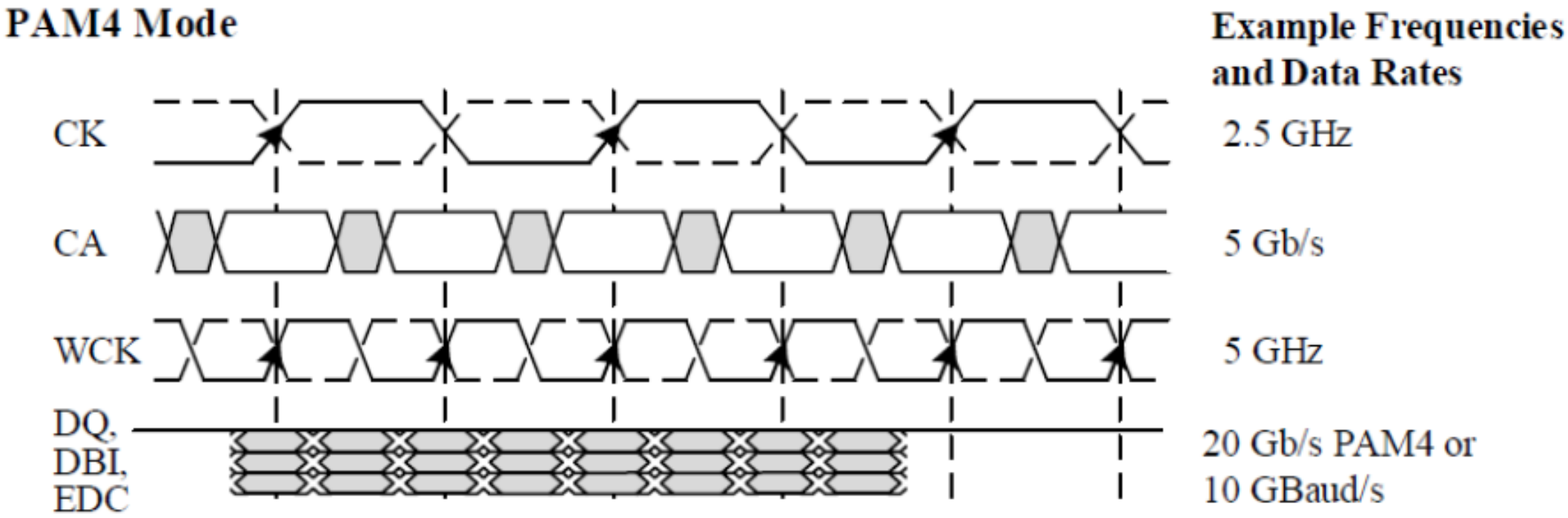


Figure 5: PAM4 Impedance Scheme

Clocking


PAM4 Mode
Example Frequencies and Data Rates
CK
2.5 GHz
CA
5 Gb/s
WCK
5 GHz
DQ, DBI, EDC
20 Gb/s PAM4 or 10 GBaud/s

Simulation and Modeling Options

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Simulating a GDDR6X Tx

- Transient Simulation
  - SPICE transistor-level model
    - Most accurate, slow simulation
  - IBIS (doesn't exist)
  - Verilog-A (could be used as a prototype for future IBIS single-ended PAM4 model keywords/extensions)
    - Accurately models 60 and120 Ω driver legs and all multi-level edge transitions
- IBIS-AMI Statistical and Time-domain Simulation
  - Use existing IBIS-AMI simulation engine
  - Traditional Tx models with PAM4 modulation
    - IBIS buffer full swing model (~40 Ω for 00-11 transition) with I-V and V-t data
    - Ideal Tx with impedance and slew rate approximating pulldown characteristics of IBIS model
  - Simulation engine options
    - Traditional rising-edge ramp for channel characterization and impulse response creation
    - Multi-edge channel characterization (uses superposition to build waveform input for Rx GetWave processing)
      - Used to improve non-linearity modeling of single-ended Tx

Verilog-A Modeling

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Background

- This single-ended PAM4 model is based on the well-known 2-equations, 2-unknowns algorithm
  - The algorithm was described and explained at the DAC 2003 IBIS Summit
    - http://www.ibis.org/summits/jun03a/muranyi1.pdf
    - That presentation used VHDL-AMS as the modeling language
    - A library of analog macromodel elements was developed in VHDL-AMS and Verilog-A and posted in 2006
    - https://ibis.org/atm_wip/element_lib/VHDL-AMS_element_library_SMASH_test.zip
    - https://ibis.org/atm_wip/element_lib/Verilog-A_element_library_HSPICE_test.zip
  - A modified version of the basic algorithm was introduced at the DATE05 IBIS Summit in 2005
    - http://www.ibis.org/summits/mar05/muranyi.pdf
    - The modifications provided a more accurate Pre/de-emphasis buffer model (a hot topic in those days)
- This PAM4 model extends the idea used in the Pre/de-emphasis model
  - The model uses multiple I-V and V-t tables that describe the transitions between the various voltage levels
  - A state machine is used to select the appropriate I-V and V-t tables for any given transition

The challenge of PAM4 stimulus in legacy IBIS

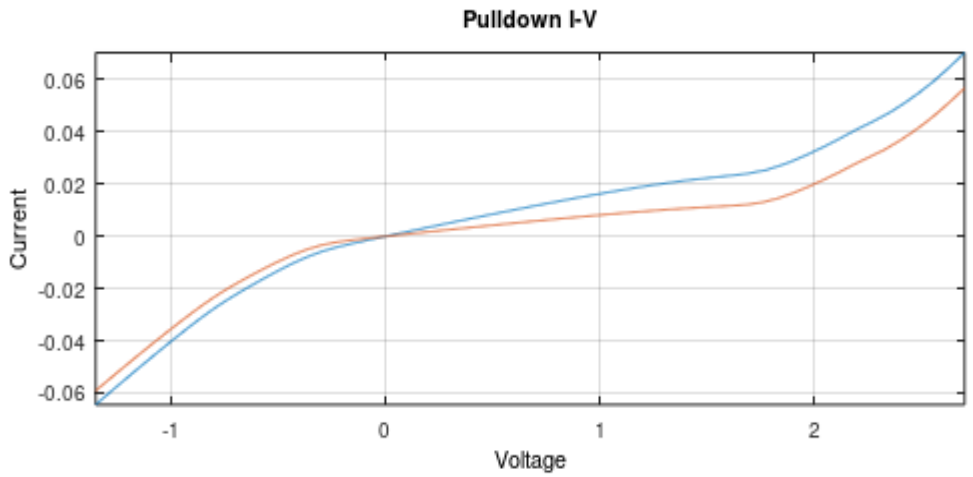
- Problem:

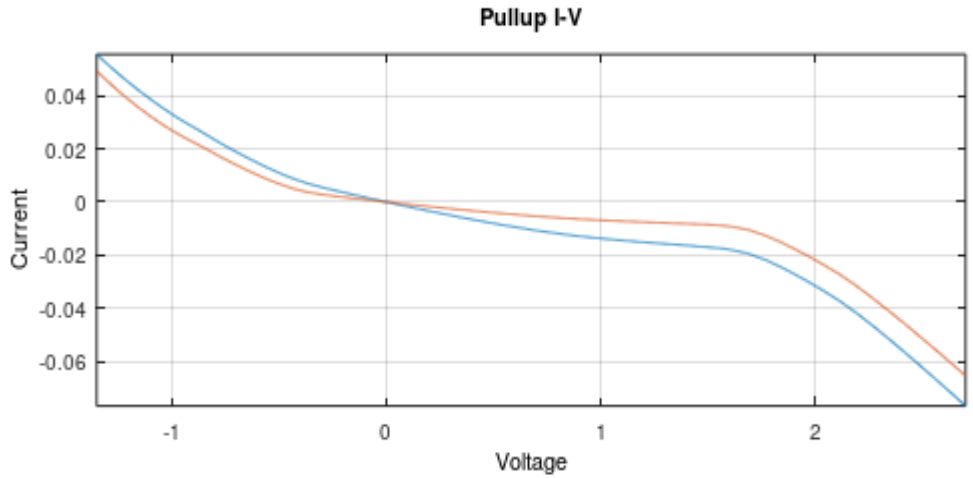
- Since the model is implemented using the [External Model] keyword inside a [Model] keyword, only a binary digital stimulus is available (‘1’ and ‘0’), but for PAM4 we need four logic states

- This limitation was solved by making use of an integer vector parameter which contains the values of the states
  - The “D_drive” stimulus is used as if it was a “clock” signal
  - When D_drive changes its state, a value is read from the integer vector parameter to determine the state of the output
  - The elements of the stimulus vector may have four values, ‘-3’, ‘-1’, ‘1’ and ‘3’
  - If the simulation runs longer than the number of elements in the vector, the vector index gets reset and the cycle repeats (wraps around)

Working with multiple I-V and V-t tables

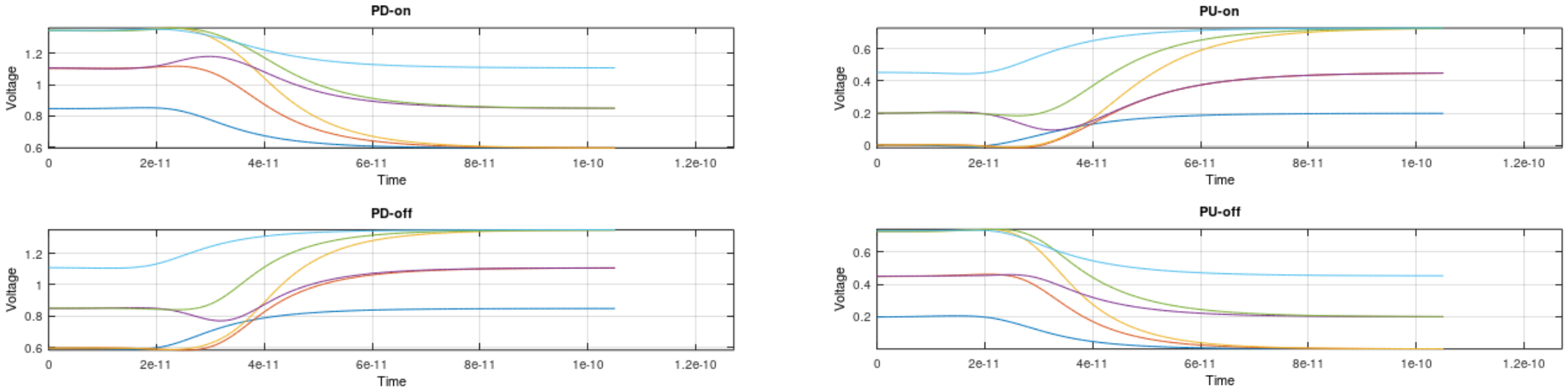
- Two sets of I-V curves were extracted from the transistor level SPICE model
  - One for the “60 Ω leg” of the buffer, and one for the “120 Ω leg” of the buffer
  - The four PAM4 voltage levels are achieved by the various parallel or series combinations of these legs
    - For the parallel combination (states ‘-3’ or ‘3’), the two I-V curves are summed and used either in the pullup or the pulldown I-V table of the model
    - For the series combination (states ‘-1’ or ‘1’), one of the I-V curves is used in one of the I-V tables (pullup or pulldown), and the other I-V curve is used in the other I-V table (pulldown or pullup)





Working with multiple I-V and V-t tables (cont'd)

- There are a total of six possible transitions between the four states
- For each of these transitions a corresponding pullup-on, pullup-off, pulldown-on and pulldown-off waveform was extracted with the appropriate V_fixture and R_fixture combinations from the transistor level SPICE model (a total of 24 waveforms)
- Each of these waveforms (or V-t tables) were converted to a corresponding K-t table using the corresponding I-V data and V_fixture and R_fixture conditions



The state machine

- Since the V-t to K-t conversion needs to be executed only once (before a simulation is executed), it doesn’t have to be present in the model during the simulation
- Even though the original (2003) VHDL-AMS and Verilog-A models did include this conversion algorithm (for the sake of completeness), it is not part of this PAM4 model (to keep it simpler)
  - The V-t to K-t conversion is performed by a MATLAB script (manually)
  - The I-V and K-t tables are passed into the Verilog-A model as model parameters
  - C_comp is also included as a model parameter
- During the simulation, the state machine decides which of the six transitions should be performed next from the stimulus input and selects the corresponding set of I-V and K-t tables
- Using the I-V and K-t tables and C_comp, the analog equations define the pullup and pulldown currents in the model for the circuit simulator

Simulation Results

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GDDR6X Simulation Setup

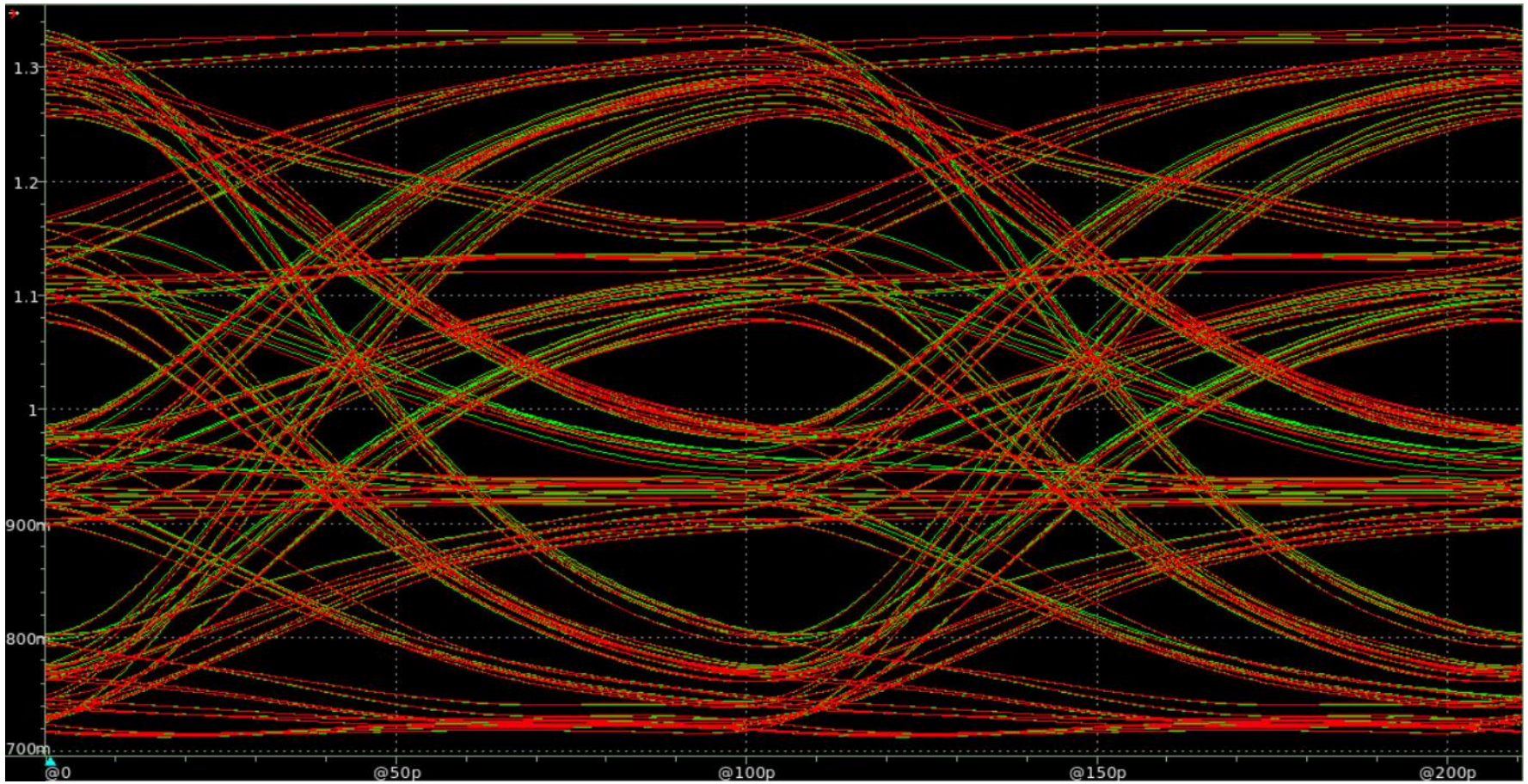
- GDDR6X-specific channel model (S-parameter converted to broadband SPICE equivalent)
- Single DQ simulation
- Datarate: 19 Gb/s PAM4 (9.5GBaud/s, 105.26ps UI)

- TX models compared
  - Transistor-level SPICE model
    - Transient simulation
  - Verilog-A model
    - Transient simulation
  - IBIS buffer full swing model (~40 Ω for 00-10 transition levels) with I-V and V-t data
    - Used for single and multi-edge channel characterization of IBIS-AMI based simulation
  - Ideal Tx with impedance and slew rate approximating pulldown characteristics of IBIS model
    - Used for single edge channel characterization of IBIS-AMI based simulation
- Rx model
  - Ideal 40 Ω termination to VDDQ

SPICE vs. Verilog-A Transient Simulation – EDA Tool A

SPICE=green, Verilog-A=red

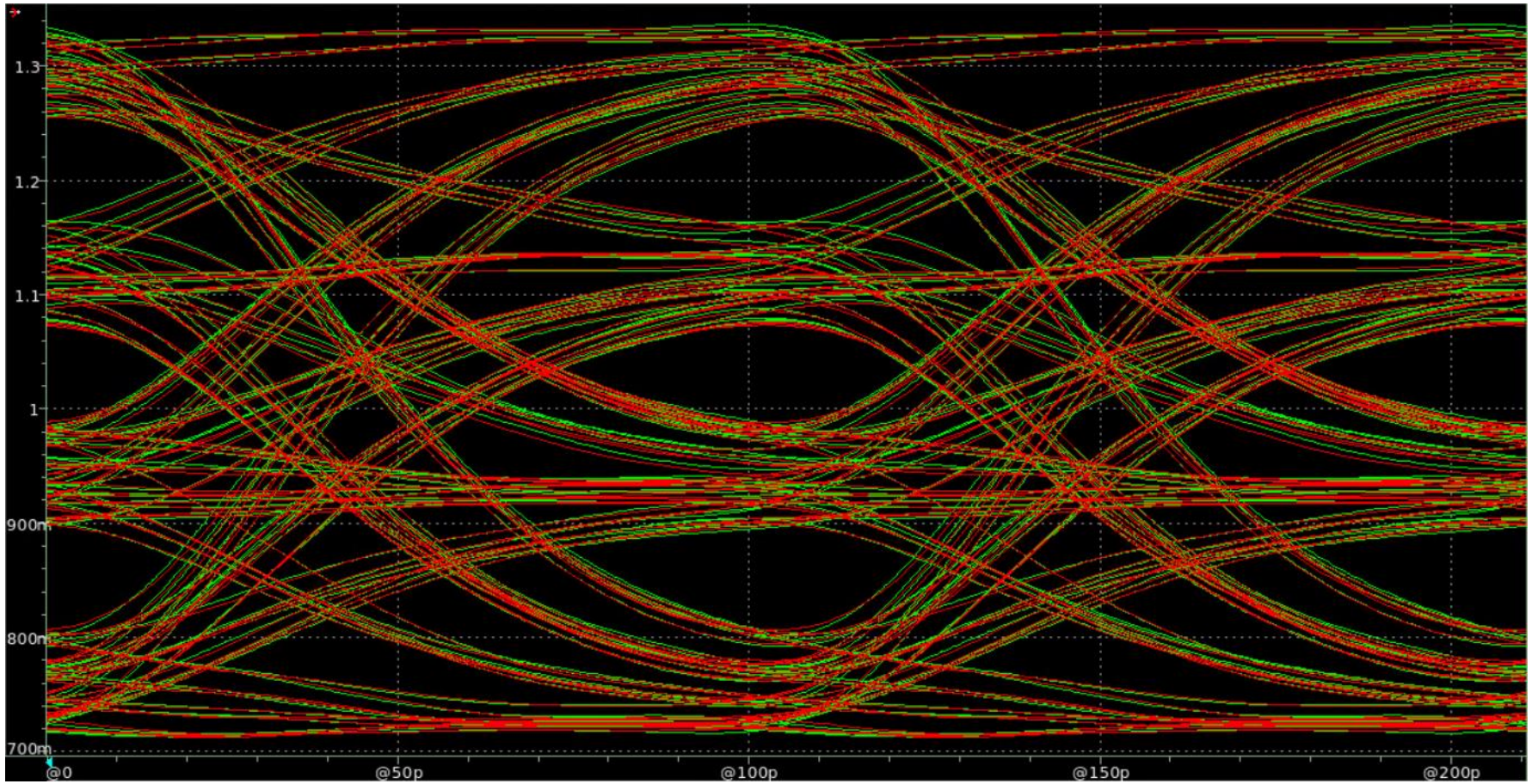
Nearly perfect match to SPICE results



SPICE vs. Verilog-A Transient Simulation – EDA Tool B

SPICE=green, Verilog-A=red

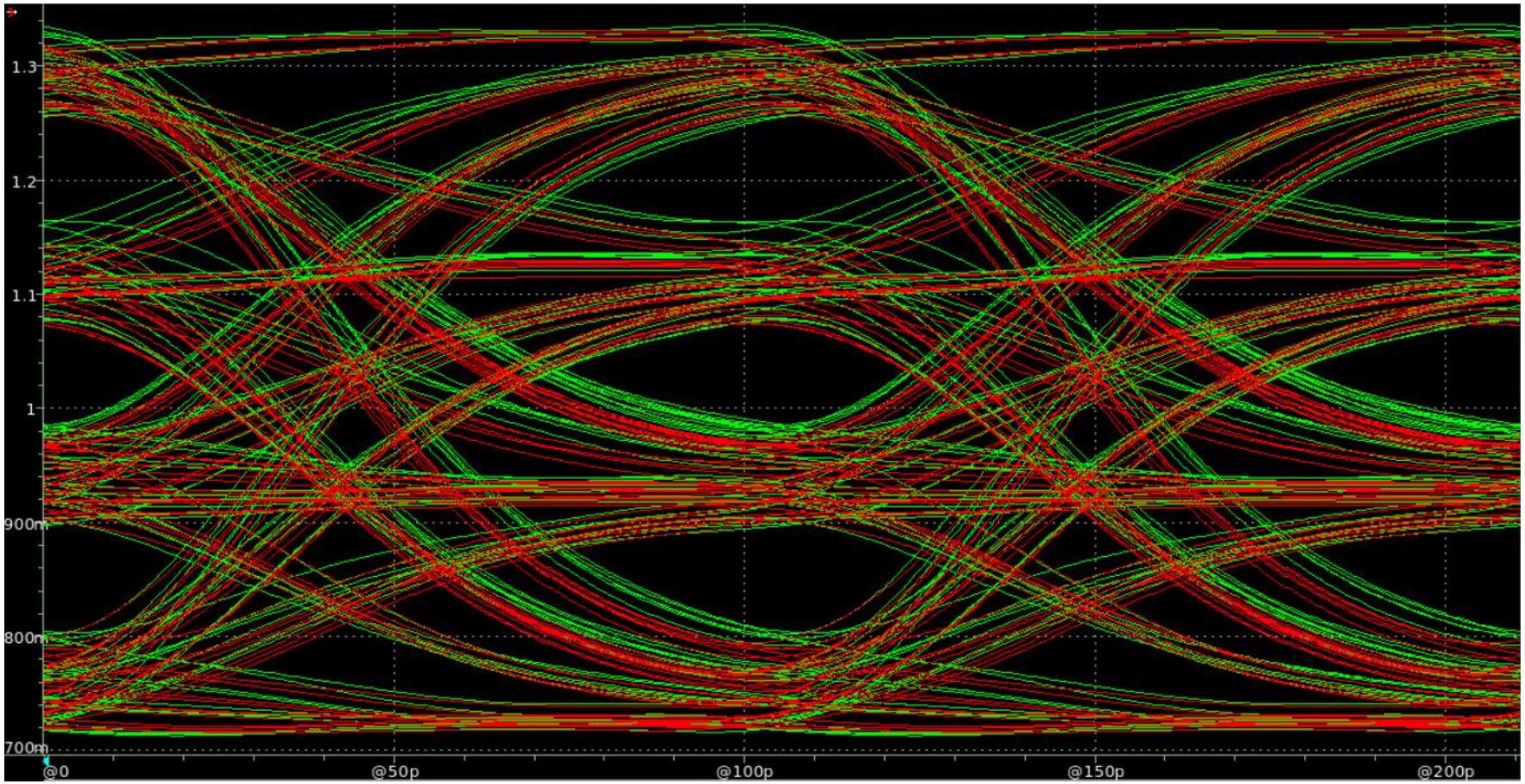
Similar match as Tool A



SPICE vs. Single Edge IBIS-AMI sim with Ideal TX

SPICE=green, IBIS-AMI=red

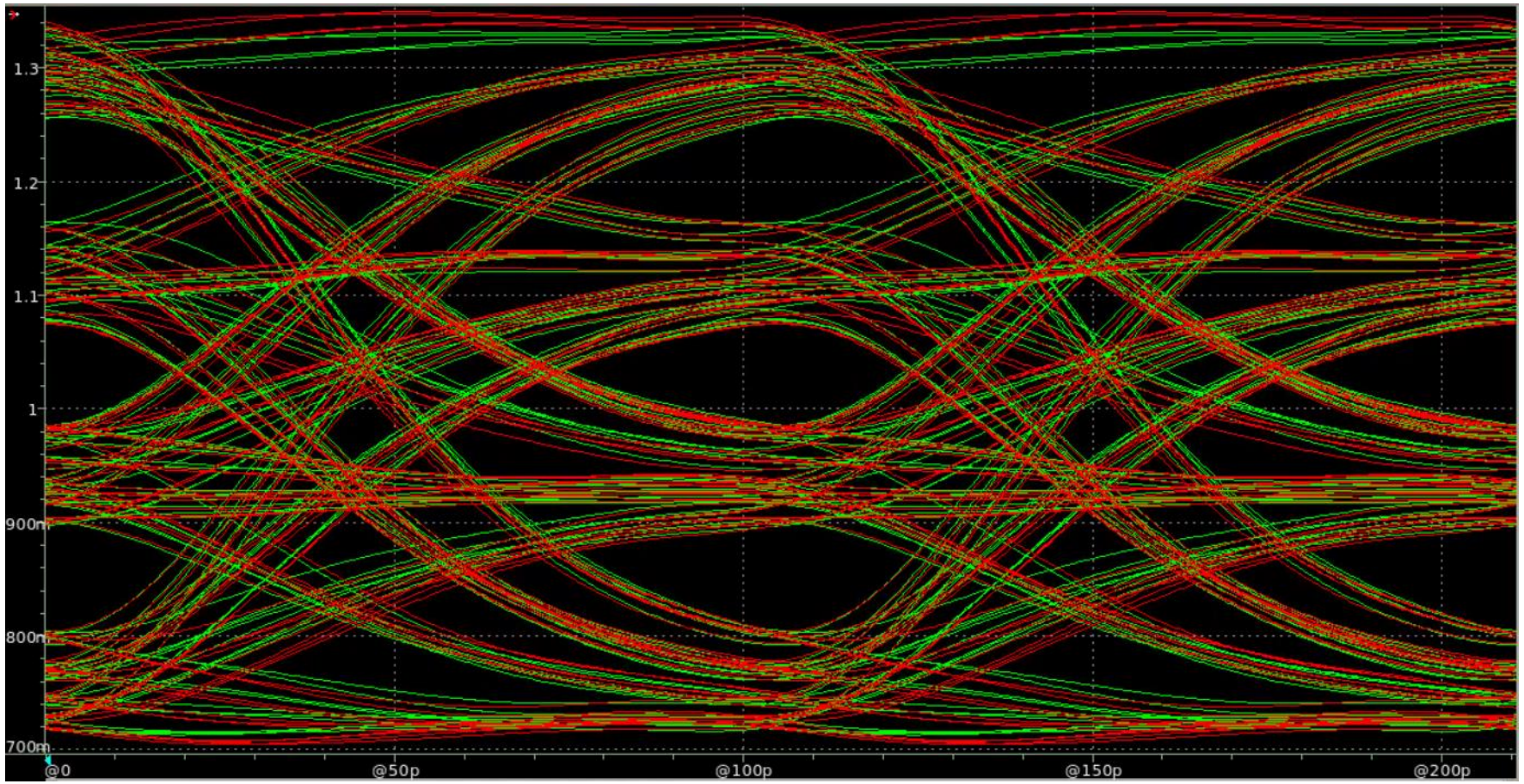
Pullup vs. pulldown impedance, linearity, and slew rate differences not modeled



SPICE vs. Single Edge IBIS-AMI sim with IBIS Buffer TX

SPICE=green, IBIS-AMI=red

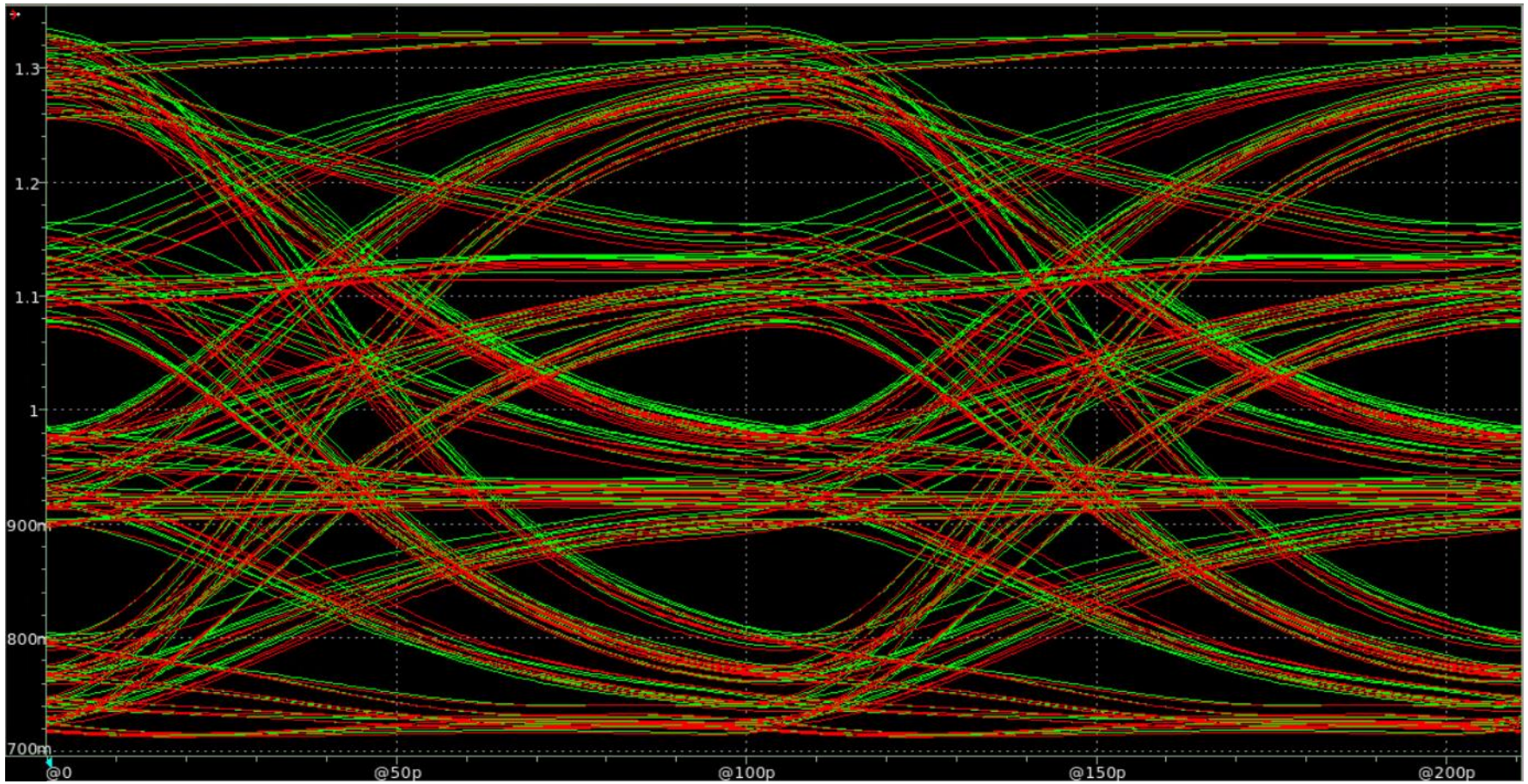
Channel characterized with 010 bit pattern



SPICE vs. Multi-edge IBIS-AMI sim with IBIS Buffer Tx

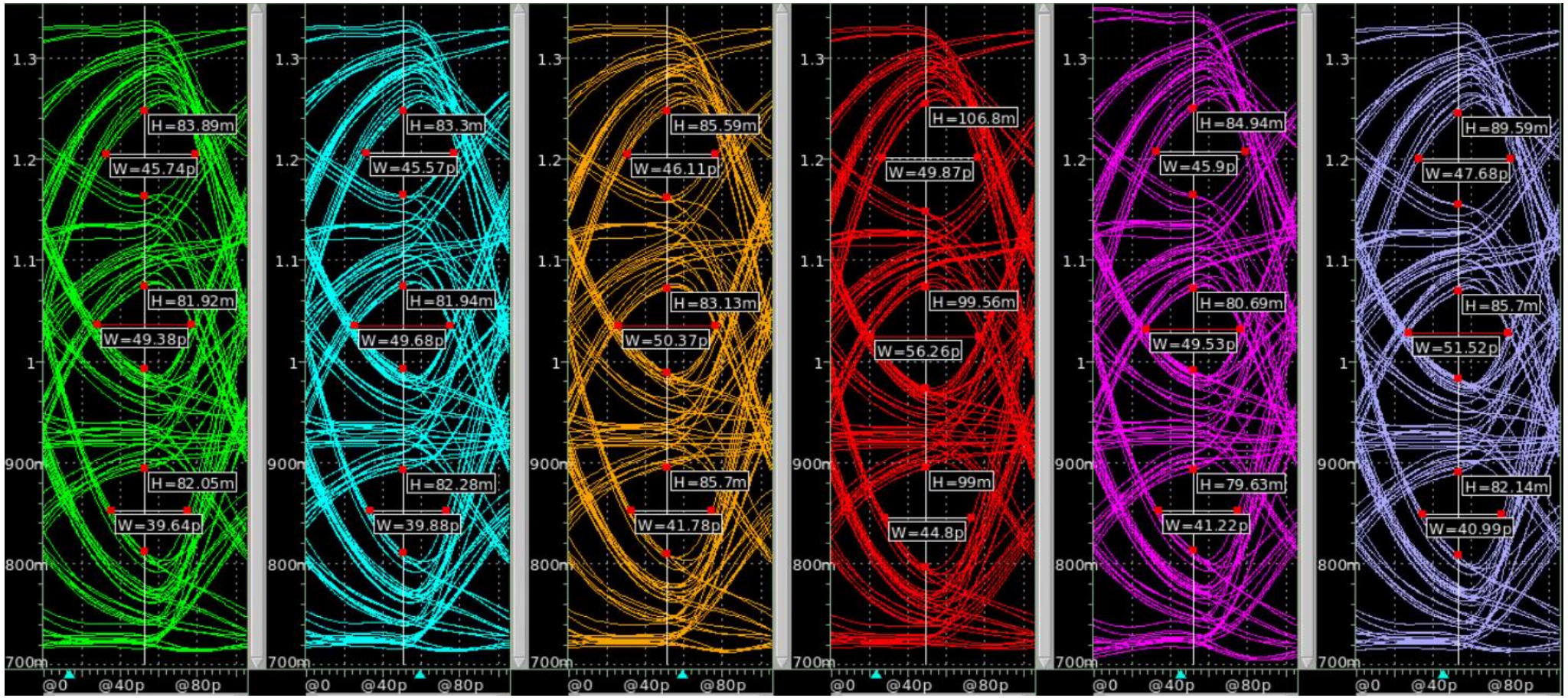
SPICE=green, IBIS-AMI=red

Channel characterized by 01 and 10 bit patterns



Eye Measurements, All Results

SPICE | Verilog-A, A | Verilog-A, B | Ideal Tx | IBIS 1 Edge | IBIS Multi-edge



Eye Width and Eye Height Comparison

	Transient Sim SPICE Tx	Transient Sim Verilog-A Tool A	Transient Sim Verilog-A Tool B	AMI – Single Edge Ideal Tx	AMI – Single Edge IBIS Buffer	AMI – Multi-Edge IBIS Buffer
Upper Eye Width (ps)	45.7	45.6	46.1	49.9	45.9	47.7
Middle Eye Width (ps)	49.4	49.7	50.4	56.3	49.5	51.5
Lower Eye Width (ps)	39.6	39.9	41.8	44.8	41.2	41.0
Upper Eye Height (mV)	83.9	83.3	85.6	106.8	84.9	89.6
Middle Eye Height (mV)	81.9	81.9	83.1	99.6	80.7	85.7
Lower Eye Height (mV)	82.1	82.3	85.7	99.0	79.6	82.1

Sampling point based on timing of max eye width of center eye.
Eye Width measured at middle of voltage swing at sampling point for all eyes.

Conclusions

- Verilog-A model shows closest match to SPICE results
  - Simulates ~10x faster than SPICE in testbench
- IBIS-AMI simulation modes developed for DDRx simulation can improve accuracy of PAM4 sims
  - Eye shape improvements seen with pullup and pulldown impedance, linearity, and slew rate differences included in traditional full swing IBIS buffer model vs. linear element
- Some edge transition timing does not match SPICE model in any IBIS-AMI simulation modes
  - Verilog-A (or IBIS buffer) model including more I-V and V-t data better captures edge timing
- What's Next?
  - Could add power-aware features (Composite Current and ISSO data table processing) to the Verilog-A model to support SSN and PDN simulations
  - Evaluate usefulness of implementing new Model_Types in IBIS (I/O_PAM4, Input_PAM4, Output_PAM4)
    - Input stimuli MSB/LSB decoding and gray-coding
    - Multiple Pullup/Pulldown curves
    - 6 sets of V-t waveforms