EMC + SIPI Virtual IBIS Summit

Fast PDN Impedance Prediction Using Deep Learning

Ling Zhang¹, Jack Juang¹, Zurab Kiguradze¹, Bo Pu¹, Shuai Jin², Songping Wu², Zhiping Yang², Jun Fan¹, Chulsoon Hwang¹

¹Missouri University of Science and Technology ²Google Inc., Mountain View, CA

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Speaker Introduction

Ling Zhang

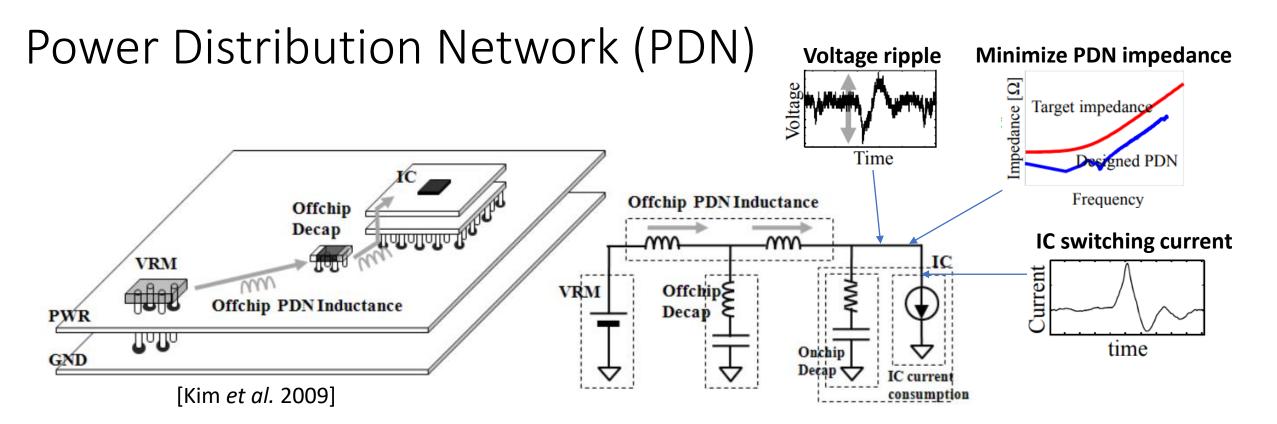
Postdoc at Zhejiang University, Hangzhou, China 2015~2021: PhD student at Missouri S&T

Co-authors:

Jack Juang, Missouri S&T
Zurab Kiguradze, Missouri S&T
Bo Pu, Missouri S&T
Shuai Jin, Google Inc.
Songping Wu, Google Inc.
Zhiping Yang, Google Inc.
Jun Fan, Missouri S&T
Chulsoon Hwang, Missouri S&T





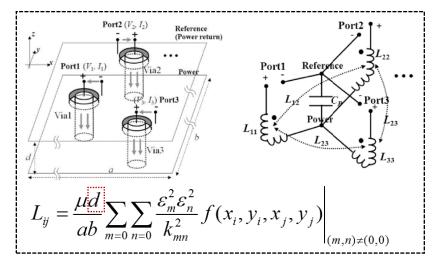


- PDN design is important to reduce voltage supply noise caused by IC switching current and ensure power integrity for IC
- Decoupling capacitors (decaps) are utilized to reduce PDN impedance so as to reduce voltage ripples



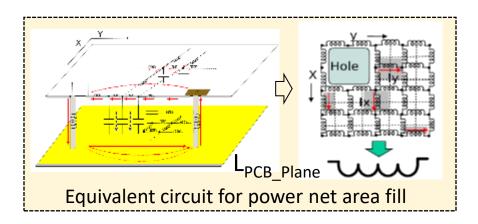
PDN Impedance Modeling

Cavity model [Kim et al. 2010]



 Cavity model: can only handle rectangle power plane shapes

Plane-Pair PEEC (PPP) Model [Wei et al. 2016]



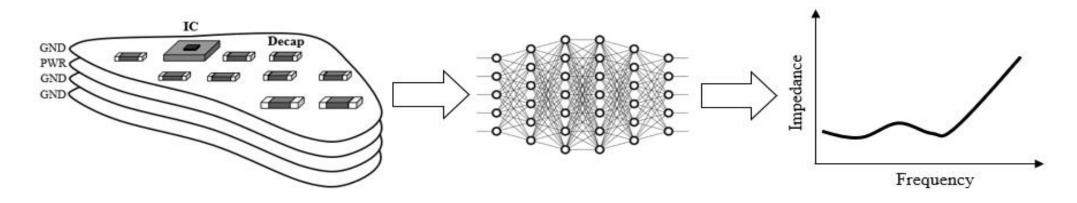
PPP: Relatively time-consuming

A fast calculation approach for multi-layer PDN with irregular board shapes is desired!!!





Objective: Deep Learning for PDN Impedance Prediction



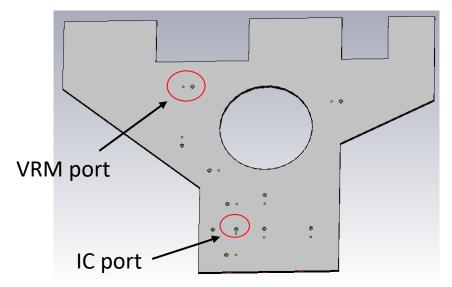
Train a deep learning model that can predict the PDN impedance given any:

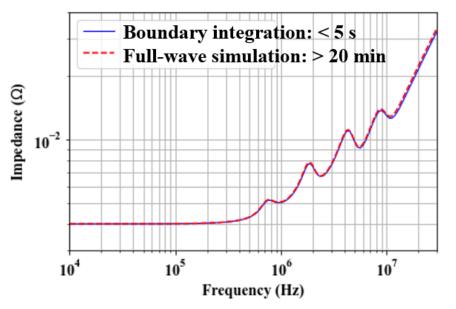
- Board shapes
- Stackup
- IC location
- Decap placement





Boundary Integration for PDN Impedance Calculation



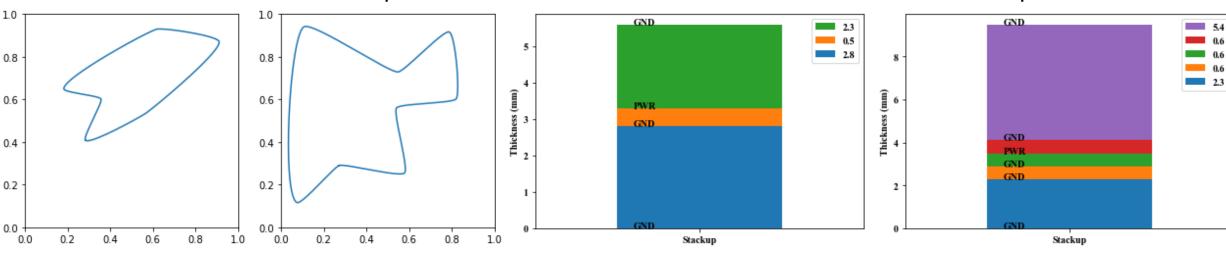


- A boundary integration method is adopted to calculate PDN impedance for arbitrary shape and stackup from DC to AC
- The boundary integration method is much faster than full-wave simulations
- L. Zhang, J. Juang, Z. Kiguradze, B. Pu, S. Jin, S. Wu, Z. Yang, and C. Hwang, "Efficient DC and AC Impedance Calculation for Arbitrary-shape and Multi-layer PDN Using Boundary Integration," *IEEE Trans. Electromagn. Compat.*, to be submitted.
- o M. Friedrich and M. Leone, "Boundary-Element Method for the Calculation of Port Inductances in Parallel-Plane Structures," *IEEE Trans. Electromagn. Compat.*, vol. 56, no. 6, pp. 1439-1447, Dec. 2014.



Generate Random Shape & Stackup





- o https://stackoverflow.com/questions/50731785/create-random-shape-contour-using-matplotlib
- o L. Zhang, J. Juang, Z. Kiguradze, B. Pu, S. Jin, S. Wu, Z. Yang, and C. Hwang, "Fast PDN Impedance Prediction Using Deep Learning," International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, accepted with minor revision.



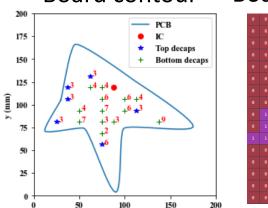
Decap Library

	Decap Parameters				
Type #	Capacitance (uF)	ESL (nH)	ESR (mΩ)	Serial number (Murata)	Size
1	0.1	0.19	34.7	GRM033C80J104KE84	0201
2	0.47	0.18	18.3	GRM033R60J474KE90	0201
3	1	0.22	15.2	GRM155B31C105KA12	0402
4	2.2	0.20	7.2	GRM155C70J225KE11	0402
5	4.7	0.28	7.1	GRM185C81A475KE11	0603
6	10	0.26	5.2	GRM188R61A106KAAL	0603
7	22	0.27	4.0	GRM188B30J226MEA0	0603
8	47	0.15	2.9	GRM219D80E476ME44	0805
9	220	0.41	1.9	GRM31CR60J227ME11	1206
10	330	0.46	1.2	GRM32EC80E337ME05	1210

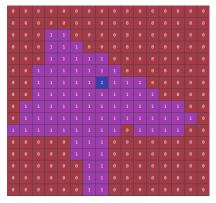


Matrix Representation

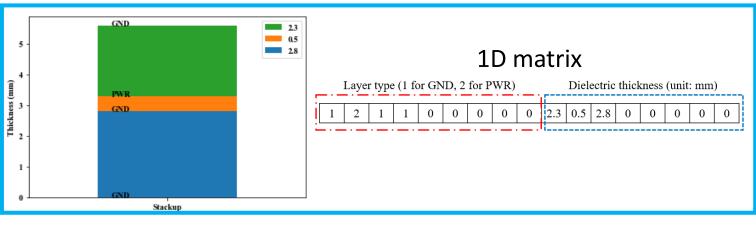
Board contour



Board shape + IC location

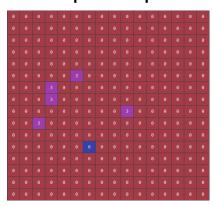


Stackup

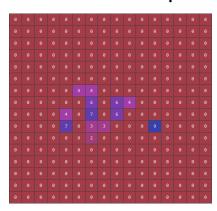


Top decaps

x (mm)



Bottom decaps



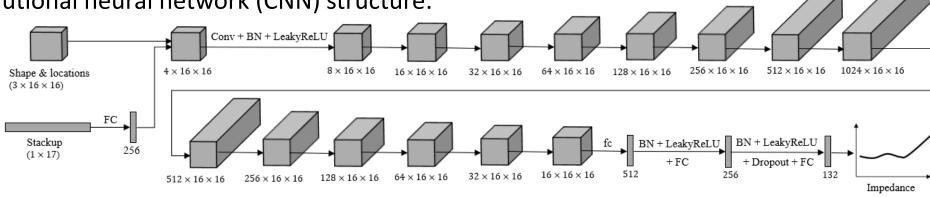
- Board information: 16×16 matrices
- Stackup (4~9 layers): 1×17 matrix
- Maximum size: 200mm×200mm; number of decap locations: 20
- IC and decap locations are generated randomly
- One unit contains one horizontal decap

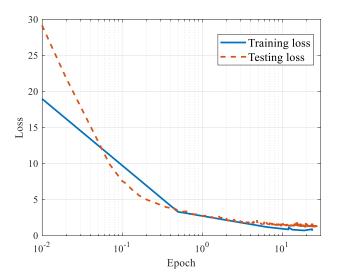
L. Zhang, et al., International Journal of Numerical Modeling: Electronic Networks, Devices and Fields, accepted with minor revision.



CNN Training

Convolutional neural network (CNN) structure:



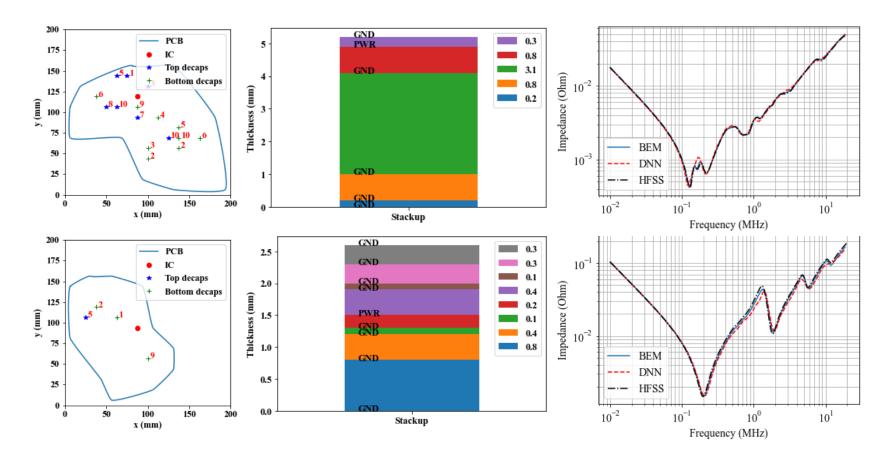


- 1.3 million board data are generated, 10,000 used for testing
- Output: dB value is used
- Loss function: root mean square error (RMSE)
- Learning rate: 0.0001; Adam optimizer; batch size 128
- Training time: 80 hours (1 NVIDIA Tesla K80 GPU)

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Test Trained Model



- RMSE for the testing data is just around 1dB
- Two testing cases are randomly picked and plotted here

Methods	Case #1	Case #2
Full-wave	35 min	40 min
BEM	10 s	30 s
DNN	0.1 s	0.1 s

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Summary

- A deep learning model is developed to fast predict the PDN impedance for arbitrarily-shaped power plane and arbitrary stackup
- The trained model can predict PDN impedance within 0.1s with a tolerable accuracy
- Code link on GitHub: https://github.com/lingzhang0319/PDN-Impedance-Prediction-Using-Deep-Learning/tree/master



Ling Zhang

Zhejiang University; Missouri S&T lingzhang_zju@zju.edu.cn; lzd76@mst.edu

Chulsoon Hwang

Missouri S&T hwangc@mst.edu

