[PSIJ Sensitivity] in IBIS

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Kinger Cai has been driving I+I strategy for Notebook platforms, and strategic PI design tool evolution in Client Computing Group. Kinger was awarded Ph. D by Shanghai Jiao Tong University in 2001, and MBA degree by W.P. Carey business school in ASU in 2008. Kinger works in signal & power integrity domains for 20+ years. Kinger holds 12 granted patents, and published 30+ papers.
Agenda

- Background
- HSIO architecture: Serial & Parallel
- Status Quo, for jitter analysis
- New system jitter analysis methodology
- [PSIJ Sensitivity] in IBIS
- [PSIJ Sensitivity] application
- Next Steps
Background

- Data speed-up => Less UI, less jitter budget
  - PCIe Gen3/4/5/6
  - LP(G)/DDR3/4/5/6
  - USB3/3.1/3.2/4, DP & THB

- Silicon Disaggregation => more complicated jitter implication
  - EMIB (Embedded Multi-die Interconnect Bridge), Foveros (Die to Die Stacking), and WoW (Wafer-on-Wafer)
  - Differentiated architecture

- Process evolution => lower operation voltage, less voltage margin
  - 22/14/10/7/6/5/4/3nm & 20A/18A
HSIO Architecture Example: Serial or Parallel

- HSIO Tx/Rx PHY with EQ, and CDR in Rx PHY
- HSIO jitter, from Data and Clock, common or independent RefCLK
- HSIO jitter, from SI & PI, of multiple power supplies’ PDNs
- HSIO jitter, of Dj and Rj, in pp or rms
Status Quo, of Jitter Analysis

- **SI & PI totally decoupled Sim, \(T_J = T_{J_{SI}} + T_{J_{PI}}(+T_{J_{PM}} + T_{J_{ctrl1}} + \ldots)\)**
  - Over-design with direct superposition of the worst SI & PI cases in TD
    - PSIJ heavily frequency-dependent to each circuit block cascaded in the path
    - Jitter contribution from the other circuitry might not be included
    - Jitter contribution significantly different upon different process technology, even for same IP

- **SI-PI Co-Sim, \(T_J = T_{J_{Eye}}(+T_{J_{PM}} + T_{J_{ctrl1}} + \ldots)\)**
  - Xtor model based, SI&PI co-sim,
    - very time-consuming, almost impossible to include all circuitry
  - Power-aware IBIS-AMI based sim
    - More efficient, but less accuracy
    - Jitter contribution from the other circuitry not included
  - PM noise needs lab verification
Jitter Analysis with PSIJ Sensitivity

- \( T_j = D_j + R_j \)
- \( R_j \) refers to an intrinsic noise, upon BER
- \( D_j \) comes from SI channel and PI noise

- \( \sum_{i=1}^{N} \text{IFFT}[\text{PSIJ}_i \ast \text{FFT}(V_{\text{noise}_i})] \)
- \( D_{j,SI} \) from SI simulation, assuming ideal power supplies
- System total \( D_j \), \( D_j = D_{j,SI} + D_{j,PI} \)

Investigating the Impact of Supply Noise on the Jitter in Gigabit I/O Interfaces
IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEPS)
Ralf Schmitt; Hai Lan; Chris Madden; Chuck Yuan, page 189-192, Oct. 2007

https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4387157
PSIJ Sensitivity Derivation

- Set up VCC_m = Vtyp + A*sin(f),
  - A = (Vmax - Vmin) / 2,
  - Keep all other power supplies at their own Vtyp

- Observe jitter impact, while sweeping f, to get PSIJ_VCC_m_ckt_i

- PSIJ_VCC_m = ∏_{i=1}^{N} PSIJ_VCC_m_ckt_i  or 
  = ∑_{i=1}^{N} PSIJ_VCC_m_ckt_i  or

- = mix of ∏_{i=A}^{B} X and ∑_{j=C}^{D} Y

- In equations, discrete {A, B, C, D} = {1, 2, ..., N}, and

- X, Y could be any combinations of PSIJ_VCC_m_ckt_i/j
Proposal of [PSIJ Sensitivity] in IBIS

- **Keyword:** [PSIJ Sensitivity] Power_signal_name (m)
- **Required:** Yes
- **Description:** Used to describe the power supply induced jitter sensitivity in PWL in frequency domain, for each power rail.
- **Usage Rules:** PSIJ Sensitivity in PWL format, for each power rail listed in [Voltage List], to evaluate the jitter impact to all the circuit blocks from its power supplies’ noise respectively.

**Example:**

```
<table>
<thead>
<tr>
<th>[PSIJ Sensitivity]</th>
<th>VDDn</th>
</tr>
</thead>
<tbody>
<tr>
<td>frequency (Hz)</td>
<td>sensitivity (ps/mv)</td>
</tr>
<tr>
<td>100000</td>
<td>3.60</td>
</tr>
<tr>
<td>1000000</td>
<td>3.10</td>
</tr>
<tr>
<td>10000000</td>
<td>4.30</td>
</tr>
<tr>
<td>100000000</td>
<td>1.90</td>
</tr>
<tr>
<td>1000000000</td>
<td>0.50</td>
</tr>
</tbody>
</table>
```

**[Voltage List]**

```
<table>
<thead>
<tr>
<th>V(name)</th>
<th>V(typ)</th>
<th>V(min)</th>
<th>V(max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDn</td>
<td>0.600</td>
<td>0.540</td>
<td>0.660</td>
</tr>
<tr>
<td>VSS</td>
<td>0.000</td>
<td>0.000</td>
<td>0.000</td>
</tr>
</tbody>
</table>
```

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Examples of [PSIJ Sensitivity] in IBIS

<table>
<thead>
<tr>
<th>Voltage List</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(name)</td>
</tr>
<tr>
<td>VDD1</td>
</tr>
<tr>
<td>VCC2</td>
</tr>
<tr>
<td>VSS</td>
</tr>
</tbody>
</table>

[End Voltage List]

<table>
<thead>
<tr>
<th>PSIJ Sensitivity</th>
<th>VDD1</th>
</tr>
</thead>
<tbody>
<tr>
<td>frequency (Hz)</td>
<td>sensitivity (ps/mv)</td>
</tr>
<tr>
<td>100000</td>
<td>1.1</td>
</tr>
<tr>
<td>1000000</td>
<td>2.2</td>
</tr>
<tr>
<td>10000000</td>
<td>7.8</td>
</tr>
<tr>
<td>100000000</td>
<td>4.0</td>
</tr>
<tr>
<td>1000000000</td>
<td>3.9</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PSIJ Sensitivity</th>
<th>VCC2</th>
</tr>
</thead>
<tbody>
<tr>
<td>frequency (Hz)</td>
<td>sensitivity (ps/mv)</td>
</tr>
<tr>
<td>100000</td>
<td>2.7</td>
</tr>
<tr>
<td>1000000</td>
<td>3.0</td>
</tr>
<tr>
<td>10000000</td>
<td>4.9</td>
</tr>
<tr>
<td>100000000</td>
<td>4.1</td>
</tr>
<tr>
<td>1000000000</td>
<td>3.8</td>
</tr>
</tbody>
</table>
Quick IP Selection, based upon [PSIJ Sensitivity]

- Same IP is better:
  - from vendor2 than
  - from vendor1

- Same IP is better:
  - upon process1 than
  - upon process2

- Same IP is the best
  - from vendor2 and
  - upon process1.
Next Steps

▪ Submit IBIS BIRD to include [PSIJ Sensitivity] in IBIS.
▪ Call for EDA vendors to support [PSIJ Sensitivity] in IBIS
▪ Call for chip vendors to support [PSIJ Sensitivity] in IBIS
▪ Call for platform designers to support [PSIJ Sensitivity] in IBIS
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