

# [PSIJ Sensitivity] in IBIS

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# Presenter



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Kinger Cai has been driving I+I strategy for Notebook platforms, and strategic PI design tool evolution in Client Computing Group. Kinger was awarded Ph. D by Shanghai Jiao Tong University in 2001, and MBA degree by W.P. Carey business school in ASU in 2008. Kinger works in signal & power integrity domains for 20+ years. Kinger holds 12 granted patents, and published 30+ papers.

# Agenda

- Background
- HSIO architecture: Serial & Parallel
- Status Quo, for jitter analysis
- New system jitter analysis methodology
- [PSIJ Sensitivity] in IBIS
- [PSIJ Sensitivity] application
- Next Steps

# Background

- Data speed-up => Less UI, less jitter budget

- PCIe Gen3/4/5/6
- LP(G)/DDR3/4/5/6
- USB3/3.1/3.2/4, DP & THB



- Silicon Disaggregation => more complicated jitter implication

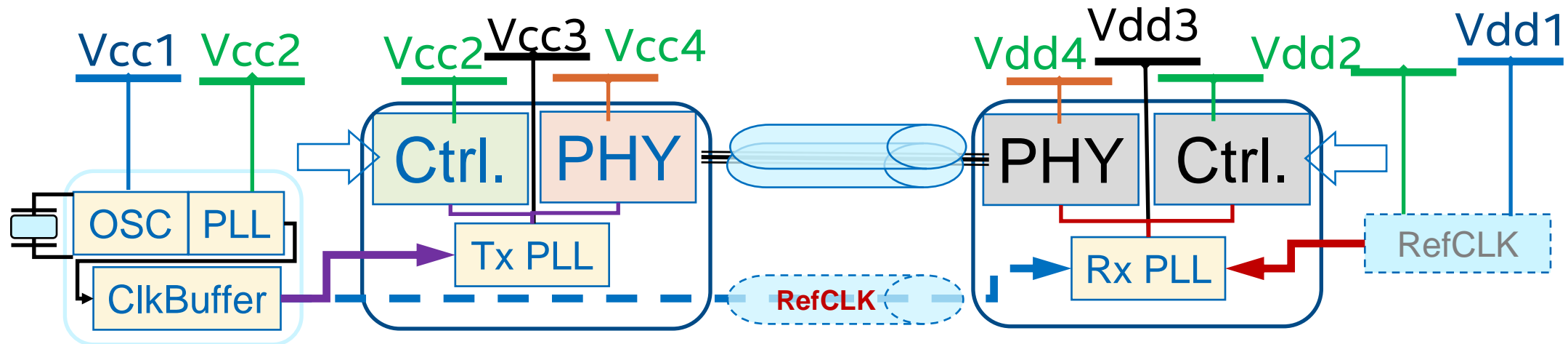
- EMIB (Embedded Multi-die Interconnect Bridge), Foveros (Die to Die Stacking), and WoW (Wafer-on-Wafer)
- Differentiated architecture

- Process evolution => lower operation voltage, less voltage margin

- 22/14/10/7/6/5/4/3nm & 20A/18A

# HSIO Architecture Example: Serial or Parallel

- HSIO Tx/Rx PHY with EQ, and CDR in Rx PHY
- HSIO jitter, from Data and Clock, common or independent RefCLK
- HSIO jitter, from SI & PI, of multiple power supplies' PDNs
- HSIO jitter, of Dj and Rj, in pp or rms

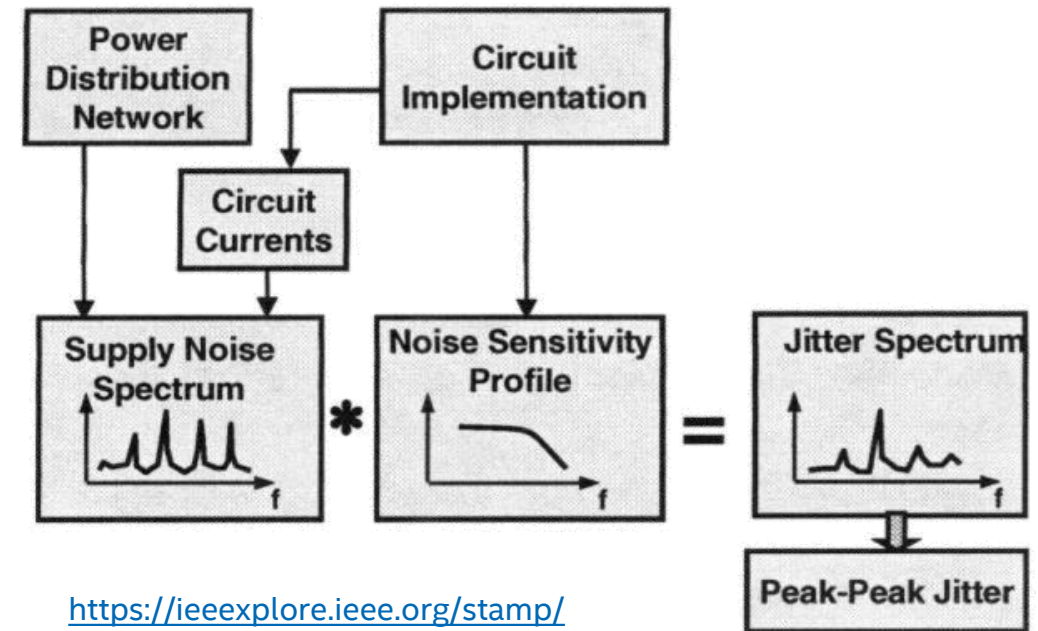


# Status Quo, of Jitter Analysis

- SI & PI totally decoupled Sim,  $T_j = T_{j-SI} + T_{j-PI} (+T_{j-PM} + T_{j-ctrl1} + \dots)$ 
  - Over-design with direct superposition of the worst SI & PI cases in TD
    - PSIJ heavily frequency-dependent to each circuit block cascaded in the path
    - Jitter contribution from the other circuitry might not be included
    - Jitter contribution significantly different upon different process technology, even for same IP
- SI-PI Co-Sim,  $T_j = T_{j-Eye} (+T_{j-PM} + T_{j-ctrl1} + \dots)$ 
  - Xtor model based, SI&PI co-sim,
    - very time-consuming, almost impossible to include all circuitry
  - Power-aware IBIS-AMI based sim
    - More efficient, but less accuracy
    - Jitter contribution from the other circuitry not included
  - PM noise needs lab verification

# Jitter Analysis with PSIJ Sensitivity

- $T_j = D_j + R_j$
- $R_j$  refers to an intrinsic noise, upon BER
- $D_j$  comes from SI channel and PI noise
  
- $D_{j-PI} = \sum_{i=1}^N IFFT[PSIJ_i * FFT(Vnoise_i)]$
- $D_{j-SI}$  from SI simulation, assuming ideal power supplies
  
- System total  $D_j$ ,  $D_j = D_{j-SI} + D_{j-PI}$

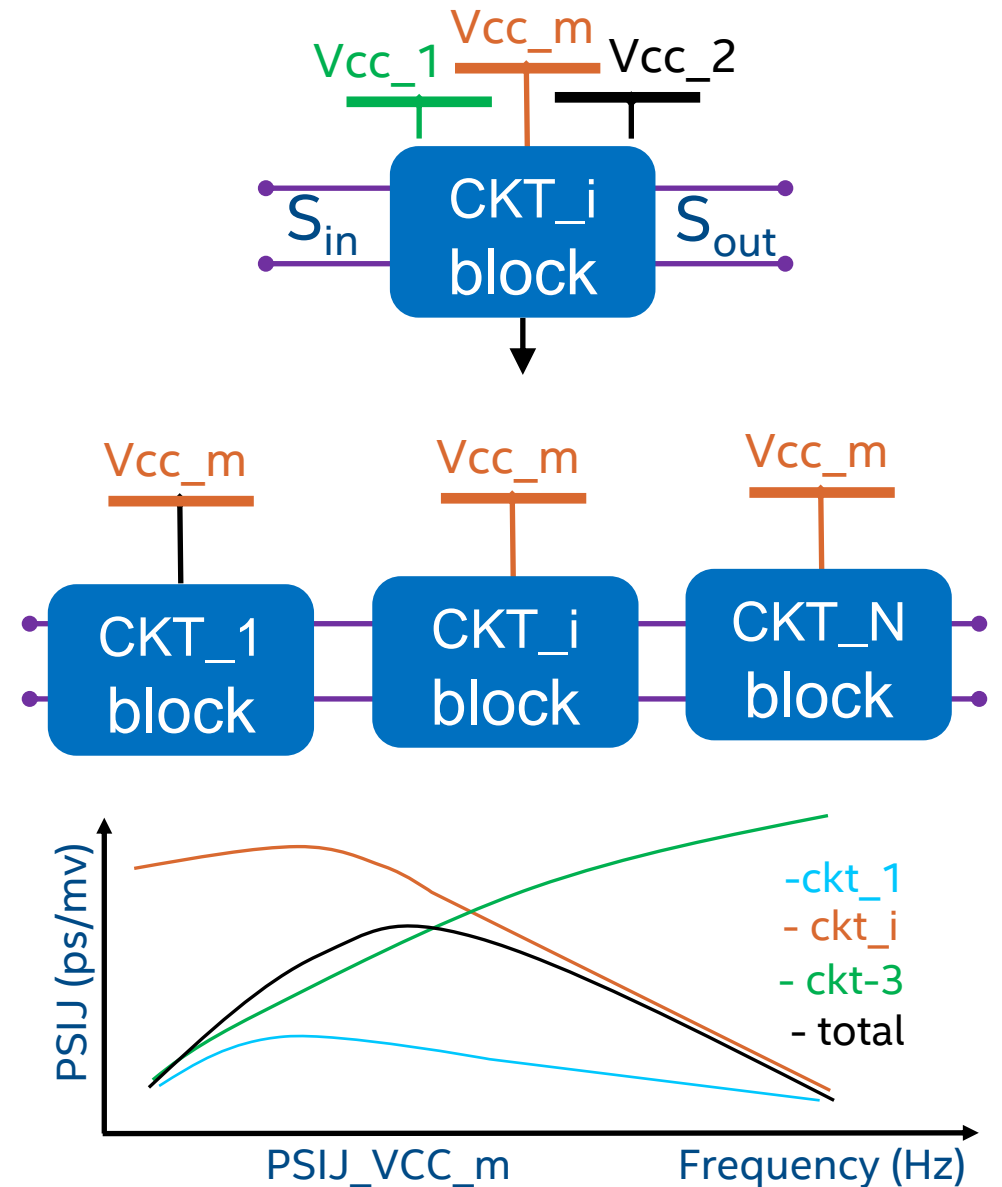


<https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4387157>

Investigating the Impact of Supply Noise on the Jitter in Gigabit I/O Interfaces  
IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEPS)  
Ralf Schmitt; Hai Lan; Chris Madden; Chuck Yuan, page 189-192, Oct. 2007

# PSIJ Sensitivity Derivation

- Set up  $VCC_m = V_{typ} + A \cdot \sin(f)$ ,
  - $A = (V_{max} - V_{min}) / 2$ ,
  - Keep all other power supplies at their own  $V_{typ}$
- Observe jitter impact, while sweeping  $f$ , to get  $PSIJ\_VCC\_m\_ckt\_i$
- $PSIJ\_VCC\_m = \prod_{i=1}^N PSIJ\_VCC\_m\_ckt_i$  or
- $= \sum_{i=1}^N PSIJ\_VCC\_m\_ckt_i$  or
- = mix of  $\prod_{i=A}^B X$  and  $\sum_{j=C}^D Y$
- In equations, discrete  $\{A, B, C, D\} = \{1, 2, \dots, N\}$ , and
- $X, Y$  could be any combinations of  $PSIJ\_VCC\_m\_ckt_{i/j}$





# Proposal of [PSIJ Sensitivity] in IBIS

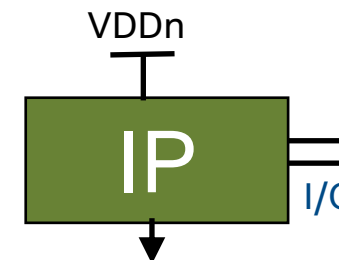
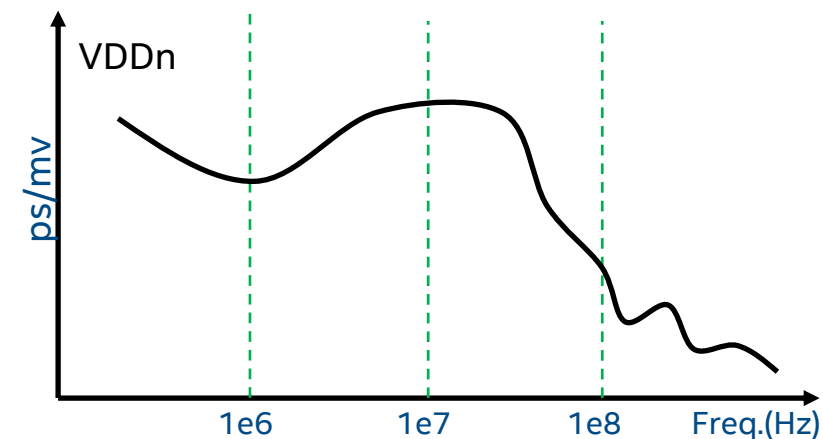
- **Keyword:** [PSIJ Sensitivity] Power\_signal\_name (m)
- **Required:** Yes
- **Description:** Used to describe the power supply induced jitter sensitivity in PWL in frequency domain, for each power rail.
- **Usage Rules:** PSIJ Sensitivity in PWL format, for each power rail listed in [Voltage List], to evaluate the jitter impact to all the circuit blocks from its power supplies' noise respectively.

Example:

[PSIJ Sensitivity] VDDn	
frequency(Hz)	sensitivity (ps/mv)
100000	3.60
1000000	3.10
10000000	4.30
100000000	1.90
1000000000	0.50

[Voltage List]			
V(name)	V(typ)	V(min)	V(max)
VDDn	0.600	0.540	0.660
VSS	0.000	0.000	0.000

[End Voltage List]



# Examples of [PSIJ Sensitivity] in IBIS

[Voltage List]

V(name)	V(typ)	V(min)	V(max)
VDD1	1.000	0.900	1.100
VCC2	0.600	0.540	0.660
VSS	0.000	0.000	0.000

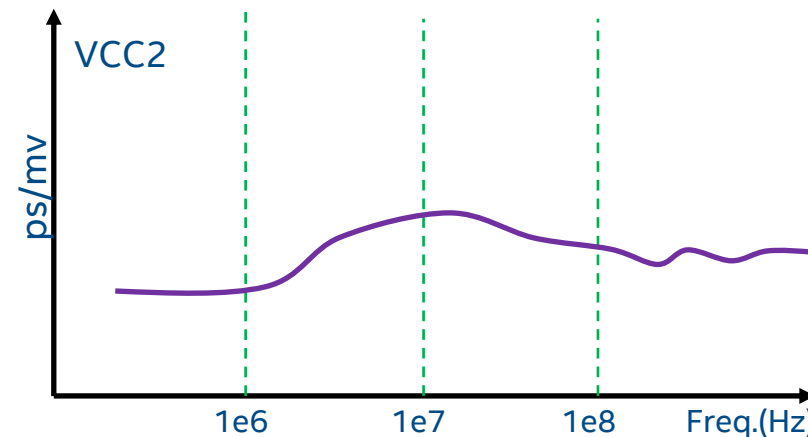
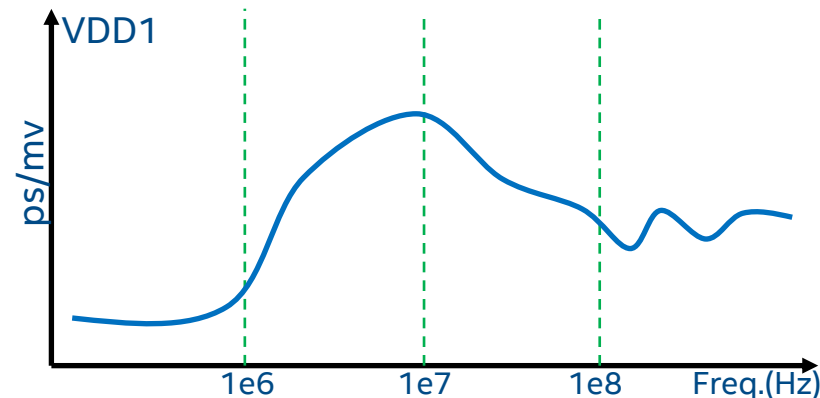
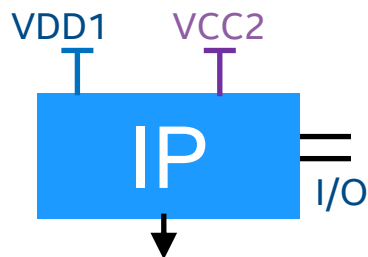
[End Voltage List]

[PSIJ Sensitivity] VDD1

frequency(Hz)	sensitivity (ps/mv)
100000	1.1
1000000	2.2
10000000	7.8
100000000	4.0
1000000000	3.9

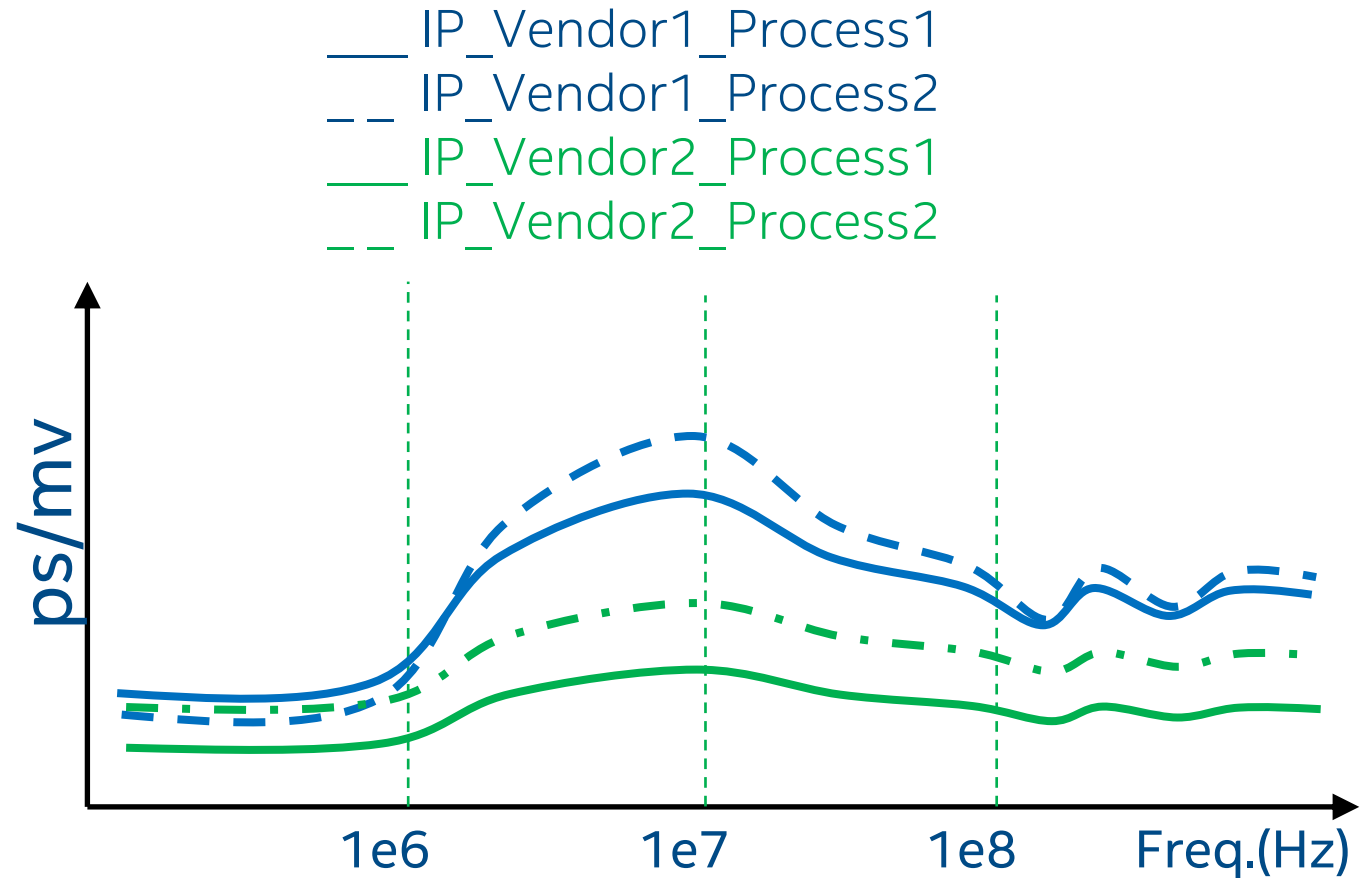
[PSIJ Sensitivity] VCC2

frequency(Hz)	sensitivity (ps/mv)
100000	2.7
1000000	3.0
10000000	4.9
100000000	4.1
1000000000	3.8



# Quick IP Selection, based upon [PSIJ Sensitivity]

- Same IP is better:
  - from vendor2 than
  - from vendor1
- Same IP is better:
  - upon process1 than
  - upon process2
- Same IP is the best
  - from vendor2 and
  - upon process1.



# Next Steps

- Submit IBIS BIRD to include [PSIJ Sensitivity] in IBIS.
- Call for EDA vendors to support [PSIJ Sensitivity] in IBIS
- Call for chip vendors to support [PSIJ Sensitivity] in IBIS
- Call for platform designers to support [PSIJ Sensitivity] in IBIS

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