BIRD223:  
Add Support for SPIM in IBIS  
- approved by IBIS Open Forum on July 14, 2023

SPIM = Streamlined Power Integrity Model

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Executive Summary

**Background:**
- OEM/ODMs desire to design Time-To-Market innovative products effectively
- Platform PI design without standard model significantly lags SI design with IBIS
- SPIM expedites platform PI design while protecting chip vendor’s IP

**Timeline:**
- PKG PI model was introduced upon FastPI PI architecture in 2018
- SPIM upon FastPI architecture got support with 3 EDA vendors in 2021
- SPIM draft initial version was brought up in IBIS ATM Group in 2022
- BIRD223, Add support for SPIM in IBIS, was submitted in March 2023
- BIRD223 got approved in IBIS Open Forum on July 14, 2023

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Platform PI Design: SPIM- Streamlined PI Model

Well taken care of in PKG & Silicon PDN design, by chip vendors, through SPIM, and CVRM auto-calculation built in FastPI.

**SPIM:**
- S parameter
- Rnetwork (DC)
- Weighted source
- Defined target
- Pin awareness

**Platform Level PI Design**

IEEE Paper: *Scalable Platform Power Integrity Design Approach with Standard PI Model (SPIM) and Unified PI Target (UPIT)*


Xingjian Kinger Cai; Yun Ling; Steven Yun Ji; Jimmy Hsiao; Chi-te Chen; Denis Chen, page 64-66, 14-18 May 2018

**• SPIM:** Streamlined PI Model, for each power rail in a SoC/PKG, or a module.
Platform PI Design: Stimulus & Target Definition

\[ [S_{pdn}] \rightarrow [Z_{pdn}] \]

\[ [V] = [Z_{pdn}][I] \]

\[ [V] = [v_1, v_2, \ldots, v_N, v_{S1}, v_{S2}, \ldots, v_{SM}]^T \]

\[ [I] = [w_1, w_2, \ldots, w_N, 0, 0, \ldots, 0]^T \]

\[ \sum_{i=1}^{i=N} w_i = 1 \]

\[ Z_{s_i} = v_s = \sum_{i=1}^{i=N+M} (Z_{pdn}(N + j), i * W_i), \quad j \in \{1: M\} \]

\[ Z_{s_i} = \sum_{i=1}^{i=N} (Z_{pdn}(N + j), i * W_i), \quad j \in \{1: M\} \]

**IEEE paper: VRM Modeling for Platform FastPI upon SPIM**

2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium

Xingjian Kinger Cai; Wei Qian; Chi-te Chen; etc., page 162, August 2021

Impedance target is generally defined at the observing Port_ j.
Tree Structure of .spim FILE

```
.spim FILE
-------------
|-- File Header Section
|  -------------
|  |-- [IBIS Ver]
|  |-- [Comment Char]
|  |-- [File Name]
|  |-- [File Rev]
|  |-- [Date]
|  |-- [Source]
|  |-- [Notes]
|  |-- [Disclaimer]
|  |-- [Copyright]
|-- [Device_SPIM]
|  -------------
|  |-- [Manufacturer]
|  |-- [Description]
|-- [SPIM Rail]
|  -------------
|  |-- [SPIM Pin Cluster]
|  |  -------------
|  |  |-- [End SPIM Pin Cluster]
|  |  |  |-- [End SPIM Rail]
|  |  |-- [SPIM Port List]
|  |  |  |-- [End SPIM Port List]
|  |  |  |  |-- [End Device SPIM]
|  |  |  |  |  |-- [End]
|-- [SPIM Touchstone File]
|  -------------
|  |-- [SPIM Stimulus]
|  |  -------------
|  |  |-- [End SPIM Stimulus]
|  |  |-- [SPIM Target]
|  |  |  -------------
|  |  |  |-- [End SPIM Target]
|  |  |-- [SPIM Observation Port]
|  |  |  |-- [End SPIM Observation Port]
|  |  |-- [SPIM Touchstone File]
|  |  |  |-- [End SPIM Touchstone File]
|-- [SPIM Rnetwork File]
|  -------------
|  |-- [SPIM Current]
|  |  -------------
|  |  |-- [End SPIM Current]
|  |  |-- [SPIM Voltage List]
|  |  |  -------------
|  |  |  |-- [End SPIM Voltage List]
|  |  |-- [SPIM Rnetwork File]
|  |  |  |-- [End SPIM Rnetwork File]
|-- [SPIM Stimulus]
|  -------------
|  |-- [End SPIM Stimulus]
|-- [SPIM Target]
|  -------------
|  |-- [End SPIM Target]
|-- [SPIM Observation Port]
|  -------------
|  |-- [End SPIM Observation Port]
|-- [SPIM Touchstone File]
|  -------------
|  |-- [End SPIM Touchstone File]
|-- [SPIM Rnetwork File]
|  -------------
|  |-- [SPIM Current]
|  |  -------------
|  |  |-- [End SPIM Current]
|  |  |-- [SPIM Voltage List]
|  |  |  -------------
|  |  |  |-- [End SPIM Voltage List]
|  |  |-- [SPIM Rnetwork File]
|  |  |  |-- [End SPIM Rnetwork File]
|  |  |  |  |-- [End]
```

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Linkage of .spim FILE to .ibs FILE

.ibs FILE

--------------
|-- File Header Section
|   ---------------------
|   |-- [IBIS Ver]
|   |-- [Comment Char]
|   |-- [File Name]
|   |-- [File Rev]
|   |-- [Date]
|   |-- [Source]
|   |-- [Notes]
|   |-- [Disclaimer]
|   |-- [Copyright]
|   ...
|   ...
|-- [Component]
|   ...
|   ...
|   |-- [Device SPIM Group]
|   |   |-- [End Device SPIM Group]
|   ...
|   ...

Example:

[Device SPIM Group] Group_name_1
Device_SPIM_name_1 NA
Device_SPIM_name_2 NA

| selector under [Component]
| if it is in the .ibs file
| if it is in the .ibs file

| ... Device_SPIM_name_3 spim_folder/file_name_1.spim
| ... RELATIVE to the .ibs file
| ... Device_SPIM_name_4

| [Device SPIM Group] Group_name_2
Device_SPIM_name_4 NA
Device_SPIM_name_5 NA

| selector under [Component]
| if it is in the .ibs file
| if it is in the .ibs file

| ... Device_SPIM_name_5 spim_folder/file_name_2.spim
| ... RELATIVE to the .ibs file
| ... Device_SPIM_name_6

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**Example .spim FILE - Supports PI AC Analysis**

**[SPIM Touchstone File]**

<table>
<thead>
<tr>
<th>file_type file_reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>File_TS &lt;path&gt;Intel_CPU2_VCC3_PKG.s20p</td>
</tr>
</tbody>
</table>

**[End SPIM Touchstone File]**

*** Here below explains how to use *.snp s-element model in IBIS-ISS.

```plaintext
.model pkg_model S N=20 tstonefile
  ='Intel_CPU2_VCC3_PKG.s20p'
  S_one_ref
+ OB_Stimulus_1
+ OB_Stimulus_2
+ OB_Stimulus_3
+ OB_Stimulus_4
+ OB_Stimulus_5
+ OB_Stimulus_6
+ OB_Stimulus_7
+ OB_Stimulus_8
+ OB_Sense
  + BGA_1
  + BGA_2
  + BGA_3
  + BGA_4
  + BGA_5
  + BGA_6
  + BGA_7
  + BGA_8
  + BGA_9
  + BGA_10
  + BGA_11
  + 0
  + mname=pkg_model
```

**[SPIM Stimulus]**

<table>
<thead>
<tr>
<th>OB_Stimulus</th>
<th>Weighting</th>
</tr>
</thead>
<tbody>
<tr>
<td>OB_Stimulus_1</td>
<td>0.20</td>
</tr>
<tr>
<td>OB_Stimulus_2</td>
<td>0.10</td>
</tr>
<tr>
<td>OB_Stimulus_3</td>
<td>0.05</td>
</tr>
<tr>
<td>OB_Stimulus_4</td>
<td>0.05</td>
</tr>
<tr>
<td>OB_Stimulus_5</td>
<td>0.20</td>
</tr>
<tr>
<td>OB_Stimulus_6</td>
<td>0.05</td>
</tr>
<tr>
<td>OB_Stimulus_7</td>
<td>0.05</td>
</tr>
<tr>
<td>OB_Stimulus_8</td>
<td>0.30</td>
</tr>
</tbody>
</table>

**[End SPIM Stimulus]**

**[SPIM Target]**

<table>
<thead>
<tr>
<th>[SPIM Observation Port] OB_Sense</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z(Frequency)  Z(typ)  Z(min)  Z(max)</td>
</tr>
<tr>
<td>100000      0.0069 NA    NA</td>
</tr>
<tr>
<td>10000000    0.0069 NA    NA</td>
</tr>
<tr>
<td>65000000    0.0130 NA    NA</td>
</tr>
<tr>
<td>190000000   0.0285 NA    NA</td>
</tr>
<tr>
<td>400000000   0.0285 NA    NA</td>
</tr>
</tbody>
</table>

**[End SPIM Target]**
Example .spim FILE - Supports Power DC Analysis

[Rnetwork File]
| file_type file_reference
| File_IBIS_ISS <path>My_CPU2_VCC3_PKG_Rnetwork.ckt
| ...
[End SPIM Rnetwork File]

[SPIM Current]
| I(name) I(typ) I(min) I(max)
| VCC 4.50 NA 7.50
[End SPIM Current]

[SPIM Voltage List]
| V(name) V(typ) V(min) V(max)
| VCC 1.000 0.900 1.100
[End SPIM Voltage List]

[End SPIM Rail]

[End Chip SPIM]

To Achieve:
- Most accurate per-pin current distribution
- Most accurate per-pin voltage droop map
- Most accurate Board level full PD analysis
FastPI (Platform PI Architecture with SPIM) Roadmap

Customer Database (customer)

SPI Models (Chip vendors)

C/L/D/R/S models (customer/vendors)

VR model (Auto-cal./Vendor)

SPIM works standalone, and/or also together with all IBIS Power models of Capacitor/Inductor/Diode/Resistor

FastPI (Platform PI design Framework)
Calling for major EDA vendors.

IEEE Paper: **Scalable Platform Power Integrity Design Approach with Standard PI Model (SPIM) and Unified PI Target (UPIT)**

AC analysis (Review & Sign-off) Version-1

Capacitor optimization for cost-optimal PDN

DC analysis (Review & Sign-off) Version-2

Transient analysis (Validation/VRTT) Version-3

User Friendly
EDA Ecosystem
Well established!
Next Steps:

- Example .spim file for golden example available in Q3’2023
- Cookbook Rev1.0 for SPIM Ver1.0 available in Q4’2023
- BIRD223 integration into a future release of the IBIS Specification
- SPIM parser available in a future release of IBISCHK
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