IBIS Chair's Report

Lance Wang

Zuken USA

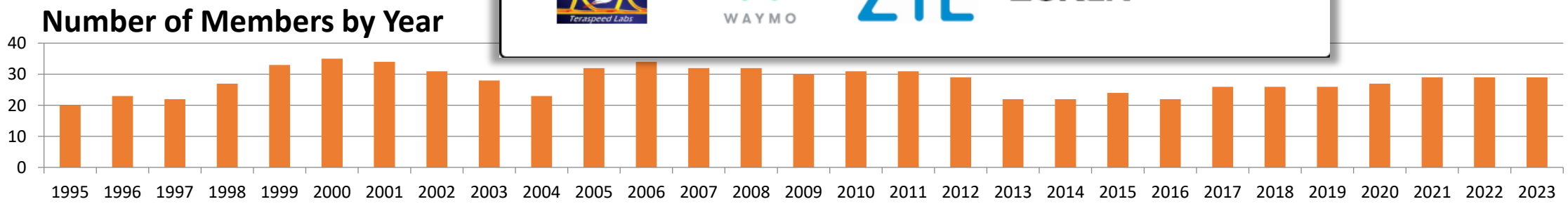
Chair, IBIS Open Forum

Hybrid IBIS Summit with IEEE EMC+SIPI 2023

Grand Rapids, MI, USA

August 4, 2023

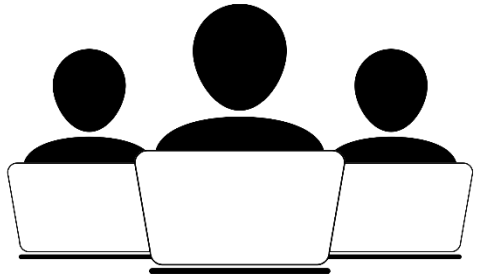
29 IBIS Members (Organization-based)



IBIS Officers June 2023- May 2024

Elected

Chair:	*Lance Wang, Zuken USA*
Vice-Chair:	*Randy Wolff, Siemens EDA*
Secretary:	*Graham Kus, MathWorks*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Zhiping Yang, MST*
Postmaster:	*Curtis Clark, ANSYS*
Webmaster:	*Steve Parker, Marvell*

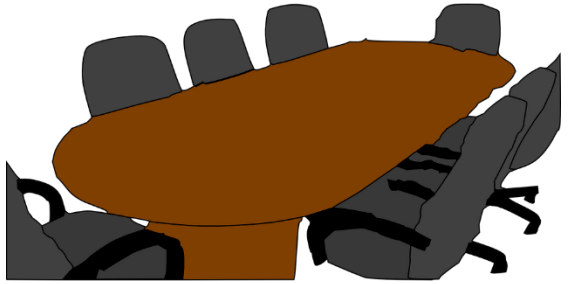


Appointed

- University Relations: *Chulsoon Hwang, MST*
- IEEE DASC IBIS Liaison: *Michael Mirmak, Intel*

IBIS Meetings

- Weekly teleconferences
  - Quality task group (Tuesdays, 09:00 PT)
  - Advanced Technology Modeling (ATM) task group (Tuesdays, 12:00 PT)
  - Interconnect task group (Wednesdays, 08:00 PT)
  - Editorial task group (suspended)
- IBIS Open Forum teleconference every 3 weeks (Fridays, 08:00 PT)
- IBIS Summit meetings (USA and international)
  - DesignCon, IEEE SPI, IEEE EMC+SIPI, Shanghai, Tokyo (JEITA-organized)
- Participants: ~280 in 2022



SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, and Michael McNair
- SAE ITC provides financial, legal, and other services
- https://www.sae-itc.com/

SAE ITC®
An SAE International Affiliate

Task Groups

- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi, Siemens EDA
  - https://ibis.org/atm_wip/
  - Develop non-interconnect technical BIRDs
- Editorial Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/editorial_wip/
  - Produce IBIS specification documents
- Interconnect Task Group
  - Chair: Michael Mirmak, Intel
  - https://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Quality Task Group
  - Chair: Bob Ross, Teraspeed Labs
  - https://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development

BIRD = Buffer Issue Resolution Document

IBIS Milestones

I/O Buffer Information Specification

- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power-aware model

Celebrating 30 Years in 2023!

I/O Buffer Information Specification

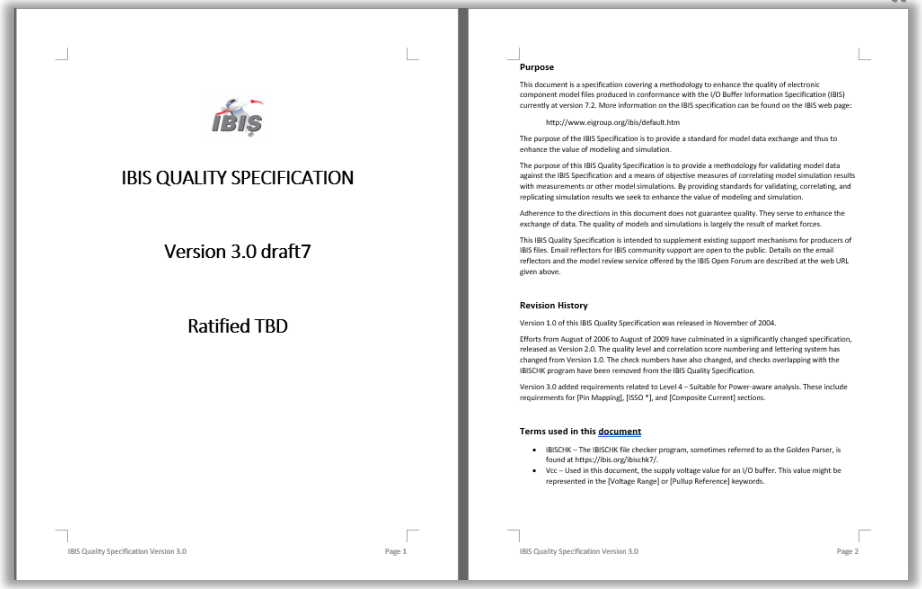
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- 2019 **IBIS 7.0**:
  - Back-channel time-domain support
  - Interconnect modeling using IBIS-ISS and Touchstone
- 2021 **IBIS 7.1:**
  - DDRx IBIS-AMI support
  - Electrical Module Description (EMD)
  - IBIS-AMI back-channel statistical optimization
- 2023 **IBIS 7.2:**
  - Redriver simulation flow fixes
  - PAMn IBIS-AMI support

Other Work

- 1995: **ANSI/EIA-656 (IBIS 2.1 International standard)**
- 1999: **ANSI/EIA-656-A (IBIS 3.2 International standard)**
- 2001: **IEC 62014-1 (IBIS 3.2 International standard)**
- 2003: **Interconnect Model Specification (ICM 1.0)**
- 2006: **ANSI/EIA-656-B (IBIS 4.2 International standard)**
- 2009: **Touchstone 2.0**
  - Official Touchstone donated from Agilent/Keysight
- 2011: **IBIS-ISS 1.0 (Interconnect SPICE Subcircuit)**
  - Subset of HSPICE
- **IBISCHK**: IBIS file syntax parser
  - Current version 7.2.0
  - Source code available for purchase
  - Compiled executables available free of charge
- **TSCHK2**: Touchstone 2.0 file syntax parser
  - Current version 2.0.1
  - Source code available for purchase
  - Compiled executables available free of charge

IBIS Quality Specification

- Quality specification updated to version 3.0 with additions for power-aware models
  - 5 new items for [Component] and [Pin Mapping]
  - 12 new items for [Model]
  - The specification document is in the process for approval by the IBIS Open Forum



IBIS QUALITY SPECIFICATION

Version 3.0 draft7

Ratified TBD

Purpose

This document is a specification covering a methodology to enhance the quality of electronic component model files produced in conformance with the I/O Buffer Information Specification (IBIS) currently at version 7.2. More information on the IBIS specification can be found on the IBIS web page:

http://www.eigroup.org/ibis/default.htm

The purpose of the IBIS Specification is to provide a standard for model data exchange and thus to enhance the value of modeling and simulation.

The purpose of this IBIS Quality Specification is to provide a methodology for validating model data against the IBIS Specification and a means of objective measures of correlating model simulation results with measurements or other model simulations. By providing standards for validating, correlating, and replicating simulation results we seek to enhance the value of modeling and simulation.

Adherence to the directions in this document does not guarantee quality. They serve to enhance the exchange of data. The quality of models and simulations is largely the result of market forces.

This IBIS Quality Specification is intended to supplement existing support mechanisms for producers of IBIS files. Email reflectors for IBIS community support are open to the public. Details on the email reflectors and the model review service offered by the IBIS Open Forum are described at the web URL given above.

Revision History

Version 1.0 of this IBIS Quality Specification was released in November of 2004.

Efforts from August of 2006 to August of 2009 have culminated in a significantly changed specification, released as Version 2.0. The quality level and correlation score numbering and lettering system has changed from Version 1.0. The check numbers have also changed, and checks overlapping with the IBISCHK program have been removed from the IBIS Quality Specification.

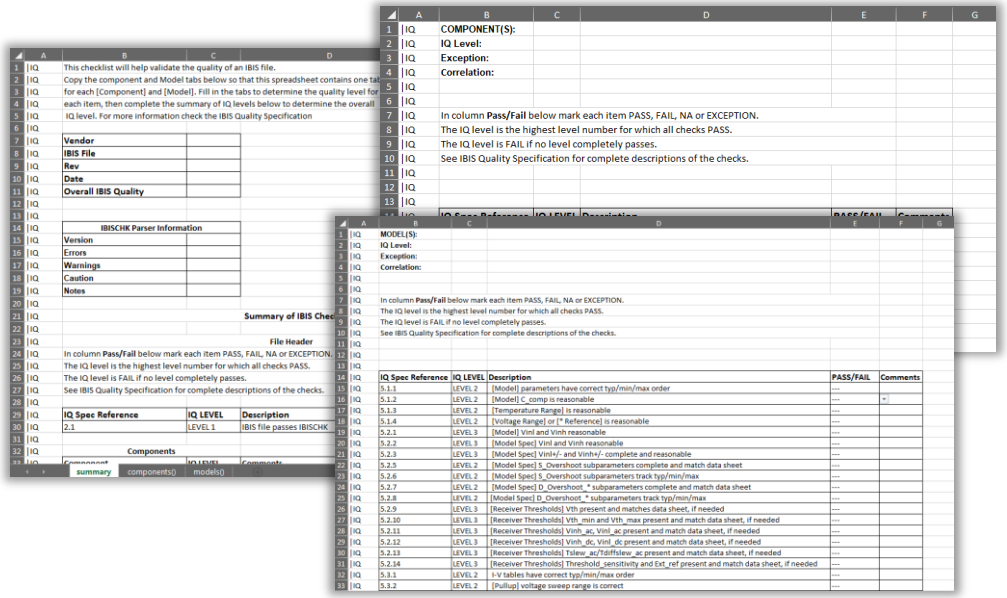
Version 3.0 added requirements related to Level 4 – Suitable for Power-aware analysis. These include requirements for [Pin Mapping], [ISSO *], and [Composite Current] sections.

Terms used in this document

- IBISCHK – The IBISCHK file checker program, sometimes referred to as the Golden Parser, is found at https://ibis.org/ibischk7/.
- Vcc – Used in this document, the supply voltage value for an I/O buffer. This value might be represented in the [Voltage Range] or [Pullup Reference] keywords.

IBIS Quality Specification Version 3.0 Page 1

IBIS Quality Specification Version 3.0 Page 2



1	IQ	COMPONENT(S):				
2	IQ	IQ Level:				
3	IQ	Exception:				
4	IQ	Correlation:				
5	IQ					
6	IQ					
7	IQ	In column **Pass/Fail** below mark each item PASS, FAIL, NA or EXCEPTION.				
8	IQ	The IQ level is the highest level number for which all checks PASS.				
9	IQ	The IQ level is FAIL if no level completely passes.				
10	IQ	See IBIS Quality Specification for complete descriptions of the checks.				
11	IQ					
12	IQ					
13	IQ					

IQ Spec Reference	IQ LEVEL	Description	PASS/FAIL	Comments
5.1.1	LEVEL 2	[Model] parameters have correct typ/min/max order	---	
5.1.2	LEVEL 2	[Model] C_comp is reasonable	---	
5.1.3	LEVEL 2	[Temperature Range] is reasonable	---	
5.1.4	LEVEL 2	[Voltage Range] or [* Reference] is reasonable	---	
5.2.1	LEVEL 3	[Model] Vinl and Vinh reasonable	---	
5.2.2	LEVEL 3	[Model Spec] Vinl and Vinh reasonable	---	
5.2.3	LEVEL 3	[Model Spec] Vinl+/- and Vinh+/- complete and reasonable	---	
5.2.5	LEVEL 2	[Model Spec] S_Overshoot subparameters complete and match data sheet	---	
5.2.6	LEVEL 2	[Model Spec] S_Overshoot subparameters track typ/min/max	---	
5.2.7	LEVEL 2	[Model Spec] D_Overshoot_* subparameters complete and match data sheet	---	
5.2.8	LEVEL 2	[Model Spec] D_Overshoot_* subparameters track typ/min/max	---	
5.2.9	LEVEL 3	[Receiver Thresholds] Vth present and matches data sheet, if needed	---	
5.2.10	LEVEL 3	[Receiver Thresholds] Vth_min and Vth_max present and match data sheet, if needed	---	
5.2.11	LEVEL 3	[Receiver Thresholds] Vinh_ac, Vinl_ac present and match data sheet, if needed	---	
5.2.12	LEVEL 3	[Receiver Thresholds] Vinh_dc, Vinl_dc present and match data sheet, if needed	---	
5.2.13	LEVEL 3	[Receiver Thresholds] Tslew_ac/Tdiffslew_ac present and match data sheet, if needed	---	
5.2.14	LEVEL 3	[Receiver Thresholds] Threshold_sensitivity and Ext_ref present and match data sheet, if needed	---	
5.3.1	LEVEL 2	I-V tables have correct typ/min/max order	---	
5.3.2	LEVEL 2	[Pullup] voltage sweep range is correct	---	

- Quality checklist spreadsheet
  - The checklist spreadsheet is in sync with the specification document
  - The spreadsheet includes some automation to determine IQ level on each component and model sheet
  - The spreadsheet file will be available on the website along with the new version of the specification

What's Next for IBIS?

- IBIS Open Forum's task groups are discussing these topics:
  - Expanded system-level perspective
    - Clock/data relationships, timing information, equalization training
  - Power Integrity focused modeling
    - Chip-level Standard Power Integrity Model (SPIM, BIRD223 accepted on July 14, 2023)
    - Improved Power Supply Induced Jitter (PSIJ) modeling (BIRD220 and others)
    - Voltage regulator, diode, and inductor models
  - Multi-level analog buffer modeling
  - Interconnect Modeling
    - Touchstone 3.0 with Pole/Residue and port mapping support
    - Touchstone 2.1 expansions
    - IBIS-ISS expansions
  - What else should we be looking at? Bring your ideas!

Participation in IBIS

- The success of IBIS depends on active participation and volunteering
- Bringing your ideas and talents to IBIS
  - Task groups for technical discussions and document editing
  - IBIS email reflectors
  - Open Forum teleconferences for event planning and voting
  - Summit presentations
  - IBIS Board and task group volunteering
  - Writing BIRDs – Buffer Issue Resolution Documents
    - Official method for submitting a proposed change to the IBIS specification
    - Many developed collaboratively in task groups
    - Discussed and voted on in Open Forum meetings

IBIS Website Resources

IBIS Summits

Task Group Info

Member FAQ

Spec documents

*IRDs

Email support

Syntax Parser Downloads

[Thank You]

IBIS Open Forum:
Web: https://ibis.org
Email: info@ibis.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.