IBIS Chair’s Report

Lance Wang
Zuken USA
Chair, IBIS Open Forum

Hybrid IBIS Summit with IEEE EMC+SIPI 2023
Grand Rapids, MI, USA
August 4, 2023
29 IBIS Members (Organization-based)
Chair: Lance Wang, Zuken USA
Vice-Chair: Randy Wolff, Siemens EDA
Secretary: Graham Kus, MathWorks
Treasurer: Bob Ross, Teraspeed Labs
Librarian: Zhiping Yang, MST
Postmaster: Curtis Clark, ANSYS
Webmaster: Steve Parker, Marvell

• University Relations: Chulsoon Hwang, MST
• IEEE DASC IBIS Liaison: Michael Mirmak, Intel
IBIS Meetings

• Weekly teleconferences
  • Quality task group (Tuesdays, 09:00 PT)
  • Advanced Technology Modeling (ATM) task group (Tuesdays, 12:00 PT)
  • Interconnect task group (Wednesdays, 08:00 PT)
  • Editorial task group (suspended)

• IBIS Open Forum teleconference every 3 weeks (Fridays, 08:00 PT)

• IBIS Summit meetings (USA and international)
  • DesignCon, IEEE SPI, IEEE EMC+SIPI, Shanghai, Tokyo (JEITA-organized)

• Participants: ~280 in 2022
SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, and Michael McNair
- SAE ITC provides financial, legal, and other services
- [https://www.sae-itc.com/](https://www.sae-itc.com/)
Task Groups

• Advanced Technology Modeling Task Group
  • Chair: Arpad Muranyi, Siemens EDA
  • https://ibis.org/atm_wip/
  • Develop non-interconnect technical BIRDs

• Editorial Task Group
  • Chair: Michael Mirmak, Intel
  • https://ibis.org/editorial_wip/
  • Produce IBIS specification documents

• Interconnect Task Group
  • Chair: Michael Mirmak, Intel
  • https://ibis.org/interconn_wip/
  • Develop on-die/package/module/connector interconnect modeling BIRDs

• Quality Task Group
  • Chair: Bob Ross, Teraspeed Labs
  • https://ibis.org/quality_wip/
  • Oversee IBISCHK parser testing and development

BIRD = Buffer Issue Resolution Document
I/O Buffer Information Specification

- **1993-1994 IBIS 1.0-2.1:**
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- **1997-1999 IBIS 3.0-3.2:**
  - Package models
  - Electrical Board Description (EBD)
- **2002-2006 IBIS 4.0-4.2:**
  - Receiver models
  - AMS languages
- **2007-2012 IBIS 5.0-5.1:**
  - IBIS-AMI SerDes models
  - Power-aware model

### IBIS Milestones

- **2013-2015 IBIS 6.0-6.1:**
  - PAM4 multi-level signaling
  - Power delivery package models
- **2019 IBIS 7.0:**
  - Back-channel time-domain support
  - Interconnect modeling using IBIS-ISS and Touchstone
- **2021 IBIS 7.1:**
  - DDRx IBIS-AMI support
  - Electrical Module Description (EMD)
  - IBIS-AMI back-channel statistical optimization
- **2023 IBIS 7.2:**
  - Redriver simulation flow fixes
  - PAMn IBIS-AMI support

Celebrating 30 Years in 2023!

### Other Work

- **1995:** ANSI/EIA-656 (IBIS 2.1 International standard)
- **1999:** ANSI/EIA-656-A (IBIS 3.2 International standard)
- **2001:** IEC 62014-1 (IBIS 3.2 International standard)
- **2003:** Interconnect Model Specification (ICM 1.0)
- **2006:** ANSI/EIA-656-B (IBIS 4.2 International standard)
- **2009:** Touchstone 2.0
  - Official Touchstone donated from Agilent/Keysight
- **2011:** IBIS-ISS 1.0 (Interconnect SPICE Subcircuit)
  - Subset of HSPICE
- **IBISCHK:** IBIS file syntax parser
  - Current version 7.2.0
  - Source code available for purchase
  - Compiled executables available free of charge
- **TSCHK2:** Touchstone 2.0 file syntax parser
  - Current version 2.0.1
  - Source code available for purchase
  - Compiled executables available free of charge
IBIS Quality Specification

• Quality specification updated to version 3.0 with additions for power-aware models
  • 5 new items for [Component] and [Pin Mapping]
  • 12 new items for [Model]
  • The specification document is in the process for approval by the IBIS Open Forum

• Quality checklist spreadsheet
  • The checklist spreadsheet is in sync with the specification document
  • The spreadsheet includes some automation to determine IQ level on each component and model sheet
  • The spreadsheet file will be available on the website along with the new version of the specification
What’s Next for IBIS?

• IBIS Open Forum’s task groups are discussing these topics:
  • Expanded system-level perspective
    • Clock/data relationships, timing information, equalization training
  • Power Integrity focused modeling
    • Chip-level Standard Power Integrity Model (SPIM, BIRD223 accepted on July 14, 2023)
    • Improved Power Supply Induced Jitter (PSIJ) modeling (BIRD220 and others)
    • Voltage regulator, diode, and inductor models
  • Multi-level analog buffer modeling
  • Interconnect Modeling
    • Touchstone 3.0 with Pole/Residue and port mapping support
    • Touchstone 2.1 expansions
    • IBIS-ISS expansions
  • What else should we be looking at? Bring your ideas!
Participation in IBIS

• The success of IBIS depends on active participation and volunteering

• Bringing your ideas and talents to IBIS
  • Task groups for technical discussions and document editing
  • IBIS email reflectors
  • Open Forum teleconferences for event planning and voting
  • Summit presentations
  • IBIS Board and task group volunteering

• Writing BIRDs – Buffer Issue Resolution Documents
  • Official method for submitting a proposed change to the IBIS specification
  • Many developed collaboratively in task groups
  • Discussed and voted on in Open Forum meetings
[Thank You]

IBIS Open Forum:
Web: https://ibis.org
Email: info@ibis.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.