Updates on BIRD220

– Improved Power Supply Induced Jitter Model for IBIS simulation

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Outline

- Introduction
  - Motivation
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  - Feedbacks from IBIS ATM Group
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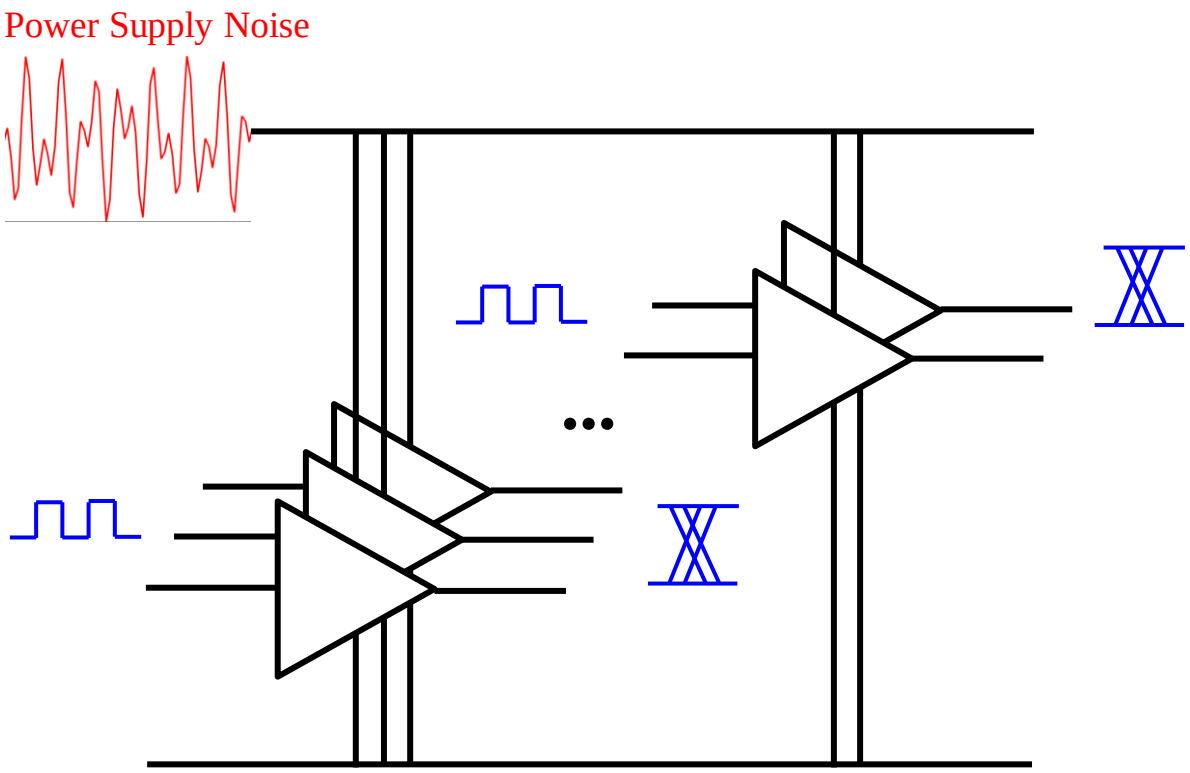
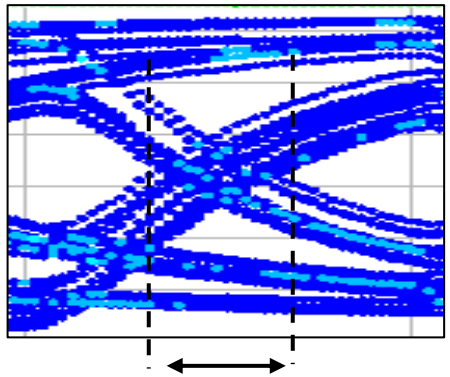
  - Jitter Sensitivity-Based Direct K_u/K_d Modification
  - Non-linear PSIJ Effect
  - BIRD 220.1

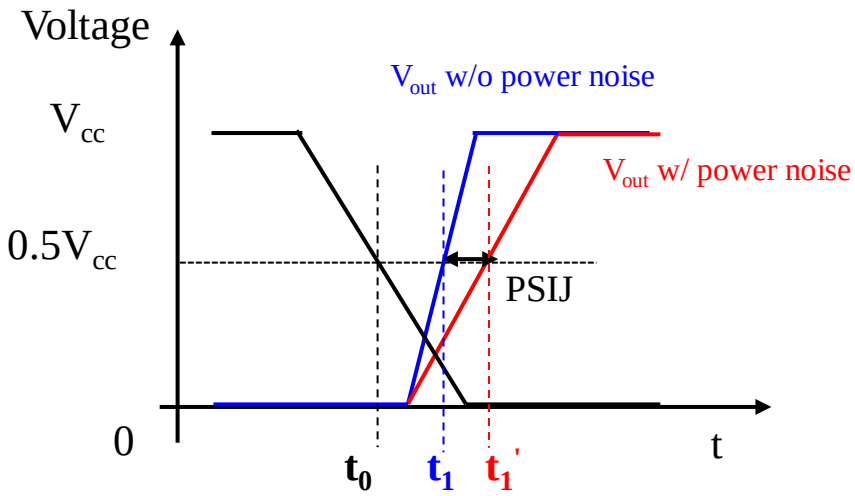
- Conclusions

Power Supply Induced Jitter (PSIJ)

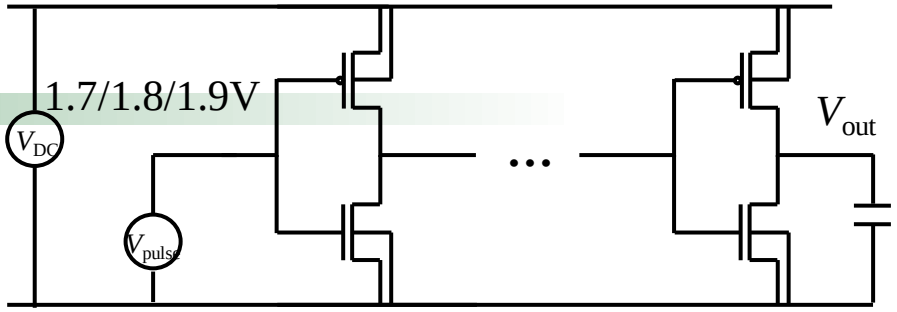
- PSIJ: The time variation in the output transition edges from ideal positions due to the **voltage fluctuations on power rail**.





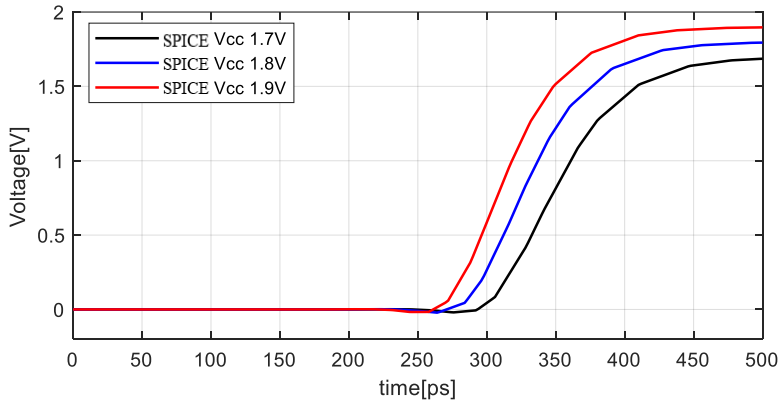


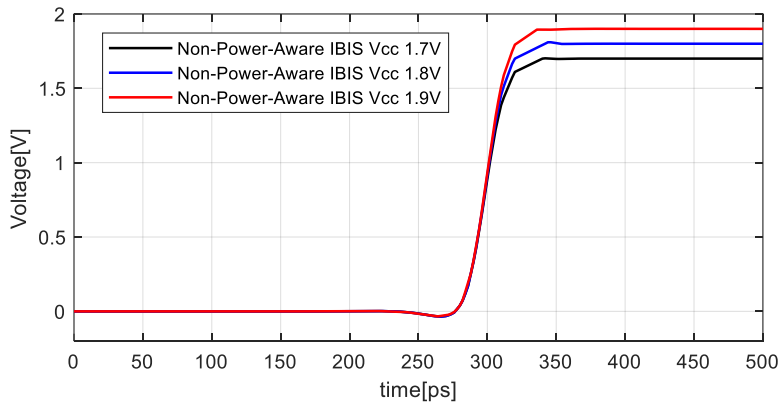
Motivation – Limitations of the IBIS Model

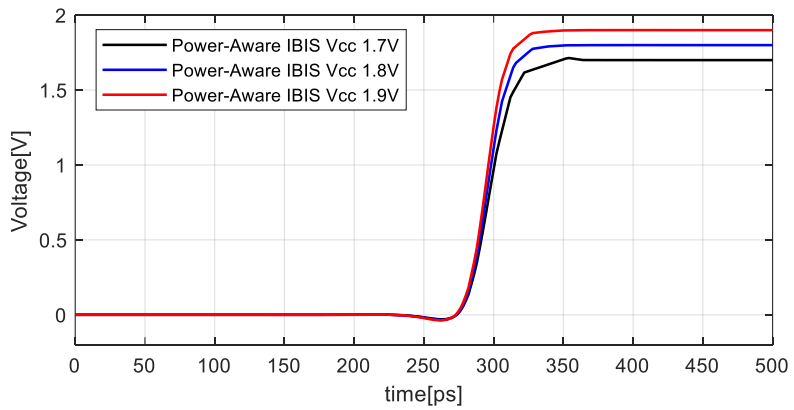


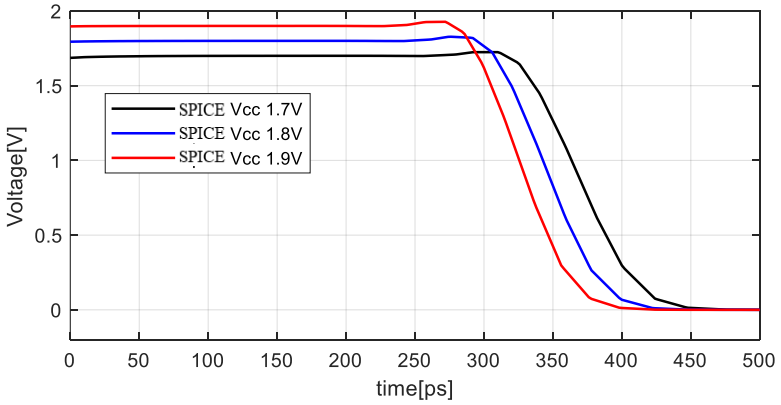
- **<u>Cannot</u>** account for the delay change caused by power noise correctly.

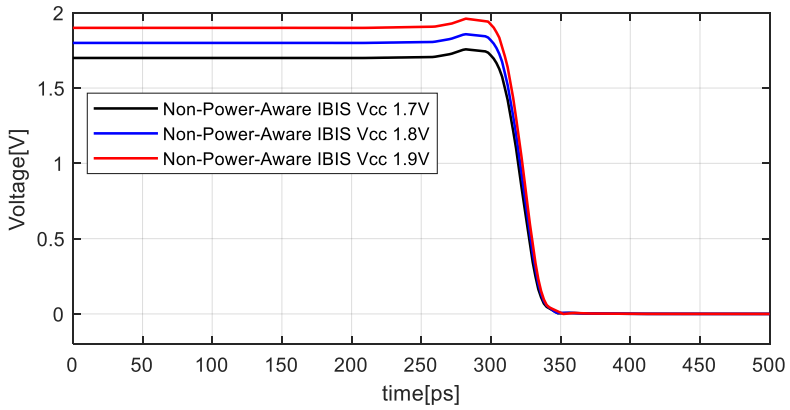
➢ Example: an inverter chain output, change power voltage to 1.7/1.8/1.9V, respectively

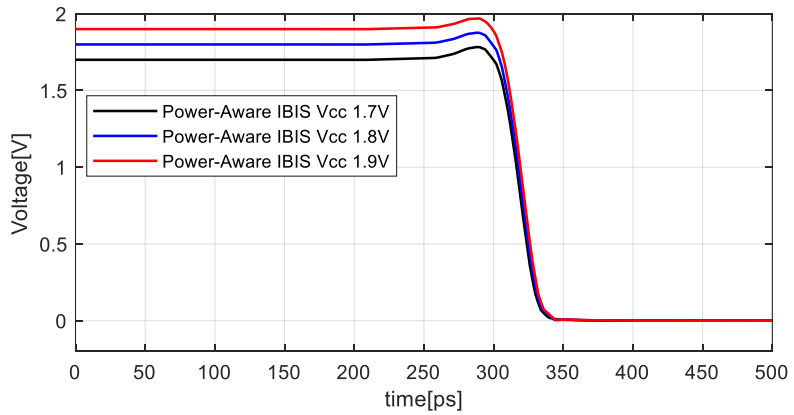








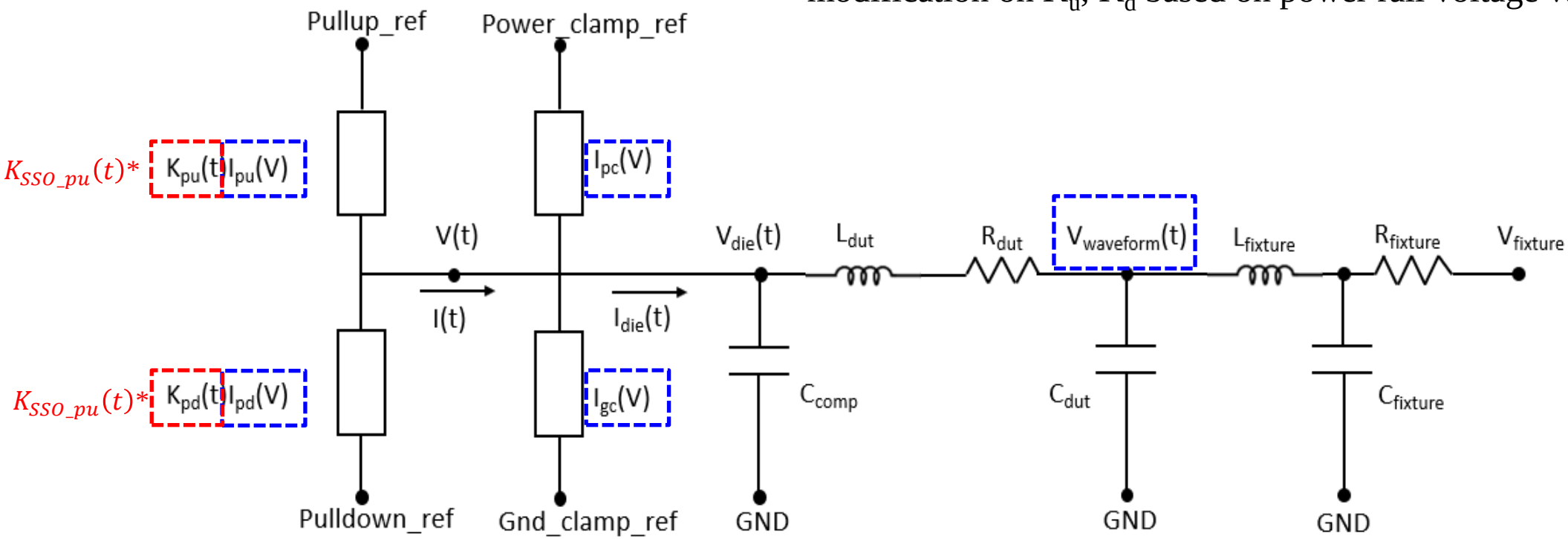




<SPICE> **<Non-Power-aware IBIS Model>** **<Power-aware IBIS Model>**

Output Buffer Structure in Power Aware IBIS

- Power-aware IBIS model considers **gate modulation effect**, ratio modification on K_u, K_d based on power rail voltage value.



$$K_{SSO\_pu}(t)K_{pu}(t)I_{pu}(V) + K_{SSO\_pu}(t)K_{pd}(t)I_{pd}(V) + I_{pc}(V) + I_{gc}(V) = I_{out}(V)$$

Power-Aware IBIS Model

- Power-aware IBIS model considers gate modulation effect, ratio modification on K_u, K_d based on power rail voltage value

Gate Modulation Coefficients

The ST "Gate Modulation" solution is based on the introduction of two coefficients, one for the Pullup and one for the Pulldown stage, which modulate properly the IBIS standard current (I_IBIS-STD) when a bouncing noise occurs on the power and ground nodes

$$I(Vgs, Vds) = Kssn(Vgs,Vds)*I(Vgs=VDD,Vds)$$

Effective SPICE current — IBIS standard current

I_effective = Kssn(Vgs,Vds)*I_IBIS-STD

$$K_d(t)I_{pd} -> K_{sspd}(V_{pd})K_d(t)I_{pd}$$

$$K_u(t)I_{pu} -> K_{sspu}(V_{pu})K_u(t)I_{pu}$$

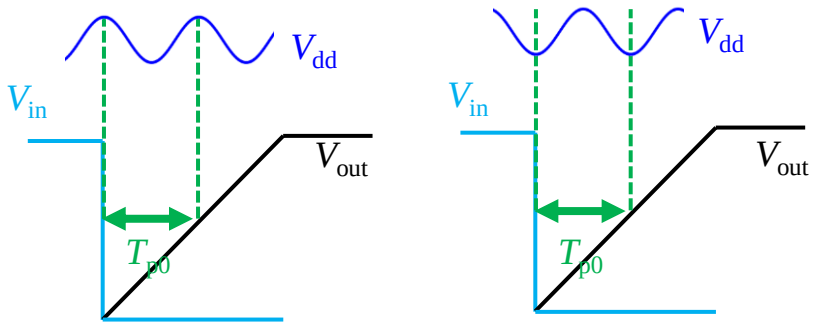
$$K_{sspd}(V_{pd}) = \frac{V_{pd}}{I_{sspd}(0)}$$

$$K_{sspu}(V_{pu}) = \frac{V_{pu}}{I_{sspu}(0)}$$

Two more tables introduced in the IBIS

Limitation: The modification of K_u, K_d does not consider the **time averaged effect**

- The ratio modification K_{sspd}, K_{sspu} on K_u, K_d is only a function of V_{pd} or V_{pu}, it cannot reflect the effect of the averaged power rail voltage noise on switching edge timing change.



"BIRD 98 and ST 'Gate Modulation' Convergence", IBIS Open Forum Teleconference, Jan. 26th, 2007. http://www.ibis.org/docs/BIRD98&ST_Proposal_Convergence.ppt

Behavioral modeling of jitter due to power supply noise for input/output buffers (US Patent 9842177B1)

BIRD 220 – Introduction

- Provide the pre-driver output rising and falling edge DC PSIJ sensitivity in s/V.
- The pre-driver should be in the same power domain as the buffer defined in the corresponding [Model].

Keyword:	**[Pre-driver PSIJ Sensitivity]**
Required:	No
Description:	Used to describe the pre-driver output rising and falling edge DC power supply-induced jitter (PSIJ) sensitivity related to the changes in voltage of the Pullup_ref terminal of a [Model].
Sub-Params:	Rising_edge, Falling_edge

Example:

```
[Pre-driver PSIJ Sensitivity]
|unit(s/V)          typ    min    max
Rising_edge         50p    52p    48p
Falling_edge        -40p   NA     NA
```

- Modify $K_u(t)$, $K_d(t)$ as a function of **time averaged** power rail voltage Vcc(t);
- Introduce correction coefficient B and A as a function of **time**.
- Use "**Pre-driver PSIJ Sensitivity**" in the process of extracting the B and A correction coefficients.

$$K_{pu}(t) = K_{pu0}(t) + B_{pu}(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A_{pu}(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2$$

$$K_{pd}(t) = K_{pd0}(t) + B_{pd}(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A_{pd}(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2$$

where the K_{pu0} and K_{pd0} are the Kpu and Kpd coefficients for typical power supply voltage V_{cc0} case, $B(t)$ and $A(t)$ are the linear and quadratic fitting coefficients, respectively, that account for the delay change due to the power rail noise voltage, and $\frac{\int_0^t V_{cc}(\tau)d\tau}{t}$ is the averaged power supply voltage since the last input switching event.

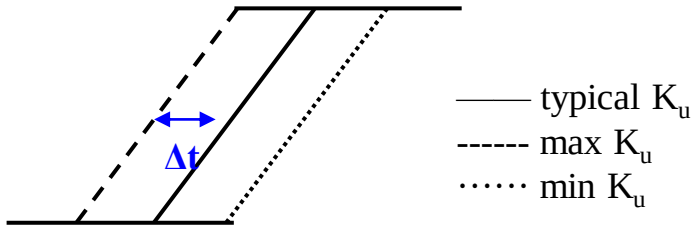
BIRD 220 – Modeling Process

Step 1: $K_u(t)$, $K_d(t)$ extraction for typ case

$$K_u(t)*I_u(V_1)+ K_d(t)*I_d(V_1)=I_{out}(V_1)$$

$$K_u(t)*I_u(V_2)+ K_d(t)*I_d(V_2)=I_{out}(V_2)$$

Step 2: $K_u(t)$, $K_d(t)$ extraction for max/min supply voltage case with DC jitter sensitivity



<K_u for output rising edge>

$$K_u/K_{d\_max/min}(t) = K_u/K_{d\_typ}\left(t \pm \frac{\text{DC Jitter sensitivity} \times \Delta V_{dd}}{\Delta t}\right)$$

Step 3: $B_u(t)$, $A_u(t)$ and $B_d(t)$, $A_d(t)$ extraction

$$K_{u\_max}(t) = K_{u0}(t) + B_u(t)(V_{cc\_max} - V_{cc0}) + A_u(t)(V_{cc\_max} - V_{cc0})^2$$

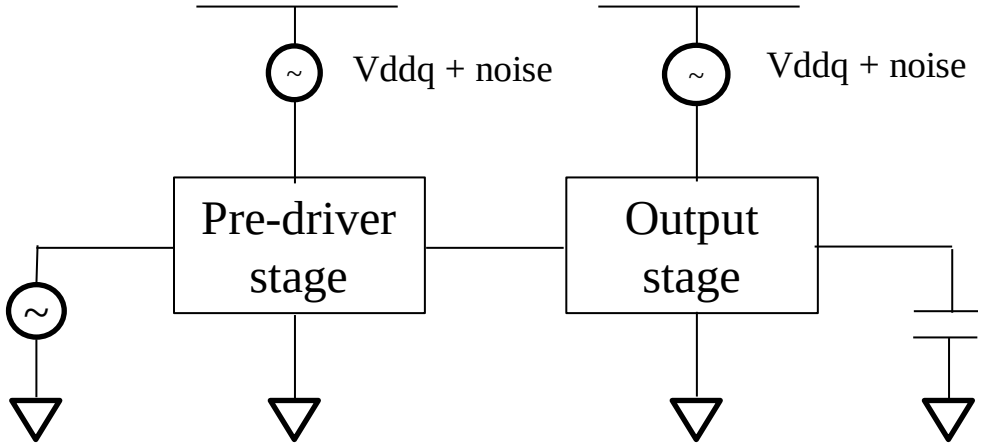
$$K_{u\_min}(t) = K_{u0}(t) + B_u(t)(V_{cc\_min} - V_{cc0}) + A_u(t)(V_{cc\_min} - V_{cc0})^2$$

Step 4: $K_u(t)$, $K_u(t)$ modification

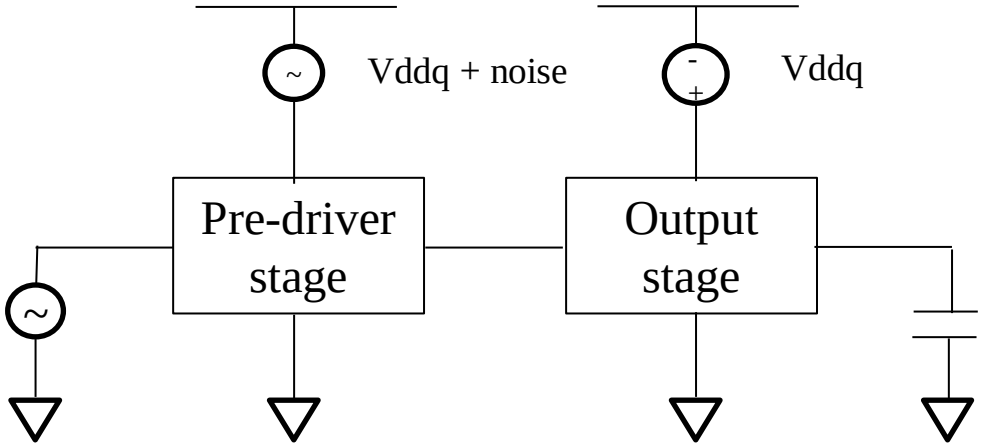
$$K_u(t) = K_{u0}(t) + B_{pu}(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A_{pu}(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2$$

$$K_d(t) = K_{d0}(t) + B_{pd}(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A_{pd}(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2$$

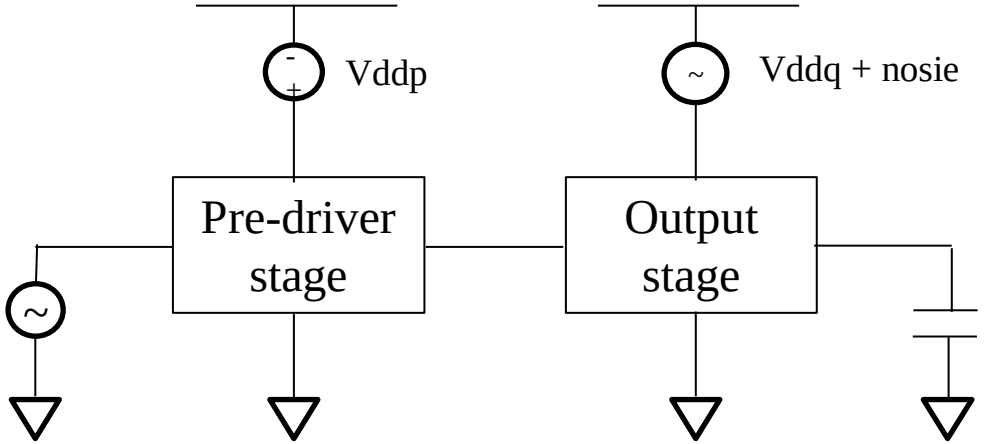
Why Only Pre-driver PSIJ Sensitivity – Simulation Setup for Pre-Driver PSIJ Effect



(a) Power noise for both pre-driver and output stage



(b) Power noise only for pre-driver stage



(c) Power noise only for output stage

PSIJ Sensitivity Comparison

Case (load = 1pF)	SPICE	Power Aware IBIS Model
Vcc noise only for the pre-driver stages (b)	141.5 ps/V	
Vcc noise only for the output stage (c)	43.15 ps/V	
Vcc noise for all the stages (a)	182 ps/V	35.5 ps/V

Case (load = 10pF)	SPICE	Power Aware IBIS Model
Vcc noise only for the pre-driver stages (b)	141.5 ps/V	
Vcc noise only for the output stage (c)	206.5 ps/V	
Vcc noise for all the stages (a)	347 ps/V	217 ps/V

Case (load = 2pF)	SPICE	Power Aware IBIS Model
Vcc noise only for the pre-driver stages (b)	143 ps/V	
Vcc noise only for the output stage (c)	59.5 ps/V	
Vcc noise for all the stages (a)	202.5ps/V	54 ps/V

- The driver output PSIJ Sensitivity caused by the pre-driver power noise is independent of the load condition of the final stage.
- The driver output PSIJ Sensitivity caused by the final-driver power noise is dependent of the load condition.
- The power aware IBIS model can model the final stage PSIJ.

Total PSIJ sensitivity = PSIJS caused by the **pre-driver** PWR noise + PSIJS caused by the **final driver** PWR noise

Validation – Inverter Chain Output Rising Edge

- 8 stage inverter chain with different load capacitance
- DC power noise 1.7V/1.8V/1.9V

	PSIJ Sensitivity (ps/V)					
	Load 1pF to V_{SS}		Load 2pF to V_{SS}		Load 10pF to V_{SS}	
SPICE	**-184.45**		**-207**		**-350**	
Non-Power-aware IBIS	-6.5		-9.5		-39.5	
Power-aware IBIS	-35.5		-54		-217	
Proposed Algorithm	**-187**		**-210.5**		**-355**	
	Δ (to SPICE)					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-Power-aware IBIS	177.95	96.48	197.5	95.41	310.9	88.71
Power-aware IBIS	148.95	80.75	153	73.91	133	38
Proposed Algorithm	**2.55**	**1.38**	**3.5**	**1.69**	**5**	**1.43**

- The improved IBIS model using the proposed algorithm reduces the discrepancy to within 2% for the three tested load conditions.

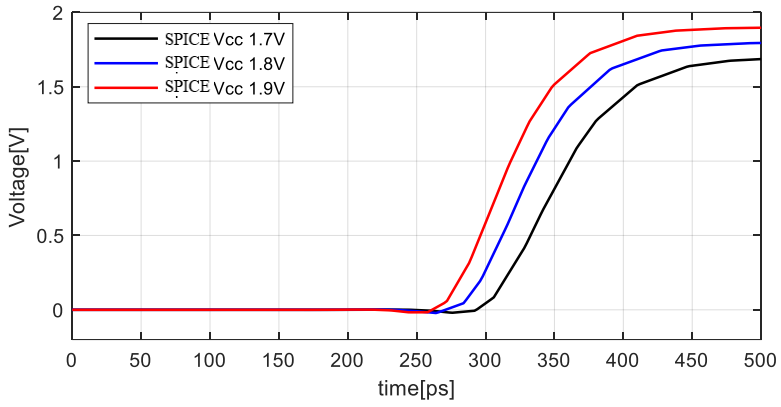
Validation – Inverter Chain Output Falling Edge

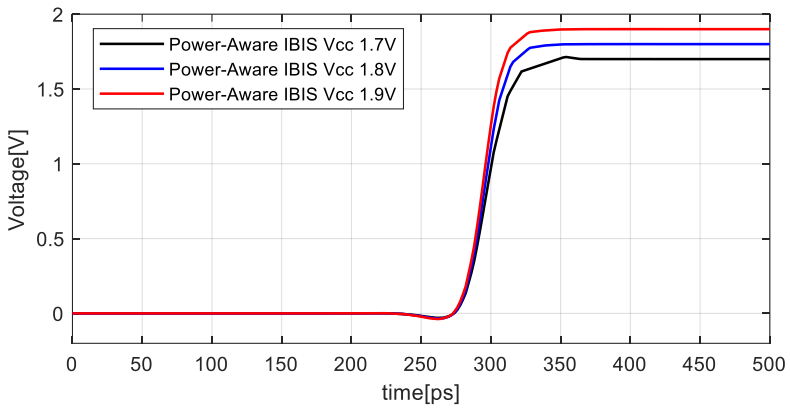
- 8 stage inverter chain with different load capacitance
- DC power noise 1.7V/1.8V/1.9V

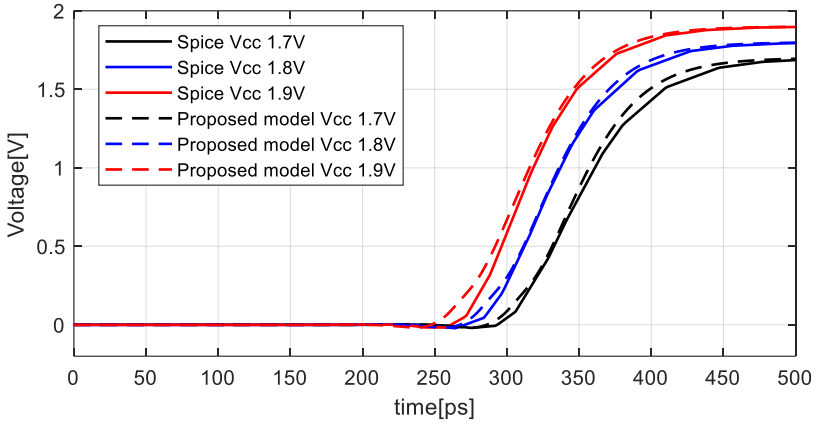
	PSIJ Sensitivity (ps/V)					
	Load 1pF to V_{SS}		Load 2pF to V_{SS}		Load 10pF to V_{SS}	
SPICE	**-193.91**		**-194.16**		**-188.71**	
Non-Power-aware IBIS	24.41		36.07		123.21	
Power-aware IBIS	25		35		135	
Proposed Model	**-188.95**		**-186.75**		**-175.85**	
	Δ (to SPICE)					
	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%	Absolute diff (ps/V)	%
Non-Power-aware IBIS	218.32	112.59	230.23	118.58	311.92	165.29
Power-aware IBIS	218.91	112.89	229.16	118.03	323.71	171.53
Proposed Model	**4.96**	**2.56**	**7.41**	**3.82**	**12.86**	**6.81**

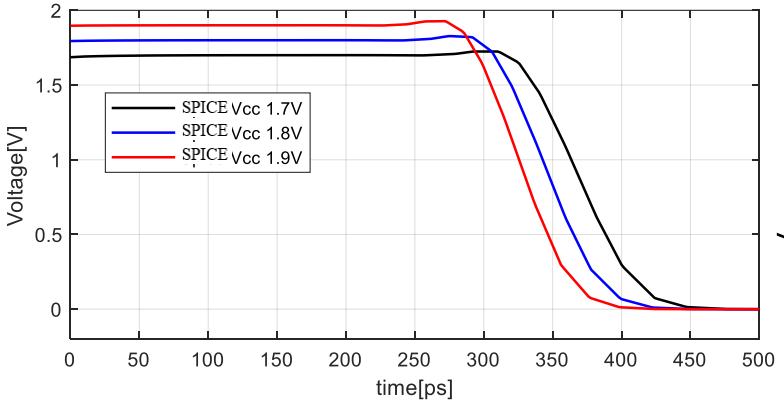
- For non-power-aware IBIS and power-aware IBIS model, the simulated PSIJ sensitivities show the opposite trend to the SPICE results.
- The IBIS model applying the proposed algorithm corrects the trend and reduces the differences to less than 7%.

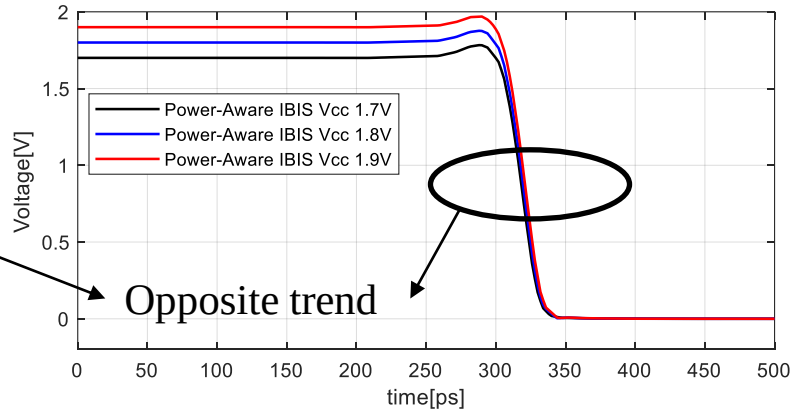
Validation – Output Waveform Comparison – with 2 pF Load

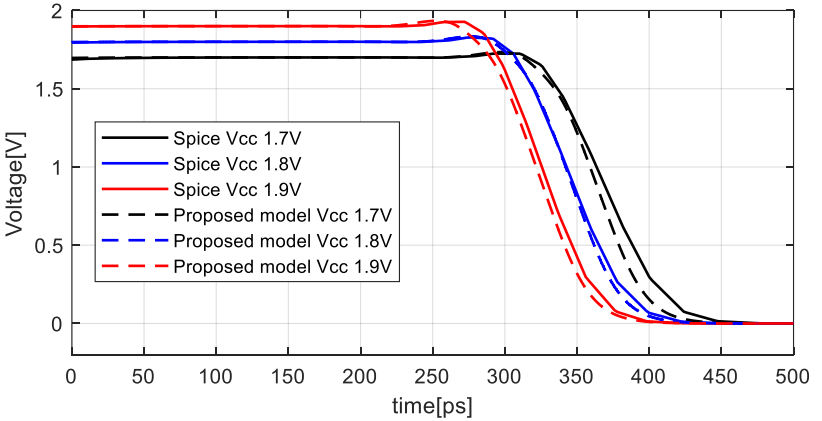






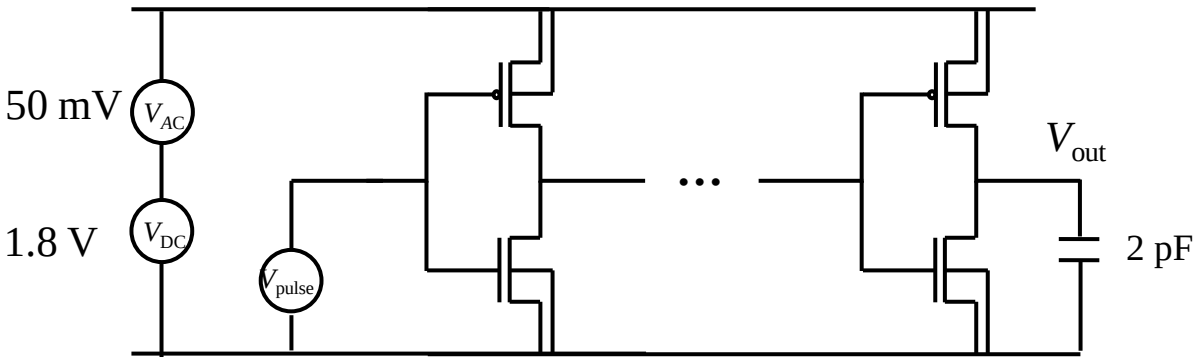




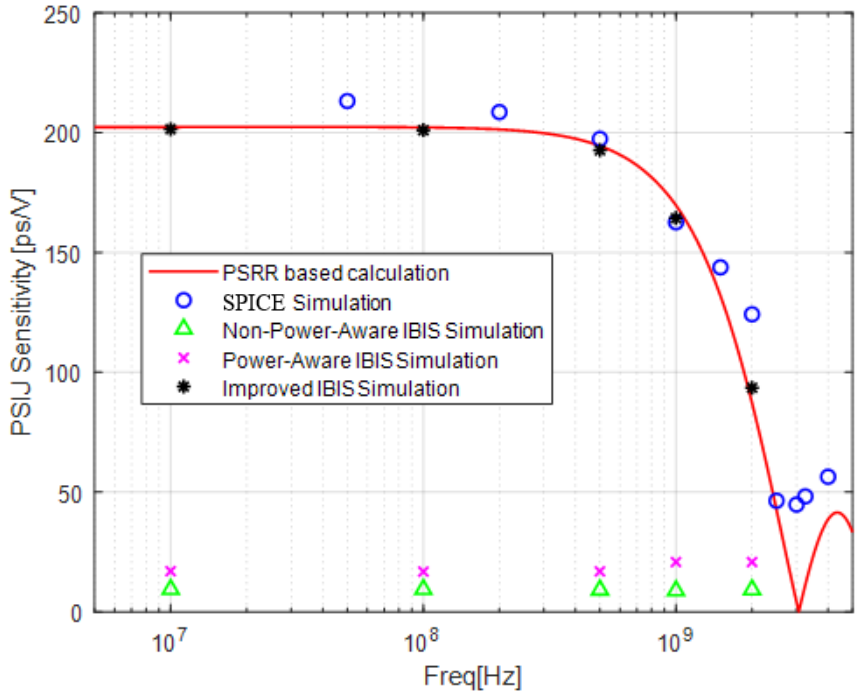


<SPICE> **<Power-aware IBIS Model>** **<PSIJS-based Model (Compared to SPICE)>**

Improvement for AC Noise Cases – Inverter Chain Output Rising Edge

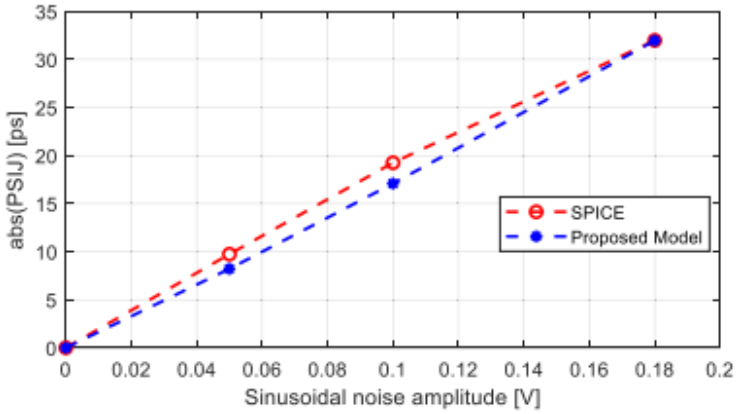


<8-Stage Inverter Chain Simulation Setup with AC Power Noise>



<PSIJ Sensitivity with AC Noise >

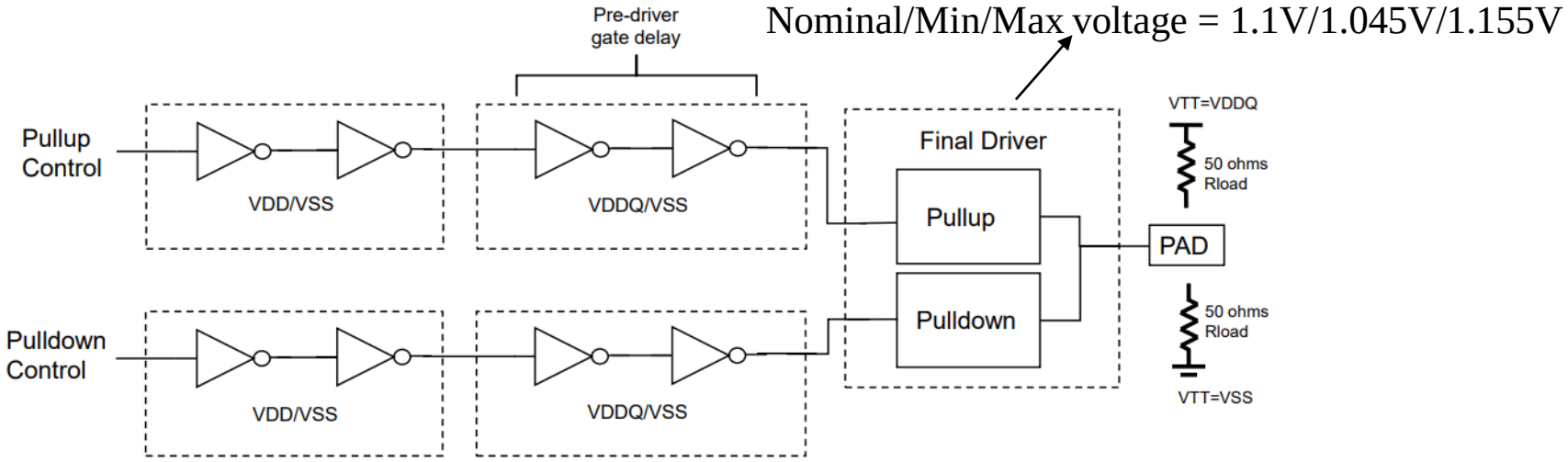
- DC Jitter Sensitivity is required for input, but the usage situation can be extended to the AC noise case.



<PSIJ Sensitivity with different AC Noise Amplitude at 1 GHz >

Simulation Validation – DDRx DQ Tx Buffer

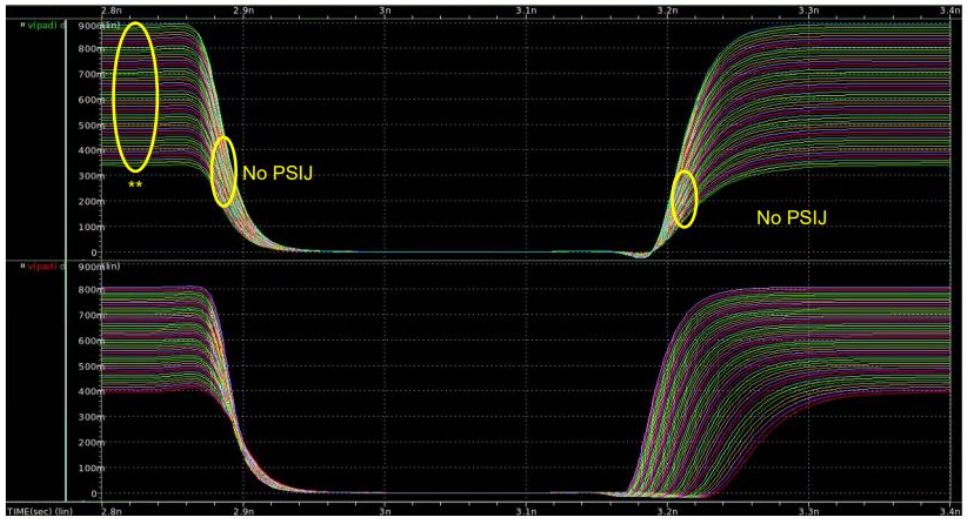
- DDRx DQ Tx Buffer with Pre-driver



- VDDQ Sweep 0.85-1.35V
- Typ Corner
- R_Load = 50 ohm
- $V_{TT} = V_{SS}$

IBIS

SPICE



https://ibis.org/atm_wip/archive/20211026/randywolff/Output%20Buffer%20PSIJ%20Analysis/Micron_PSIJ_Analysis_for_IBIS_ATM.pdf

Improvement for DC Noise Cases – DDRx DQ Tx Buffer Output Rising

- DDRx DQ Tx Buffer with Pre-Driver
- DC power noise 1.045V/1.1V/1.155V

	PSIJ Sensitivity (ps/V)					
	Load 50 ohm to V_{SS}		Load 50 ohm to V_{DDQ} (variable)		Load 50 ohm to V_{DDQ} (Fixed 1.1V)	
SPICE	**-156.65**		**-134.17**		**-95.45**	
Non-Power-aware IBIS	-15.45		-38.18		-6.36	
Power-aware IBIS	-60		-45.45		-14.55	
Proposed Model	**-159.09**		**-147.27**		**-107.27**	
	Δ (to SPICE)					
	Absolute error (ps/V)	%	Absolute error (ps/V)	%	Absolute error (ps/V)	%
Non-Power-aware IBIS	141.2	90.14	95.99	71.54	89.09	93.34
Power-aware IBIS	96.65	61.70	88.72	66.13	80.9	84.76
Proposed Model	**2.44**	**1.56**	**13.1**	**8.9**	**11.82**	**12.38**

- The output PSIJ sensitivities of the traditional non-power-aware and power-aware IBIS models are more than 60% different from the SPICE circuit simulation results.
- The difference is reduced to less than 13% after applying the proposed algorithm.

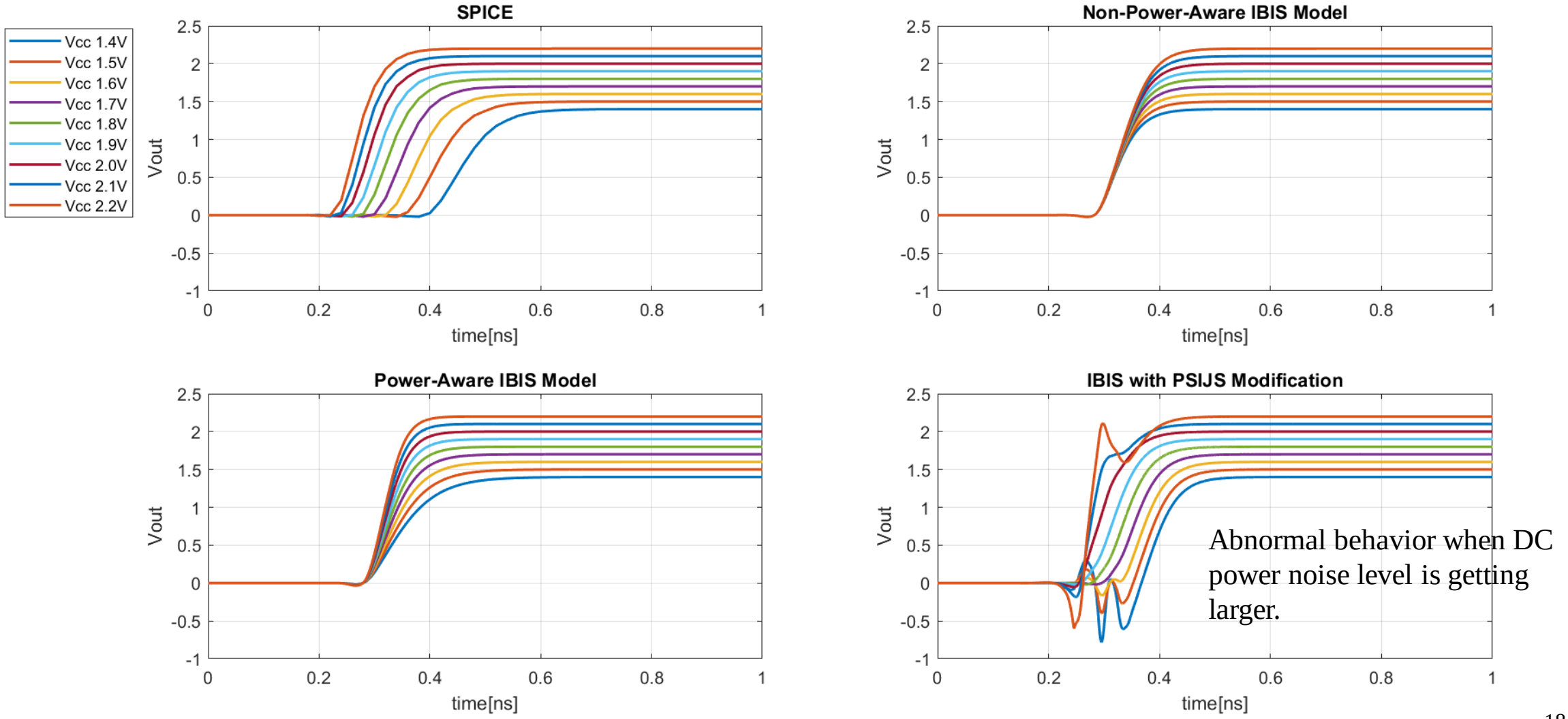
Feedbacks from IBIS ATM Group for BIRD220

- The extraction process is complicated.

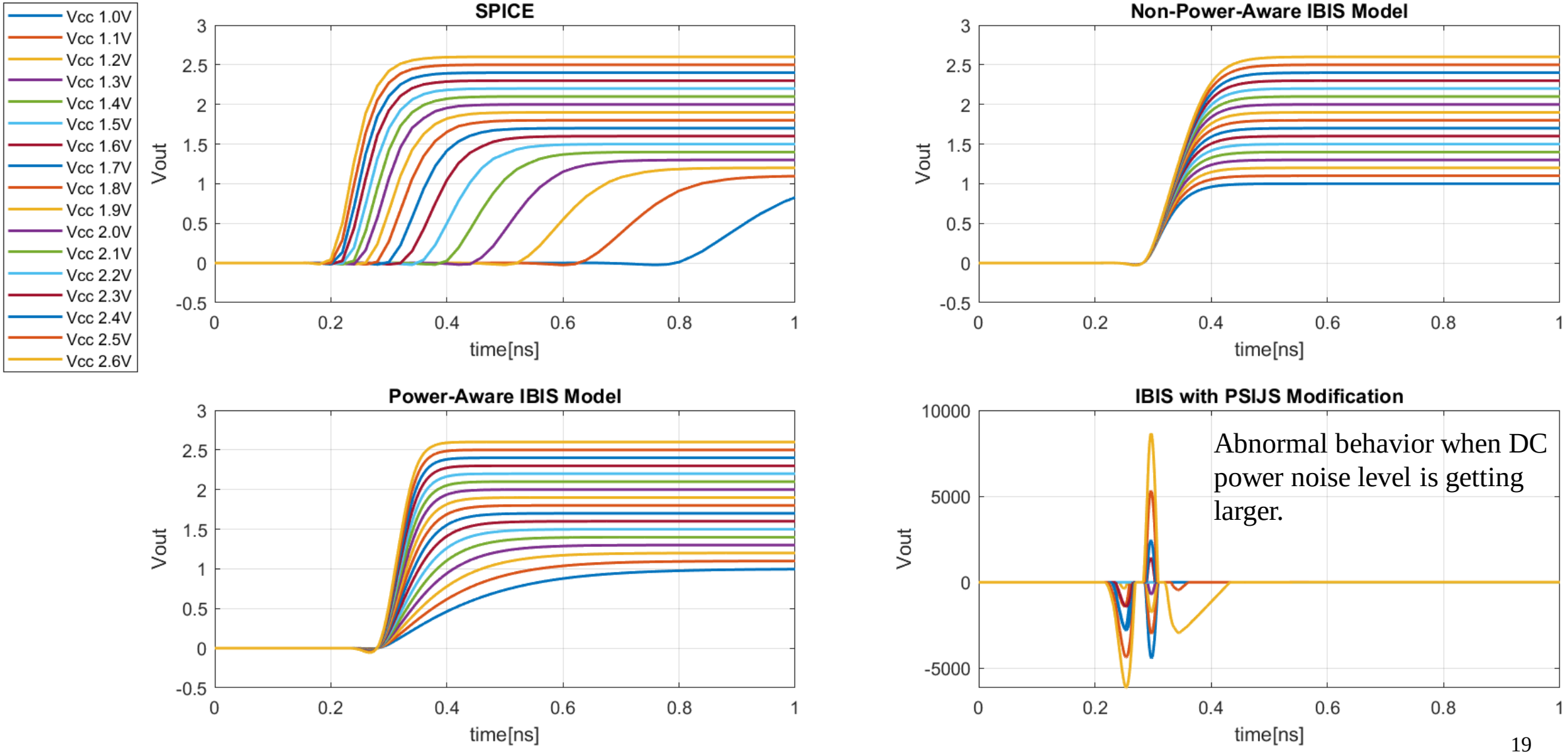
- Performance for power supply voltage in a wider range.

Further Validation and Limitation: When Power Noise is Getting Larger

- The modified model has poor compatibility with high levels of power noise.

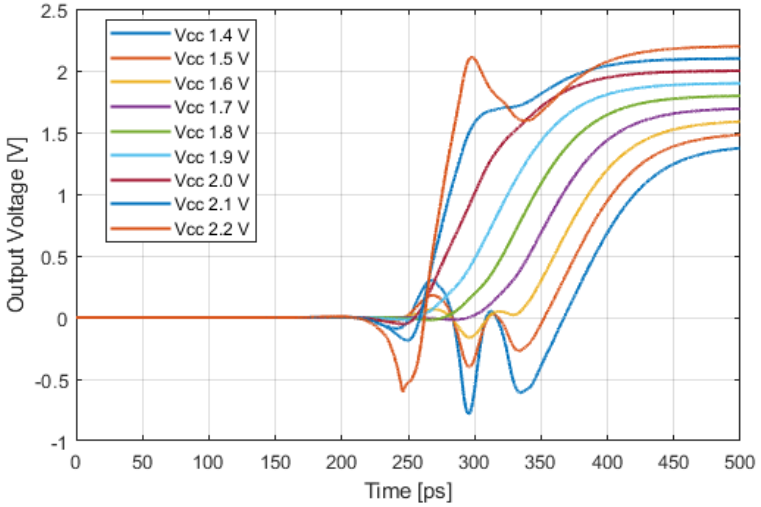


When Power Noise is Getting Larger (Cont.)

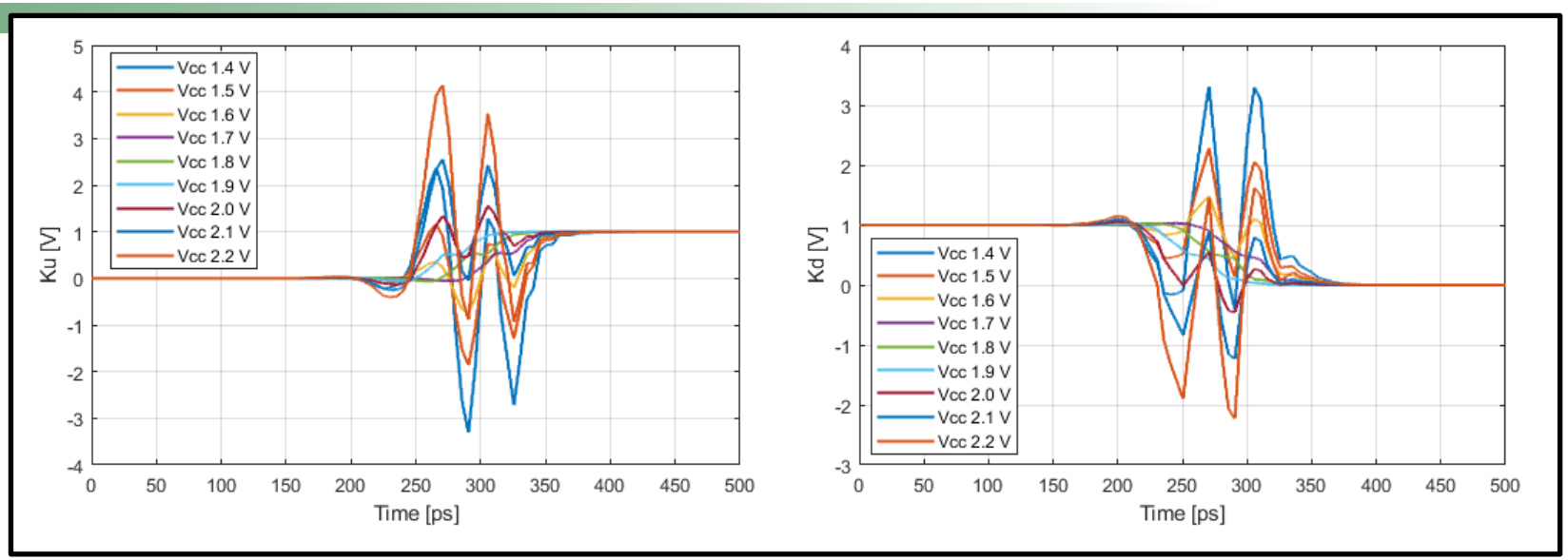


Root Cause – Correction Coefficient Dominates

$$K(t) = K(t) + B(t) \cdot \left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right] + A(t)\left[\frac{\int_0^t V_{cc}(\tau)d\tau}{t} - V_{cc0}\right]^2$$

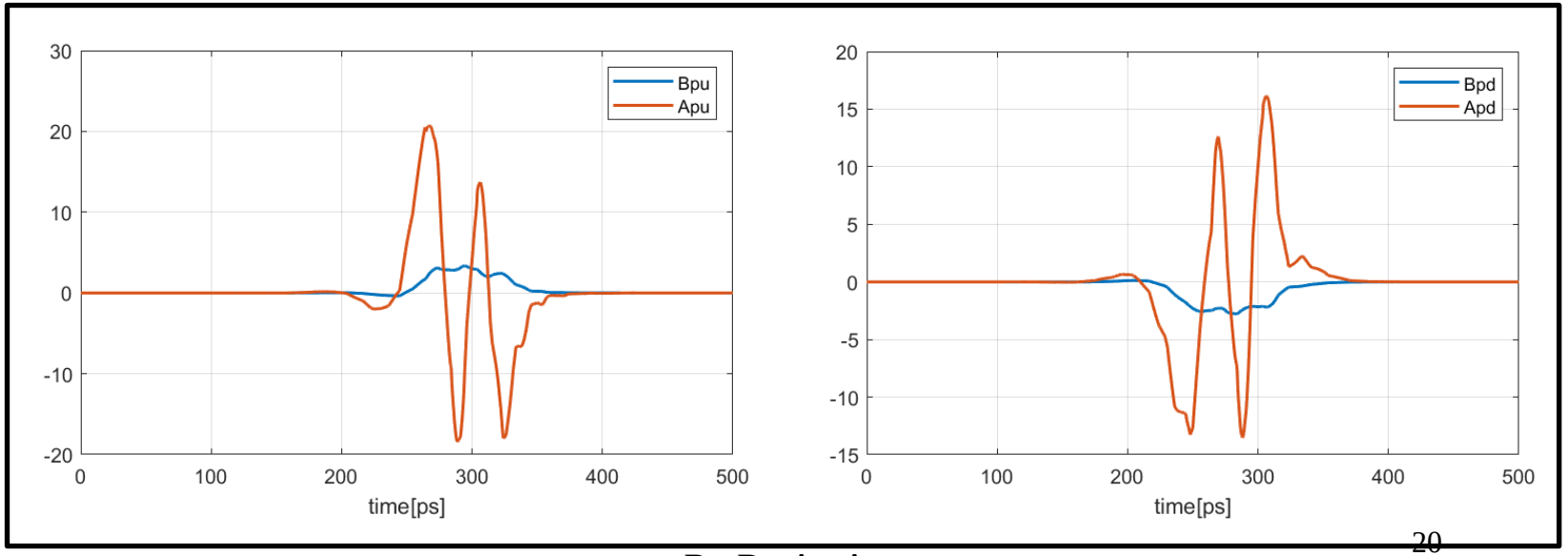


<Output with varying power supply voltage DC noise>



<K_u, K_d>

- A_{pu} and A_{pd} become dominate when the noise level increase.
- K_u and K_d show abnormal behavior, thus leading poor output performance.



<B_u, B_d, A_u, A_d >

Updates – Jitter Sensitivity-Based Direct K_u/K_d Modification

- Avoid the introduction of correction coefficient.
- Update the K_u coefficient simultaneously considering the time difference caused by the averaged power supply noise.
- No out of boundary coefficient value.

Power supply voltage noise affects K_u/K_d coefficients

$$V_{i\_avg} = \frac{\int_0^{t_i} V_{cc}(\tau)d\tau}{t_i} - V_{cc0}$$

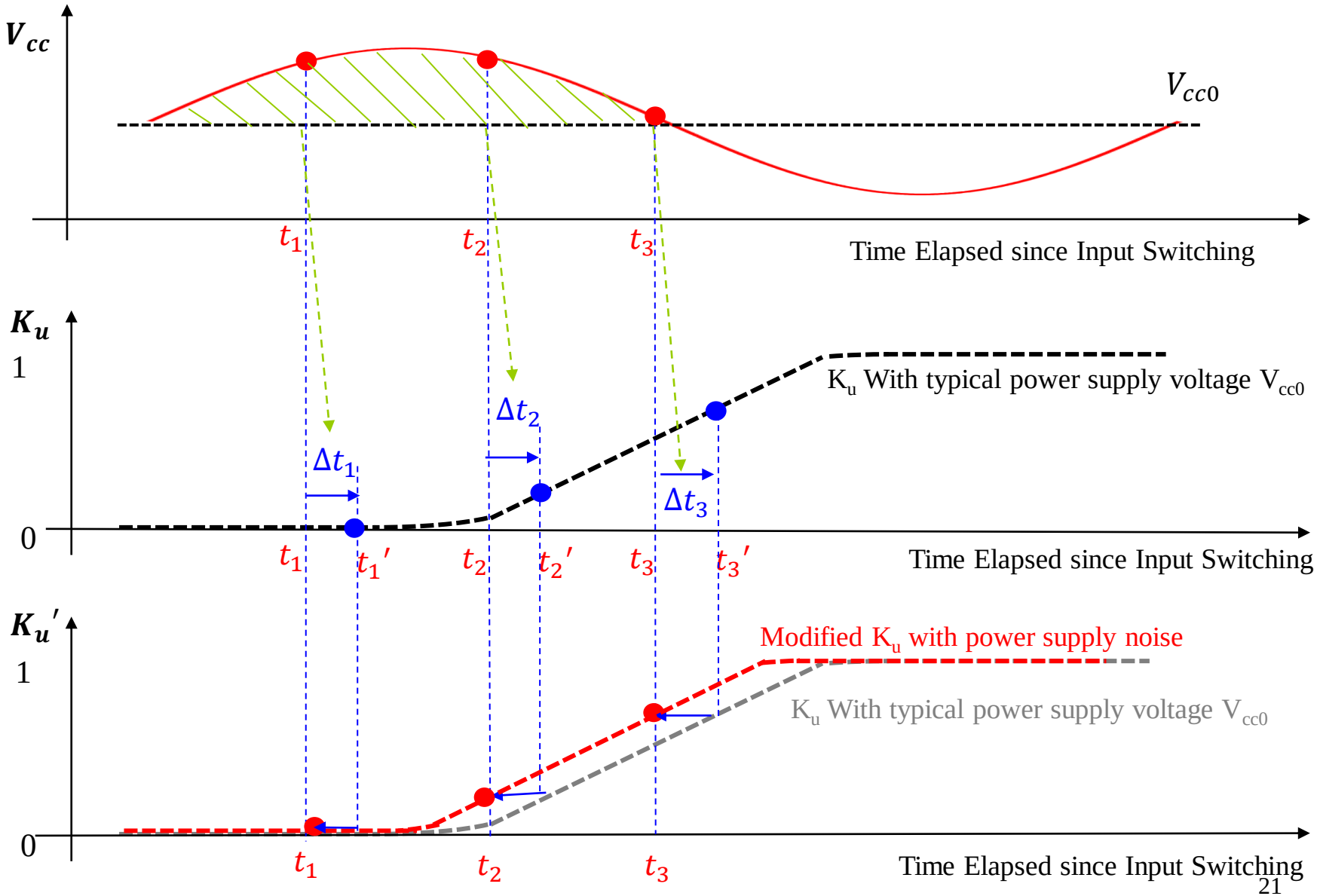
$$\Delta t_i = V_{i\_avg} \times \boldsymbol{DC\_PSIJS}$$

$$t_i' = t_i + \Delta t_i$$

$K_u(t)$ Typical K_u

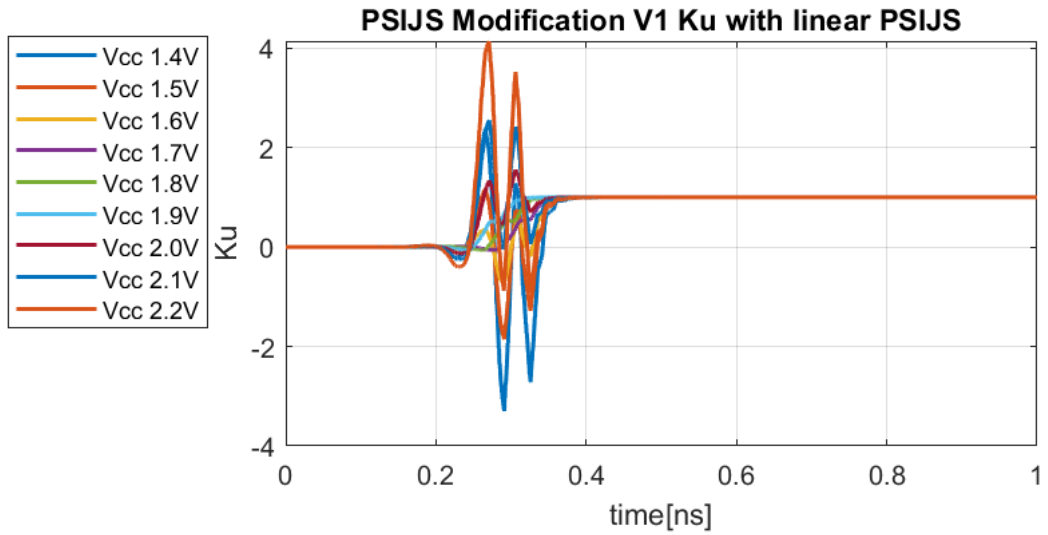
⇩ With Vcc noise

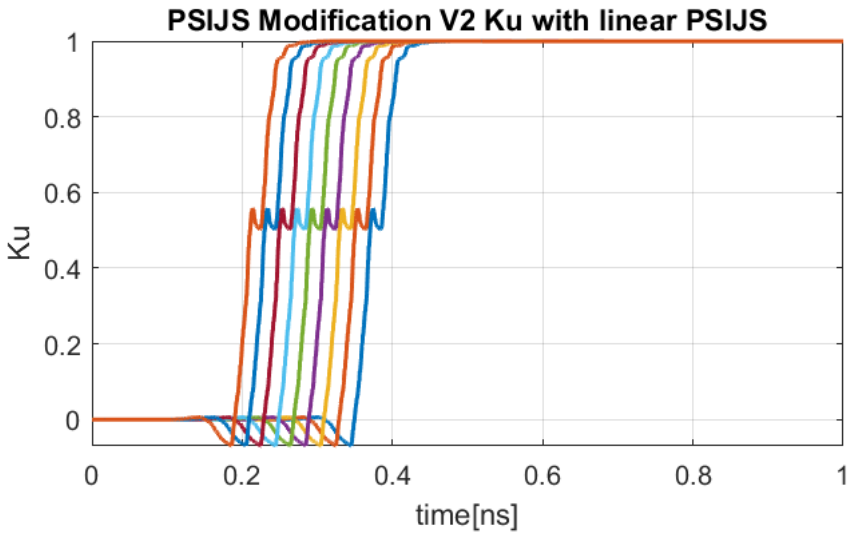
$K_u(t + \Delta t)$ Modified K_u

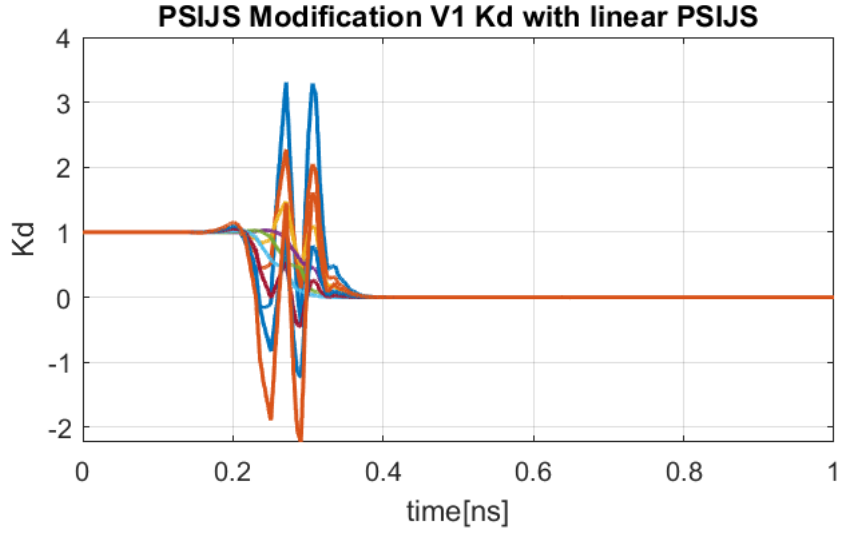


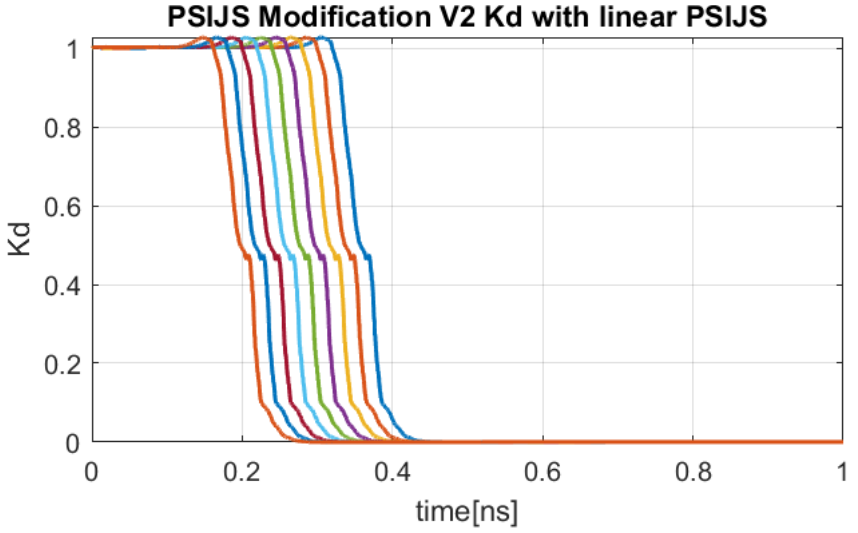
K_u/K_d Comparison for the two Modification Methods

- No out of boundary coefficient value with the direct K_u and K_d modification (v2).

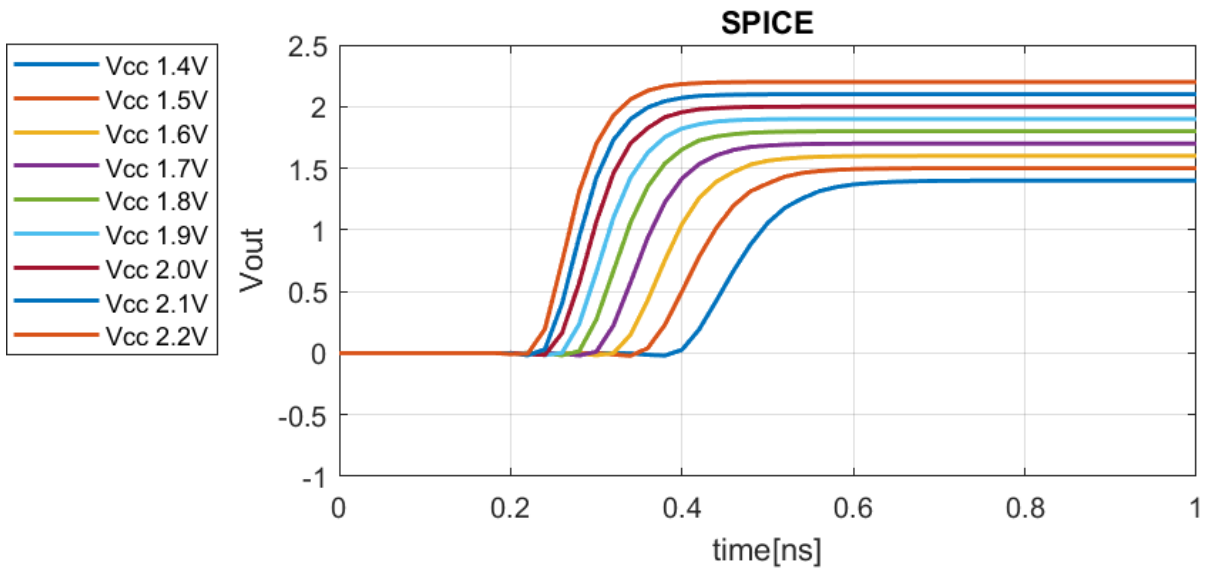


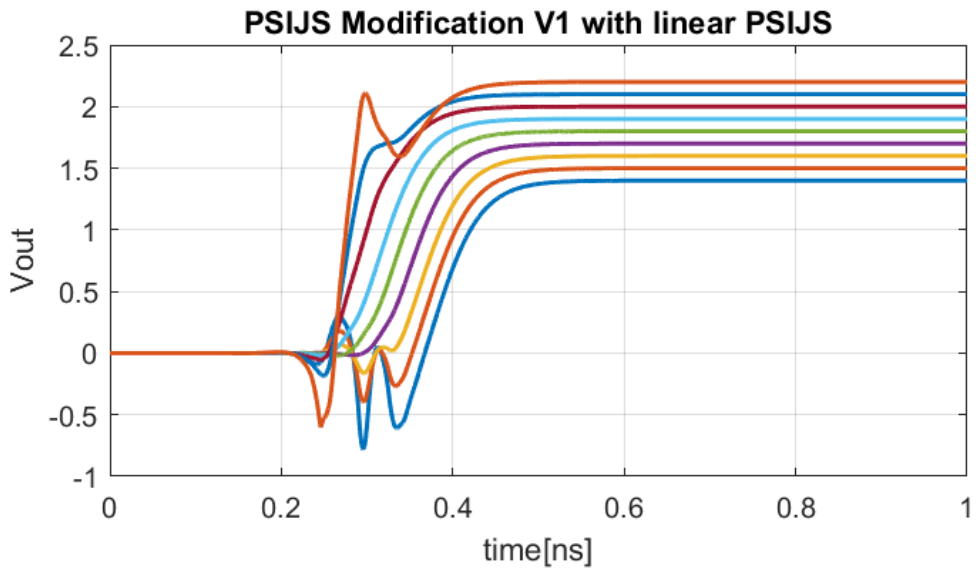


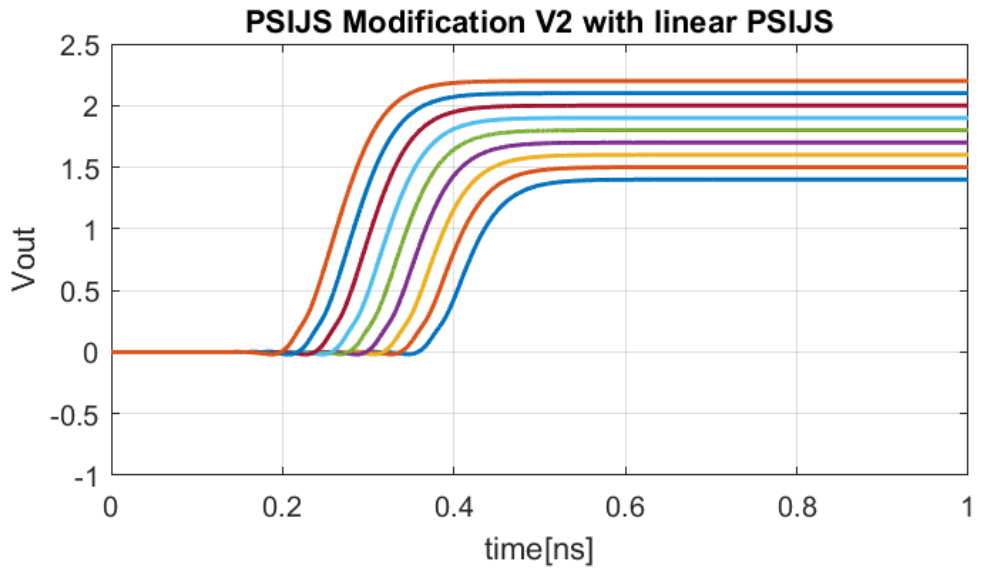




Output Waveform Comparison for the two Modification Methods

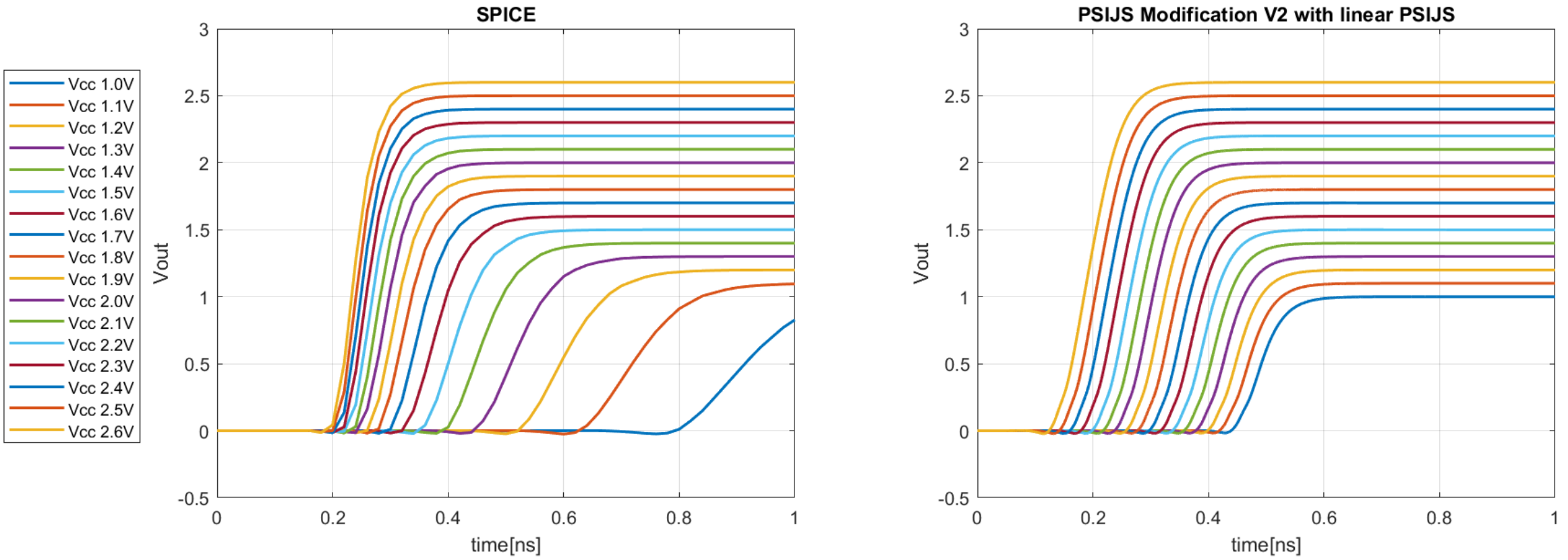






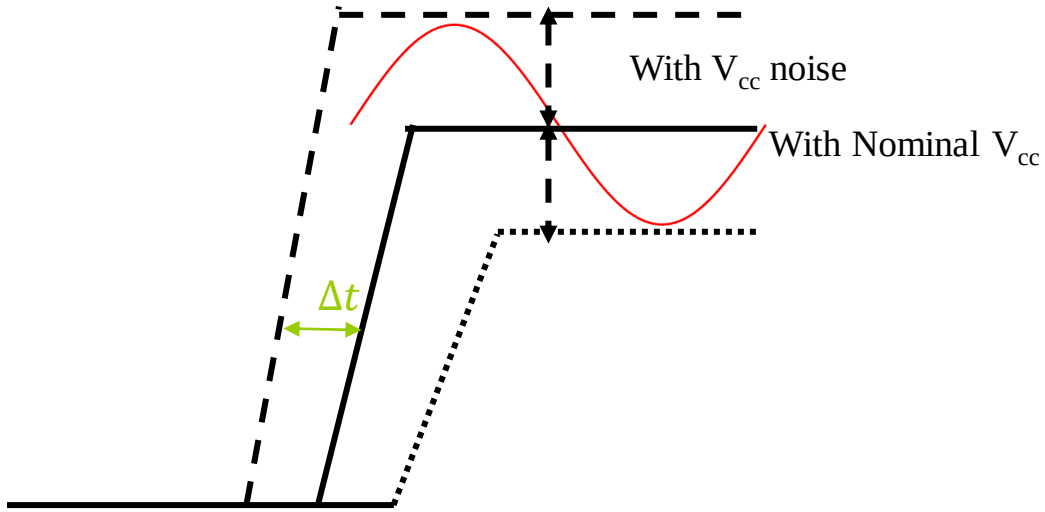
- The PSIJ sensitivity based direct K_u/K_d modification method ensures that the coefficients are within the allowed range, and thus provide better output performance when the power supply noise is large.

When Power Noise is Getting Larger

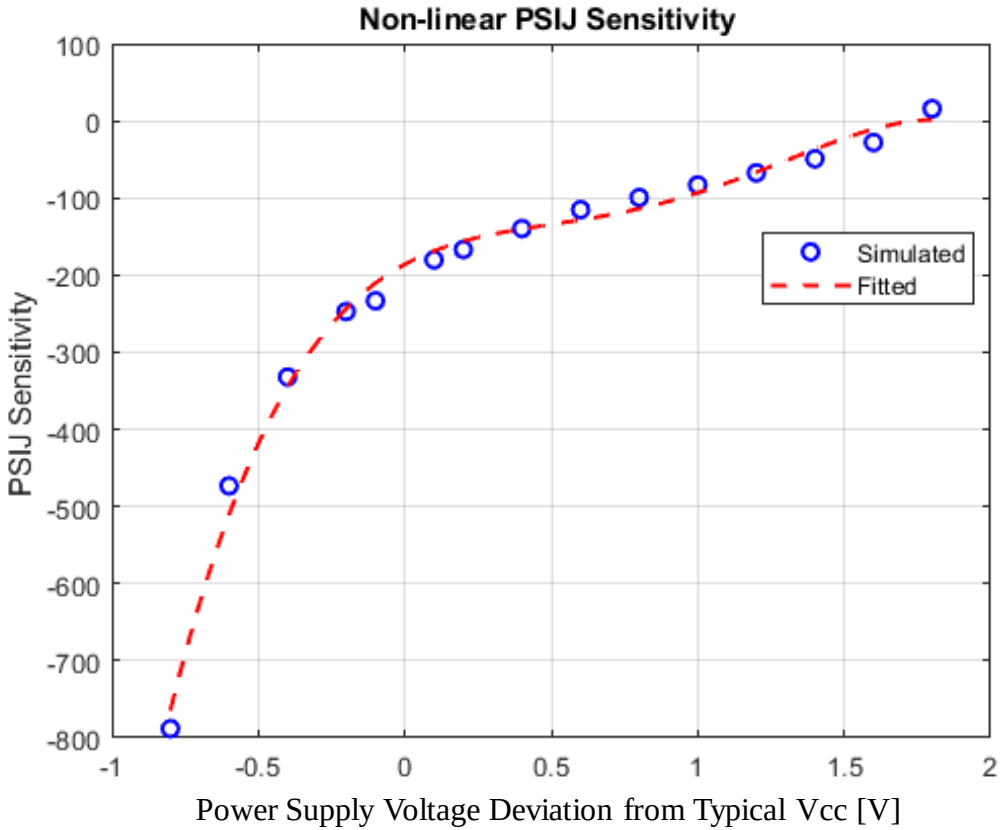


- When continuing extending the power supply voltage range, the output PSIJ sensitivity cannot be correctly characterized.
- The DC PSIJ sensitivity used in the modification is a “linear” concept.

Non-linear DC PSIJ Sensitivity



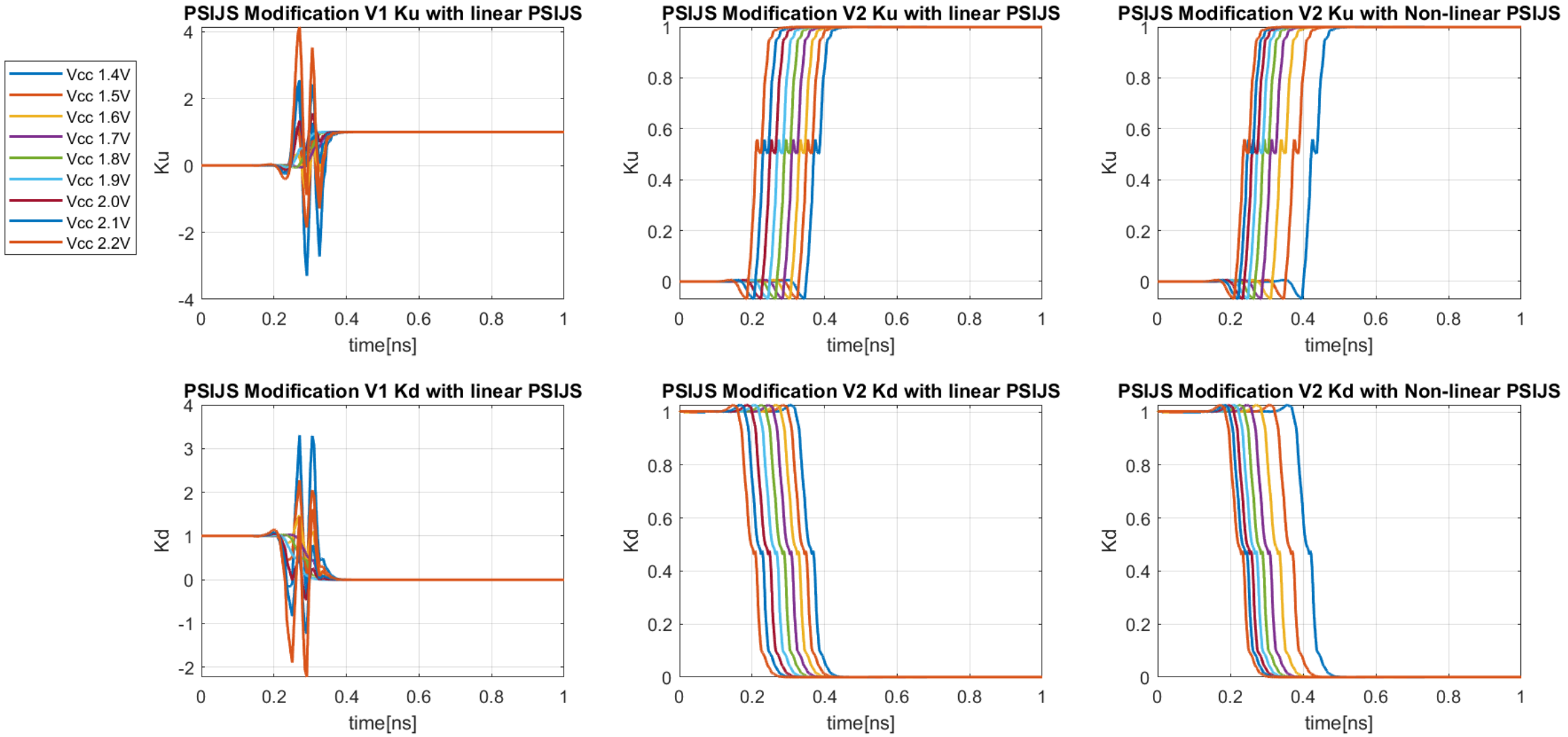
<V_{out} with Power Supply Noise>



$$DC\_PSIJS = \frac{T_{pd} - T_{pd\_typ}}{V - V_{typ}}$$

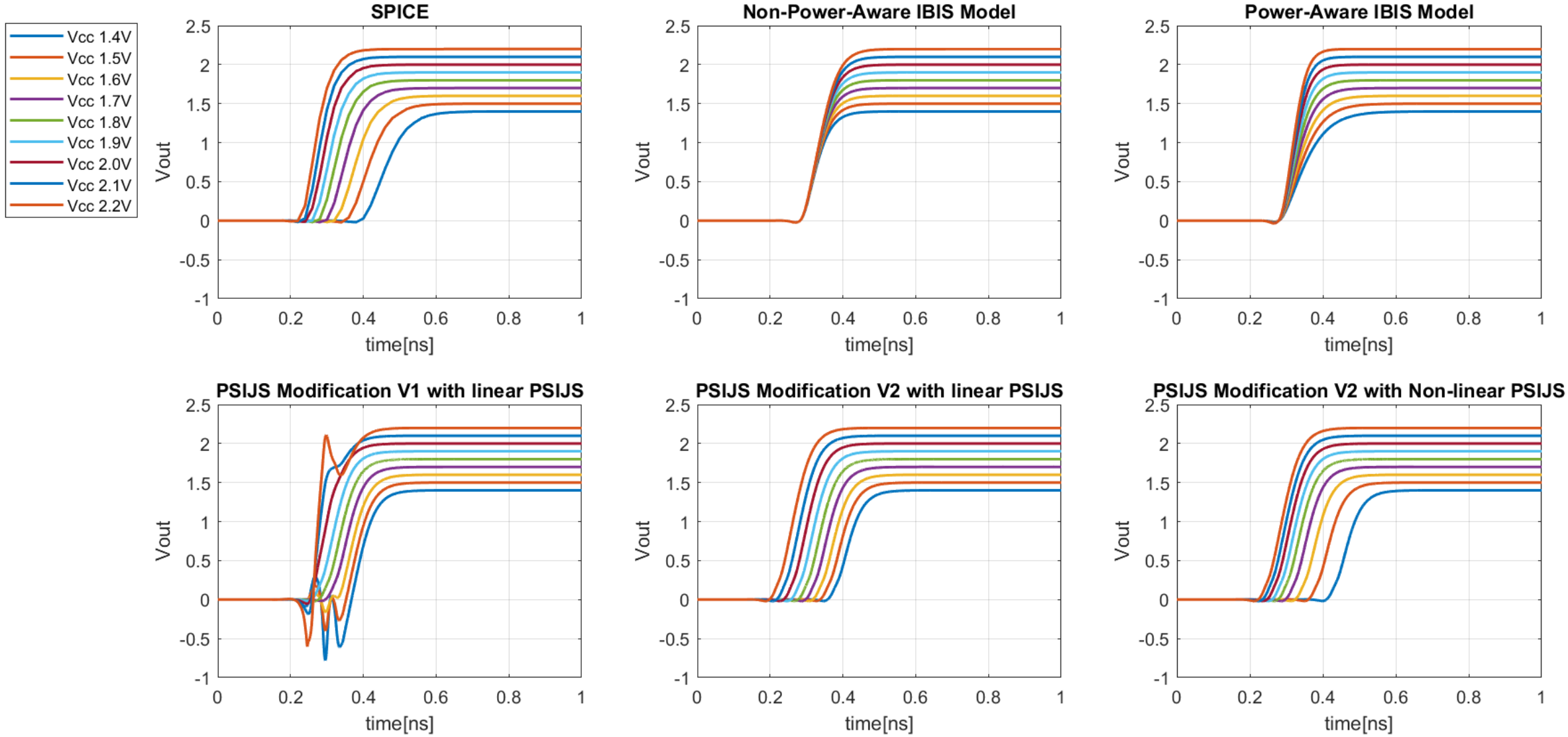
- The DC PSIJ sensitivity is a function of power supply noise amplitude.
- When the noise amplitude is small, DC jitter sensitivity can be treated as linear.
- When noise is larger, jitter sensitivity shows obvious non-linear behavior.

K_u/K_d Comparison for the two Modification Methods

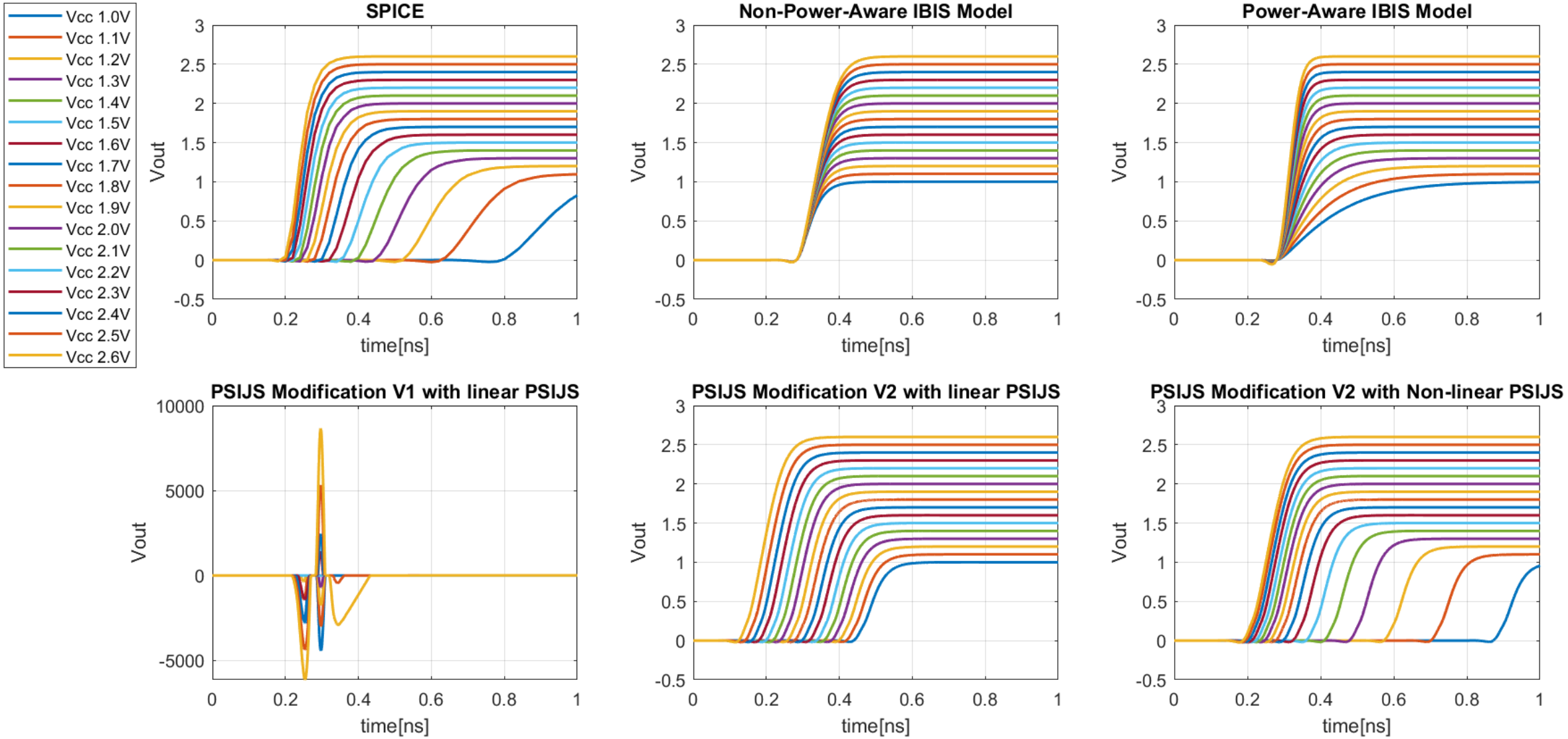


- The modification on K_u and K_d for the first two methods relate to the non-linear PSIJ sensitivity.

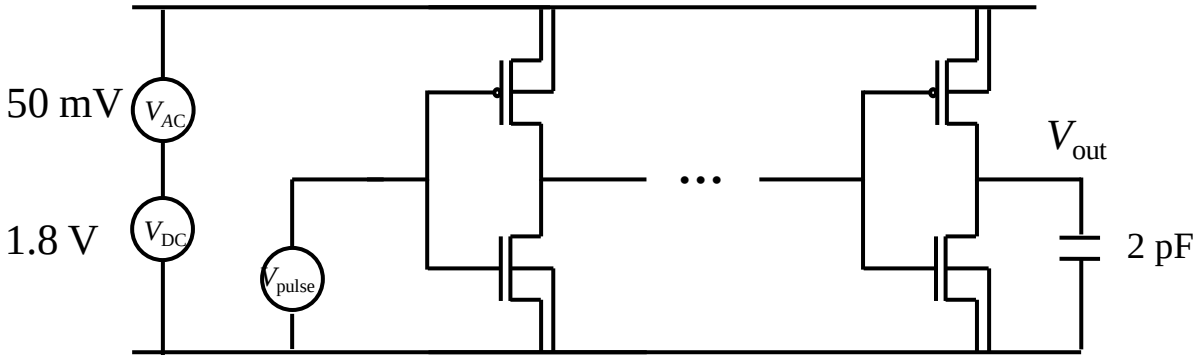
Output Waveform Comparison



Output Waveform Comparison (Cont.)

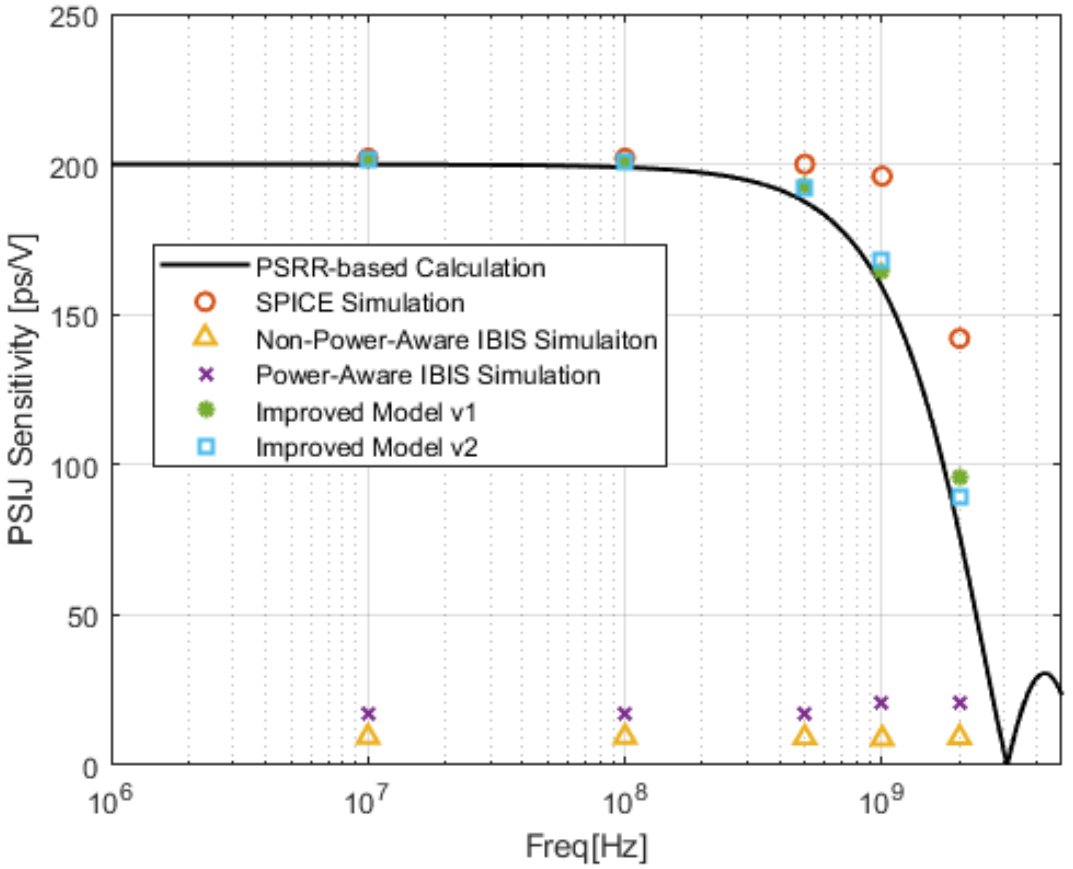


Improvement for AC Noise Cases – Inverter Chain Output Rising Edge



<8-Stage Inverter Chain Simulation Setup with AC Power Noise>

- The SPICE circuit simulation and the improved IBIS model simulation using two version of modification method show good correlation when the power noise frequency changes.



<PSIJ Sensitivity with AC Noise >

BIRD 220.1 Proposal

Keyword: **[PreDrv PSIJ Rising_edge] and [PreDrv PSIJ Falling_edge]**

Required: No

Description: Used to describe the pre-driver output rising and falling edge DC power supply-induced jitter (PSIJ) sensitivity related to the changes in voltage of the Pullup_ref terminal of a [Model], which includes the impact on the overall driver output caused by power noise present on the pre-driver. The pre-driver PSIJ under different voltage deviation to the Pullup_ref voltage should be provided, then the PSIJ sensitivity will be calculated accordingly for K_u and K_d modification.

Sub-Params: NA

<Example>

[PreDrv PSIJ Rising_edge]			unit(s)	
|Voltage Deviation	typ	min	max	
|				
| .				
| .				
-0.2V	25p	26p	24p	
-0.15V	18p	18.5p	17.5p	
-0.1V	11p	12p	10p	
-0.05V	5p	6p	4p	
0V	0p	0p	0p	
0.05V	-4p	-5p	-3p	
0.1V	-8p	-10p	-7p	
0.15V	-11p	-12p	-10p	
0.2V	-15p	-16p	-14p	
| .				
| .				

[PreDrv PSIJ Falling_edge]			unit(s)	
|Voltage Deviation	typ	min	max	
|				
| .				
| .				
-0.2V	13p	NA	NA	
-0.15V	8p	NA	NA	
-0.1V	5p	NA	NA	
-0.05V	2p	NA	NA	
0V	0p	NA	NA	
0.05V	-0.8p	NA	NA	
0.1V	-1p	NA	NA	
0.15V	-1.5p	NA	NA	
0.2V	-2p	NA	NA	
| .				
| .				

Conclusion

- New jitter sensitivity-based K_u/K_d modification method is proposed to improve the IBIS power supply induced jitter simulation accuracy.

- Works for both DC and AC power noise induced jitter prediction and is applicable with large voltage noise with non-linear jitter sensitivity.

- Provide straightforward modification based on only one keyword relates to power supply voltage fluctuation.

Thank you

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