All start from V=Z*I for platform PI & PD design

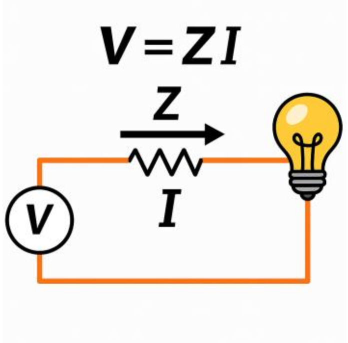
Xingjian Kinger Cai (arm Ltd.)

Hybrid IBIS Summit at IEEE
EMC+SIPI 2025
Raleigh, North Carolina
August 22, 2025

All starts from V=Z*I for platform PI & PD designs

(PI = Power Integrity & PD = Power Delivery)

- Ohm’s Law in Power Delivery Network (PDN)
- Voltage design target: **Vmin, Vmax, OS, US and Vpp** in TD
- Impedance design target: ACLL3/2/1 and DCLL in FD
- Case Study: SPIM for LPDDR5X in JEDEC



Kinger Cai (arm)

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An SAE Industry Technologies Consortia Program

Speaker

Kinger Cai

- Sr. Principal Engineer, ARM
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Kinger is Sr. PE driving Super AI platform electrical architect design & validation, and industry Power & Signal Integrity standards evolution, in Solution Eng. Group in ARM.

Kinger was a Principal Engineer/Director, in Client Computing Group in Intel, where he led cross-functional teams in driving AI PC coherent architecture strategies across mobile & client platforms and overseen design & sign-off of numerous SoCs spanning media, mobile, client, discrete GPU, & CPU servers.

Kinger earned his Ph. D from Shanghai Jiao Tong University in 2001 and MBA degree from W.P. Carey business school in ASU in 2008.

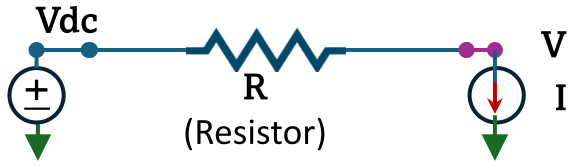
Kinger has been focusing on signal & power integrity domains for 20+ years.

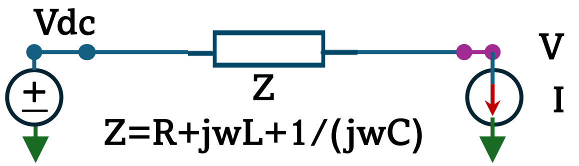
Kinger holds 14 granted patents, and published 30+ papers.

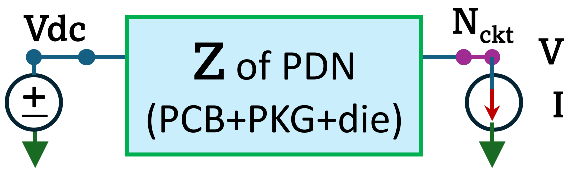
https://sites.google.com/view/fastpi

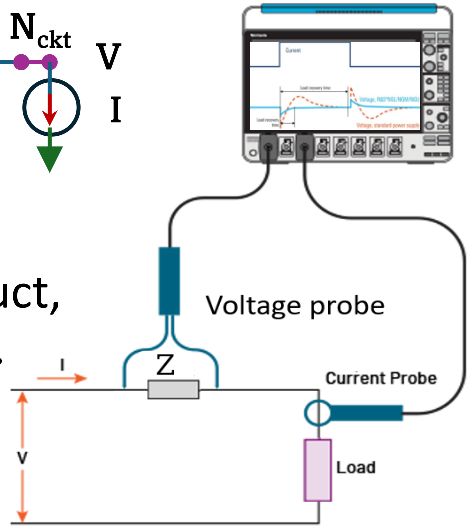
PI & PD Design Starts from Ohm's Law

- V=R*I, for resistive circuits, including resistors, with loading I (i(t) profile)
- V=Z*I, for reactive circuits, including capacitors, & inductors, Z=R+jwL+1/(jwC), Z is frequency dependent

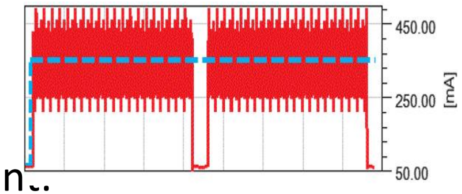






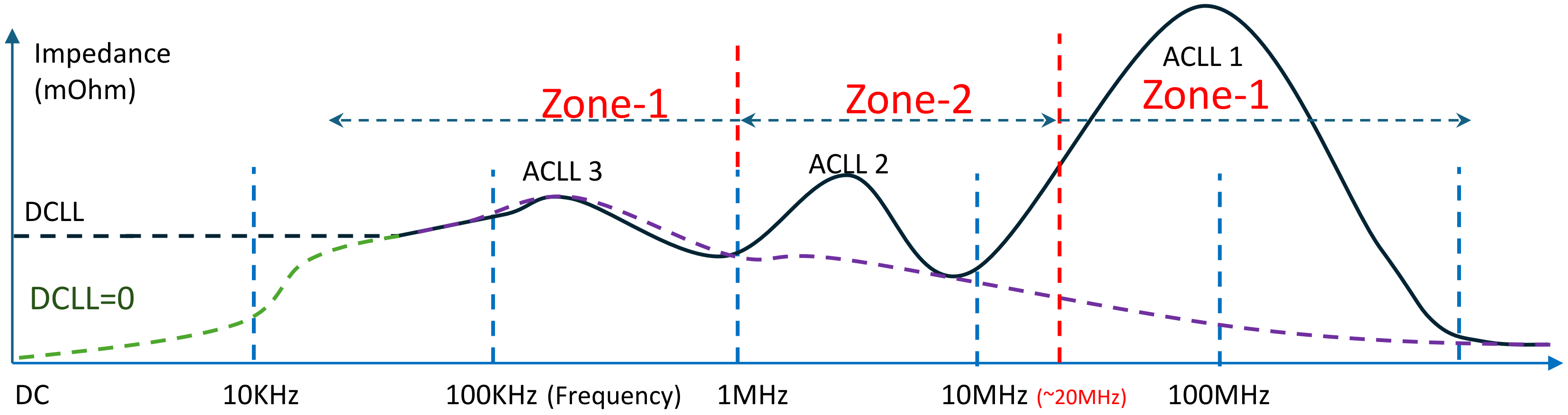


- For the worst-case I with di_max (/dt), which is deterministic for a particular PDN in a product,
  - Vdc can be fixed, or variable during operation. Z can be indirectly measured through probing V & I.
  - If Z is determined, maximum undershoot/Overshoot (US/OS) is also determined.
  - For Z amplitude globally below Zmax, US/OS will <= Zmax* di_max , Vpp <= (Zmax* di_max)*2
  - After a PDN is designed/optimized, its Z is determined, neither its loading I nor its output V.
  - If one PDN can satisfy the PI design requirements in transient design, its Z profile can be set as Ztarget.



- Therefore, at board/PCB level PDN PI design,
  - To satisfy PI design Ztarget (from a chip vendor) in Frequency Domain (FD) is sufficient, and very efficient.
  - To meet PI design targets of US/OS, Vmin/Vmax, and/or Vpp is nice to have, not necessary, most likely not possible, because on-die circuit loading (I) will not be shared by chip vendors, for IP protection, similar situation for IBIS model.

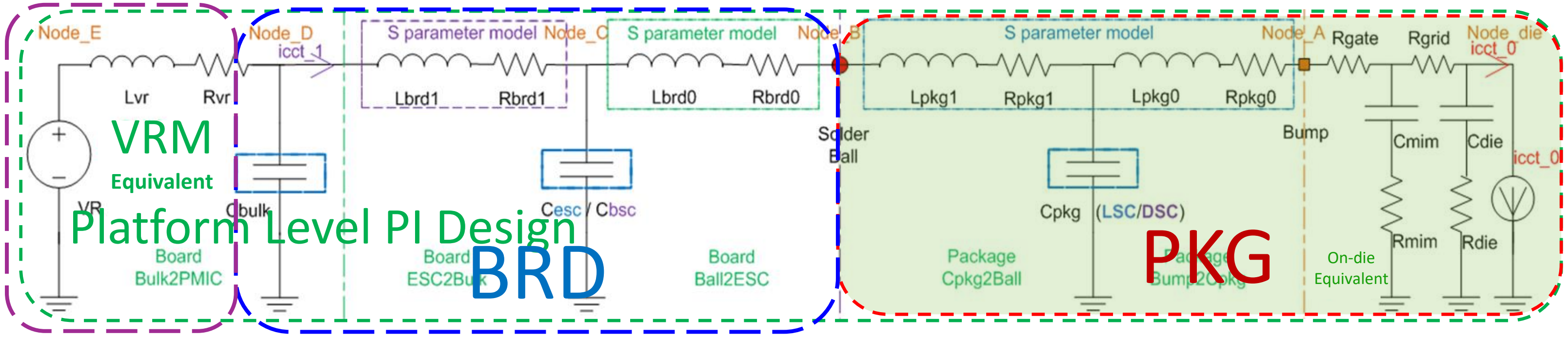
PDN Impedance Curve Decomposition



PDN Z(f) Peaks:

- ACLL1
- ACLL2
- ACLL3
- DCLL

*In modern PDN, ACLL1<ACLL2<ACLL3, with massive MIM, DTC, and TSC/BSC in PKG.
*DCLL is a soft parameter setup in VR controller, does not burn power, different from PDN DC resistance.
*DCLL is totally different concept than DC resistance Rdc (Rpath, Rnonvr, etc.) which burns power of $I^2 Rdc$.

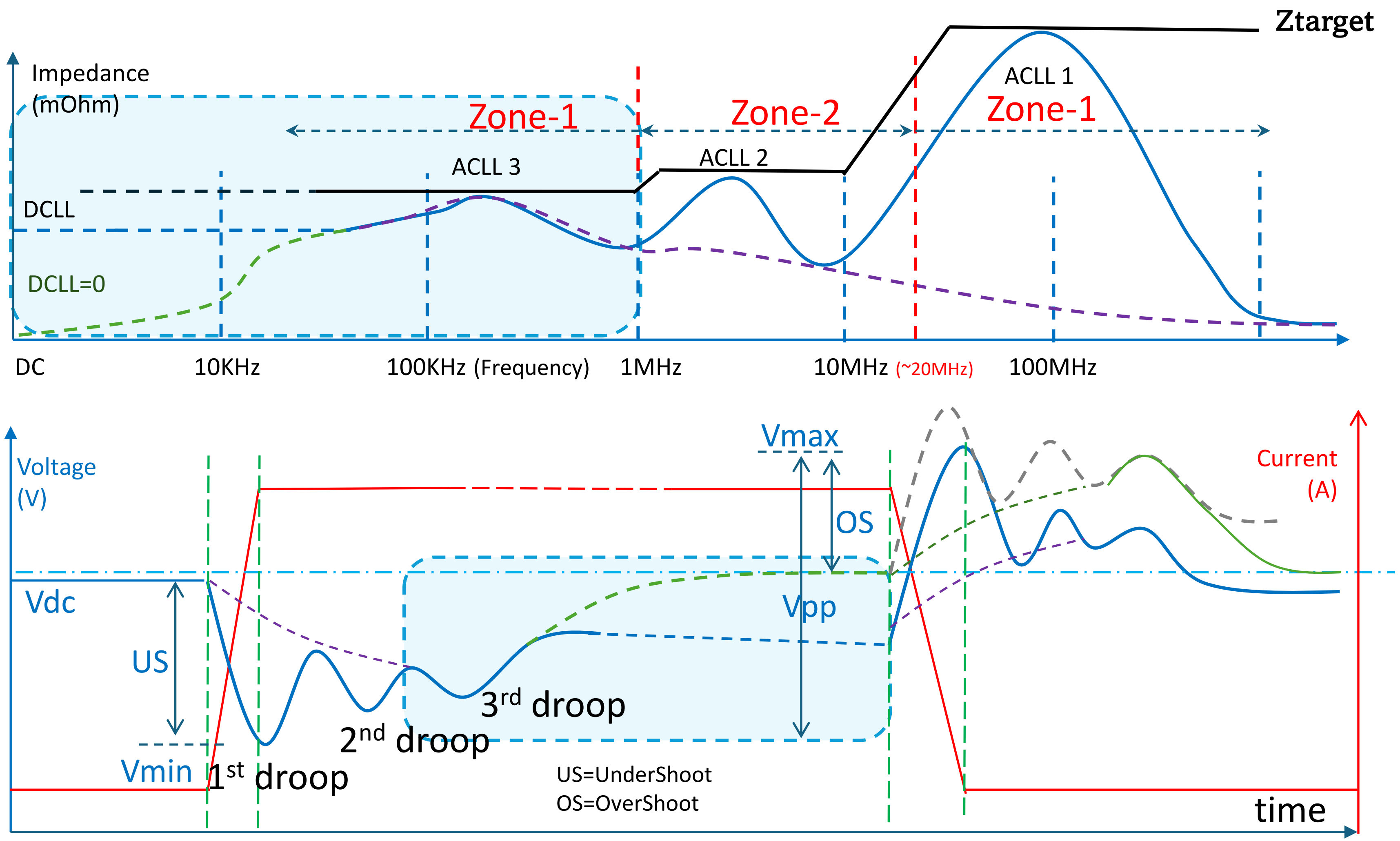


The PDN impedance curve is zoned in FD, each PDN segment of PKG, BRD and VRM will only impact certain zone(s), not the whole frequency range from DC to ~2GHz.

VRM netlist is sophisticated, its modeling shall be a dedicated topic. Please refer to the published IEEE papers:

- VRM Modeling for Platform FastPI upon SPIM, Xingjian Kinger Cai; Wei Qian; Chi-te Chen; Kundan Chand, IEEE Symposium EMC/SI/PI, 2021
- CVRM with Feedback for Platform PDN PI Design, Xingjian Kinger Cai; Yimajian Yan1, and Dong Zhong2, and Sumant Srikant3, IEEE Symposium EMC/SIPI 2025.

PDN Transient Waveform vs. AC Impedance



PDN Z(f) Targets:

- ACLL1Range
- ACLL2 Range
- ACLL3 Range
- DCLL Range

Transient Targets:

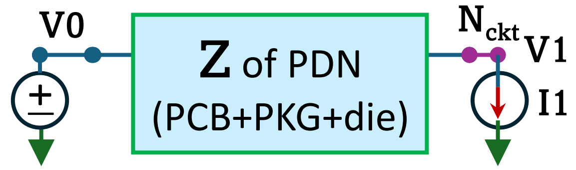
- Vmin / US
- Vmax /OS
- Vpp (IO rails)

DCLL concept shall be a dedicated topic, for its implementation, and pros and cons elaboration.

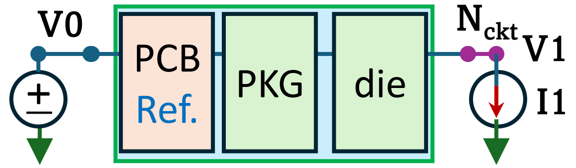
Assumed traditional controller loop, non-linear features such as adaptive clocking shall be a dedicated topic.

Platform PI & PD Design Practice

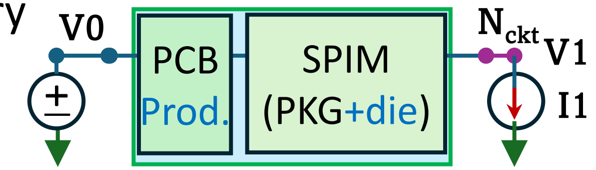
- Platform level PI design is to globally optimize/trade-off PDN routing and decoupling capacitance among on-die, in-PKG and on-PCB including VRM designs.
  - Trade off among performance, power and cost; among on-die, in-PKG and on-PCB.
  - The PDN PI design targets will be nailed down by chip designers before PKG sign-off.
  - Board level PDN PI design is usually required to design a board segment PDN, not worse than that of Chip design's internal reference design motherboard.



- PI design at Chip/PKG level, focusing on DC, Transient and then AC, by Chip vendors
  - V=Z*I, satisfies the given design target of V and loading I from die/ckt designers
  - PDN design and optimization is the focus, in terms of routing and decoupling cap.
  - Z=V/I, shall be nailed down for its up-limit (target), before PKG/die design signoff

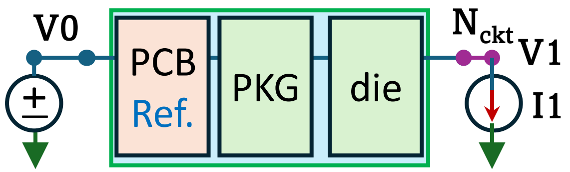


- PI design at platform/PCB level, focusing on DC and AC, rarely on Transient, by OEM/ODMs
  - If PCB level PDN satisfies Z target, so does transient targets, according to V=Z*I theoretically & practically
  - Meanwhile, on-die transient loading current (I) will not be mostly available, necessary
  - PDN Power DC shall satisfy the limits of current and current density, and IR drop

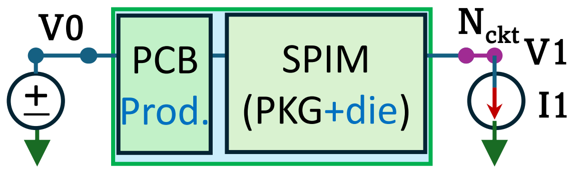


PIPD design Receivables and Deliverables

- PI design, at Chip/PKG level, (Chip vendors)
  - Receivables:
    1) Loading current **I1**, **V0**, and voltage requirements of **V1** (Vmin/Vmax, Vpp) at Node **Nckt**.
    2) On-die PI model, as simply as 1st order lumped RLC model, or sophisticated CPM model



  - Deliverables:
    1) Optimized PDN routing in PKG with sufficient decoupling capacitors, internally within Chip vendor
    2) Design targets usually impedance target in FD, from DC up to ~20MHz (why that is the common practice in the industry)
    3) SPIM at chip/PKG level, including the socket if it exists, Imax of max loading, and BGA level di/dt for VRM/PD design
    4) Imax (maximum averaged current at highest performance), for Power DC analysis, Imin (leakage current), or di & dt for PD
- PI design, at platform/PCB level, (OEM/ODMs)
  - Receivables:
    - (deliverables #2/3/4, from Chip vendors)
  - Deliverables:
    - Optimized PDN routing in PCB with sufficient decoupling capacitors,
      - meeting PI design target of impedance in FD
      - meeting power DC analysis of current and current density limits



Case Study:

1854.99C_CB23019-Proposed LPDDR5 LPDDR5X Specification Revision C.pdf

JEDEC Spec:

- Z(f) targets are defined at pin/BGA level PKG-less for all major power rails of VDD1, VDD2L, VDD2H, & VDDQ.
- From 2MHz to 10MHz, and then to 20MHz.

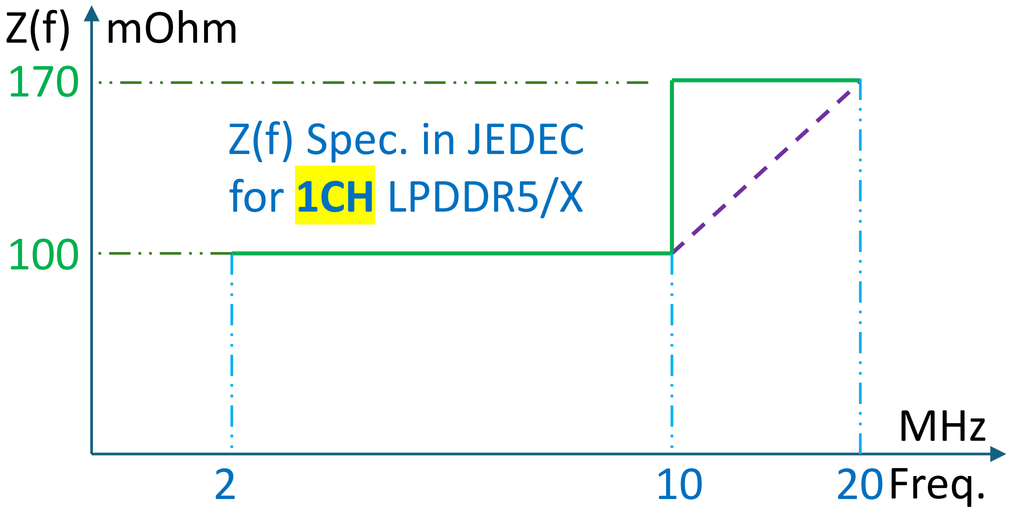
Table 384 — Recommended Voltage operating conditions

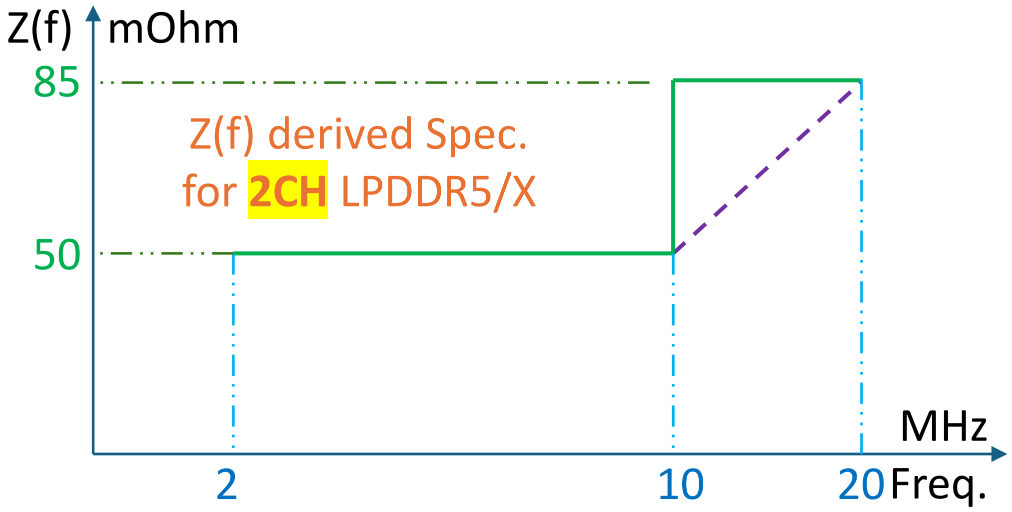
			Low Freq Voltage Spec Freq:DC to 2 MHz				Z(f) Spec Freq: 2 MHzto 10 MHz		Z(f) Spec Freq: 20 MHz		
DRAM	Symbol		Min	Typ	Max	Unit	Zmax	Unit	Zmax	Unit	Notes
Core 1 Power	VDD1		1.7	1.8	1.95	V	100	mOhm	170	mOhm	1,2,9
Core 2 Power/Input Buffer Power	VDD2H		1.01	1.05	1.12	V	40	mOhm	80	mOhm	1,2,9
	VDD2L	Single Core Power Rail (MR13 OP[7]=1B)	1.01	1.05	1.12	V	120	mOhm	190	mOhm	1,2,9
		Dual Core Power Rail (MR13 OP[7]=0B)	0.87	0.9	0.97						
I/O Buffer Power	VDDQ	SPEC Range-1	0.47	0.5	0.57	V	40	mOhm	80	mOhm	2,3,6,9
		Spec Range-2	0.27	0.3	0.37	V					2,4,9
		Allowable Range	0.27	N/A	0.57	V	N/A		N/A		5,6,7,8

NOTE 1 VDD1 uses significantly less current than VDD2H and VDD2L.
NOTE 2 DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations. This noise is included in the aperture mask defined by VdIVW. Refer to Figure 291.
NOTE 3 SPEC Range 1 is intended for IO operation with both ODT enabled and disabled.
NOTE 4 SPEC Range 2 is intended for IO operation with ODT disabled.
NOTE 5 IO operation at VDDQ levels between outside SPEC Range 1 or SPEC Range 2 is allowed with ODT disabled.
NOTE 6 Allowable range is valid only when DVFSQ enabled.
NOTE 7 100mV tolerance (-30mV/+70mV) is applied to VDDQ allowable ranges. Refer to Figure 292.
NOTE 8 Vendors may support LPDDR5 (MR8 OP [1:0] = 00B) 0.6V and LPDDR5X (MR8 OP [1:0] = 01B) 0.45V VDDQ (typ) as an option. Because ZQ calibration is optimized at VDDQ=0.5V, the output drive strength may not be guaranteed at LPDDR5 0.6V and LPDDR5X 0.45V. Refer to a vendor's data sheet.
NOTE 9 Z(f) is defined for all pins per voltage domain per channel. Z(f) does not include the DRAM package and silicon die.

One Example Z(f) Spec for VDD1 of LPDDR5/X

- Z(f) Spec is assumed step transition at 10MHz, because the Z(f) transition from 10MHz to 20MHZ is not explicitly defined in JEDEC for LPDDR5/X. But linear transition is more practical, & restrictive to satisfy.





That doubles the loading & halves PDN impedance target, result in the same values of Vmin, Vmax and Vpp.

LPDDR5X Devices Power/GND Pins

- Power pin information in 315-ball 2CHx32 PKG for major power rails

  VDD1:
  C1, C15, W1, W15

  VDD2L:
  A6, A10, B6, B10, H2, H14, J2,J14,N2, N14, P2, P14, Y6, Y10, AA6, AA10

  VDD2H:
  A7, A8,A9, B7, B9, C7, C9, D8, E7, E9,F6, F7 F9, F10,J5, J11, K1,K2,K3,K4,K5,K6, K10, K11,K12,K13, K14, K15,L6,L7, L8,L9,L10,M1,M2,M3,M4, M5, M6, M10, M11, M12, M13, M14, M15, N5, N11, T6,T7, T9, T10, U7, U9, V8, W7,W9, Y7, Y9, AA7, AA8, AA9

  VDDQ:
  A3, A13, B2, B14, C3, C13, D4, D12, E5, E11,F1, F3, F4, F12, F13, F15, G1, G2, G14, G15,R1, R2, R14,R15, T1, T3, T4, T12, T13, T15,U5, U11, V4, V12, W4, W13, Y2, Y14, AA3, AA13

  VSS:
  A5, A11,B4, B8, B12, C5,C8, C11, D2, D6, D7, D9, D10, D14, E1, E3, E8, E13, E15, F2, F8, F14, G3, G5, G7, G9, G11, G13, H3,H4 H6, H8, H10, H12, J1,J3,J7,J8, J10, J11, J12,J15, K7, K8, K9, L1,L2, L3, L4, L5, L11,L12, L13, L14, L15, M7, M8, M9, N1, N3, N4, N6, N9,N9, N10, N12, N13, N15, P4, P6, P8, P10, P12, P13, R3, R5, R7, R9, R11, R13, T2, T8, T14, U1, U3, U8, U12, U15, V2, V6, V7, V9, V10, V14, W5, W8, W11, Y4, Y8, Y12, AA5, AA11.

16.3.2 315-ball 2CHx32 Discrete Package, 0.80mm x 0.70mm using MO- 338A

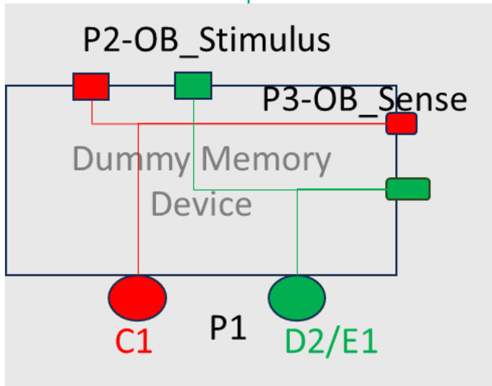
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	VDDQ	DMI0_A	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI1_A	VDDQ	NC	NC
B	NC	VDDQ	RDQS0_T_A	VSS	DQ4_A	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ12_A	VSS	RDQS1_T_A	VDDQ	NC
C	VDD1	DQ1_A	VDDQ	RDQS0_C_A	VSS	DQ5_A	VDD2H	VSS	VDD2H	DQ13_A	VSS	RDQS1_C_A	VDDQ	DQ9_A	VDD1
D	DQ0_A	VSS	DQ3_A	VDDQ	WCK0_C_A	VSS	VSS	VDD2H	VSS	VSS	WCK1_C_A	VDDQ	DQ11_A	VSS	DQ8_A
E	VSS	DQ2_A	VSS	WCK0_T_A	VDDQ	DQ6_A	VDD2H	VSS	VDD2H	DQ14_A	VDDQ	WCK1_T_A	VSS	DQ10_A	VSS
F	VDDQ	VSS	VDDQ	VDDQ	DQ7_A	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ15_A	VDDQ	VDDQ	VSS	VDDQ
G	VDDQ	VDDQ	VSS	CA0_A	VSS	CS1_A	VSS	CA2_A	VSS	CA4_A	VSS	CA6_A	VSS	VDDQ	VDDQ
H	Reset_N	VDD2L	VSS	VSS	CA1_A	VSS	CS0_A	VSS	CK_t_A	VSS	CA3_A	VSS	CA5_A	VDD2L	ZQ_A
J	VSS	VDD2L	VSS	RFU	VDD2H	RFU	VSS	VSS	CK_c_A	VSS	VDD2H	VSS	VSS	VDD2L	VSS
K	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
L	VSS	VSS	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VSS	VSS
M	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
N	VSS	VDD2L	VSS	VSS	VDD2H	VSS	CK_c_B	VSS	VSS	VSS	VDD2H	VSS	VSS	VDD2L	VSS
P	RFU	VDD2L	CA5_B	VSS	CA3_B	VSS	CK_t_B	VSS	CS0_B	VSS	CA1_B	VSS	VSS	VDD2L	RFU
R	VDDQ	VDDQ	VSS	CA6_B	VSS	CA4_B	VSS	CA2_B	VSS	CS1_B	VSS	CA0_B	VSS	VDDQ	VDDQ
T	VDDQ	VSS	VDDQ	VDDQ	DQ15_B	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ7_B	VDDQ	VDDQ	VSS	VDDQ
U	VSS	DQ10_B	VSS	WCK1_t_B	VDDQ	DQ14_B	VDD2H	VSS	VDD2H	DQ6_B	VDDQ	WCK0_T_B	VSS	DQ2_B	VSS
V	DQ8_B	VSS	DQ11_B	VDDQ	WCK1_c_B	VSS	VSS	VDD2H	VSS	VSS	WCK0_C_B	VDDQ	DQ3_B	VSS	DQ0_B
W	VDD1	DQ9_B	VDDQ	RDQS1_C_B	VSS	DQ13_B	VDD2H	VSS	VDD2H	DQ5_B	VSS	RDQS0_C_B	VDDQ	DQ1_B	VDD1
Y	NC	VDDQ	RDQS1_T_B	VSS	DQ12_B	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ4_B	VSS	RDQS0_T_B	VDDQ	NC
AA	NC	NC	VDDQ	DMI1_B	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI0_B	VDDQ	NC	NC

NOTE 1 0.8mm pitch (X-axis) 15 columns, 0.7mm pitch (Y-axis), 21 rows

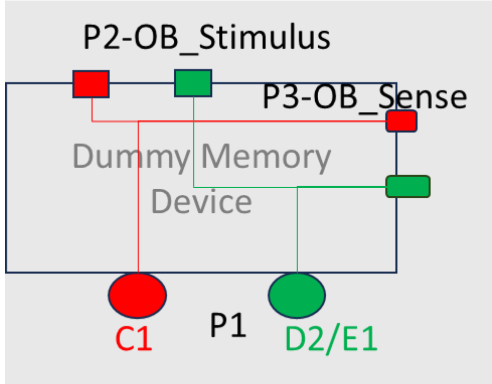
LPDDR5X.spim –VDD1-1

```
|*****************************************************************
| LPDDR5X_VDD.spim * IBIS 8.0 Model
| This SPIM of power rails in LPDDR5X is illustrating BIRD223.1.
| This Model is valid for Commercial Temperature Range 0C<=Tc<=95C
|
| Nominal R_VR and L_VR values at given VRM bandwidth, upon reference board.
|  Power Rail R_VR(Ohm)      L_VR(H)         VR Bandwidth(Hz)
| -----------       --------            --------            ---------------
|  VDD1        0.001e-3         0.001e-9        150e+3
|  VDD2L       0.001e-3         0.001e-9        150e+3
|
|*****************************************************************
|
[IBIS Ver]    8.0
[File Name]   LPDDR5X_VDD.spim
[Date]        02/12/2024
[File Rev]    1.0
[Source]      From Intel Corporation
```

```
[Device SPIM]  LPDDR5X
[Manufacturer]                    ABC Corporation
[Description]   Streamlined Power Integrity Model, Golden Example
|
[SPIM Rail] VDD1
[SPIM Pin Cluster] VSS
|Pin_cluster_name                 Pin_name_List
|
VDD1_01                           C1
VSS_VDD1_01                       D2 E1

VDD1_02                           C15
VSS_VDD1_02                       D14 E15

VDD1_03                           W1
VSS_VDD1_03                       U1 V2

VDD1_04                           W15
VSS_VDD1_04                       V14 U15
|
[END SPIM Pin Cluster]
```



LPDDR5X.spim –VDD1-2



SPIM_LP5x_VDD1.s12p

SPIM is scalable to handle from PKG-less, to actual PKG routing which will result in more actual PI design, considering inaction between PKG & PCB.

[SPIM Port List]

Port# Terminal_p	Terminal_n
1 VDD1_01	VSS_VDD1_01
2 VDD1_02	VSS_VDD1_02
3 VDD1_03	VSS_VDD1_03
4 VDD1_04	VSS_VDD1_04
5 OB_Stimulus_01_p	OB_Stimulus_01_n
6 OB_Stimulus_02_p	OB_Stimulus_02_n
7 OB_Stimulus_03_p	OB_Stimulus_03_n
8 OB_Stimulus_04_p	OB_Stimulus_04_n
9 OB_Sense_01_p	OB_Sense_01_n
10 OB_Sense_02_p	OB_Sense_02_n
11 OB_Sense_03_p	OB_Sense_03_n
12 OB_Sense_04_p	OB_Sense_04_n

[End SPIM Port List]

[SPIM Touchstone File]
| file_type file_reference
File_TS SPIM_LP5x_VDD1.s12p

[SPIM Stimulus]

OB_Stimulus_Port	Weighting
OB_Stimulus_01	1/4
OB_Stimulus_02	1/4
OB_Stimulus_03	1/4
OB_Stimulus_04	1/4

[End SPIM Stimulus]

[SPIM Target]

[SPIM Observation Port] OB_Sense_01

Z(Frequency)	Z(typ)	Z(min)	Z(max)
1000000	0.05	NA	NA
10000000	0.05	NA	NA
10100000	0.085	NA	NA
10000000	0.085	NA	NA

|

[SPIM Observation Port] OB_Sense_02

Z(Frequency)	Z(typ)	Z(min)	Z(max)
1000000	0.05	NA	NA
10000000	0.05	NA	NA
10100000	0.085	NA	NA
10000000	0.085	NA	NA

|

[SPIM Observation Port] OB_Sense_03

Z(Frequency)	Z(typ)	Z(min)Z(max)	
1000000	0.05	NA	NA
10000000	0.05	NA	NA
10100000	0.085	NA	NA
10000000	0.085	NA	NA

|

[SPIM Observation Port] OB_Sense_04

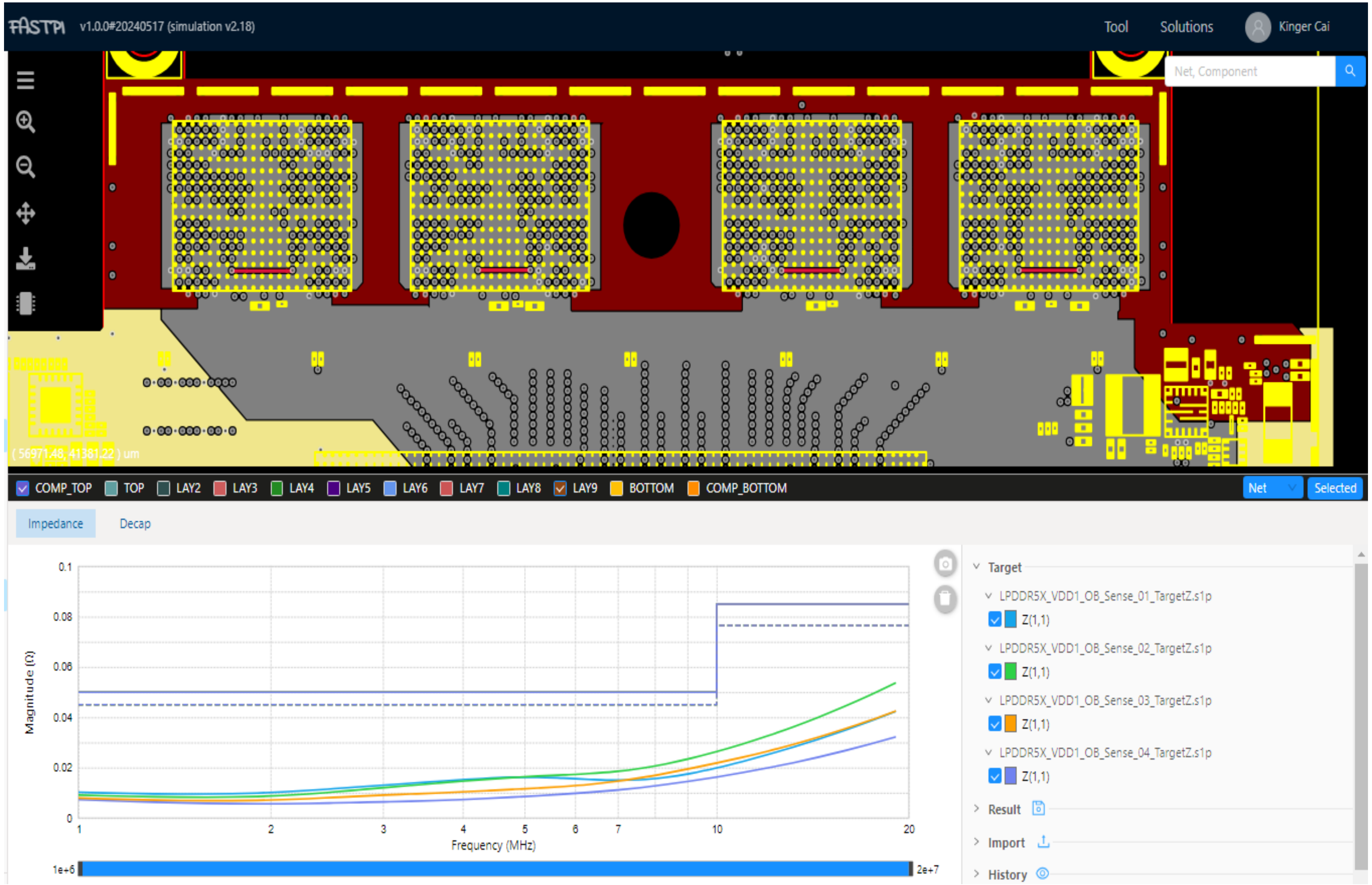
Z(Frequency)	Z(typ)	Z(min)	Z(max)
1000000	0.05	NA	NA
10000000	0.05	NA	NA
10100000	0.085	NA	NA
10000000	0.085	NA	NA

|

[End SPIM Target]
[END SPIM Touchstone File]

LPDDR5X.spim Supports PDN Review and Sign-off

- Per JEDEC Spec, PDN PI design sign-off is only required to satisfy the impedance target up to 20MHz in FD, for all 4 major power rails.
- There is no requirements to meet certain PI design requirements from transient simulation.
- There is neither loading current profiles required to be shared from memory vendors, nor Vpp targets required to satisfy.



Takeaways

- **Fundamental Principle** – PI/PD design starts from $\mathbf{V = Z \times I}$.
- **Platform-Level PI** – Optimize PDN routing and decoupling across die, package, PCB, and VRM for PPA
- **PDN Characteristics** – Once designed, $\mathbf{Z}$ is fixed; loading $\mathbf{I}$ and output $\mathbf{V}$ are varying during operation.
- **Z Target** – If a PDN meets transient requirements, its $\mathbf{Z}$ profile can serve as $\mathbf{Ztarget}$.
- **Chip-level PI** – define PI targets before package sign-off, upon a reference board design.
- **Correlation** – Meeting $\mathbf{Ztarget}$ ensures transient targets are met, both theoretically and practically.
- **Board-Level PI** – Design to keep board PDN impedance below $\mathbf{Ztarget}$ in frequency domain.
- **Reality** – On-die transient currents are rarely shared by chip vendors, same situation for IBIS, for IP protection.
- **Power DC**– always a must, to meet current, current density, and IR drop specifications.
- **Industry Standard** – JEDEC supports board-level sign-off based on impedance targets.

Thank You!

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