2025 IEEE INTERNATIONAL SYMPOSIUM ON ELECTROMAGNETIC COMPATIBILITY, SIGNAL & POWER INTEGRITY

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Bridging EMF with Circuit Simulation

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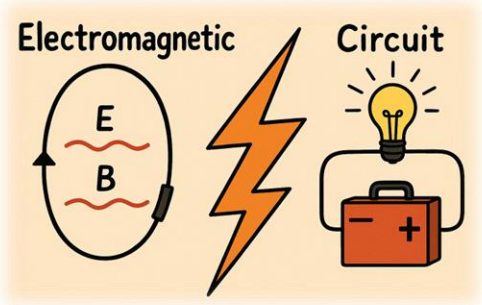
arm

Hybrid IBIS Summit at IEEE
EMC+SIPI 2025
Raleigh, North Carolina
August 22, 2025

Bridging EMF with Circuit Simulation

- Electromagnetic Field = EMF
- Kirchhoff's Law
- S-element in netlist



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An SAE Industry Technologies Consortia Program

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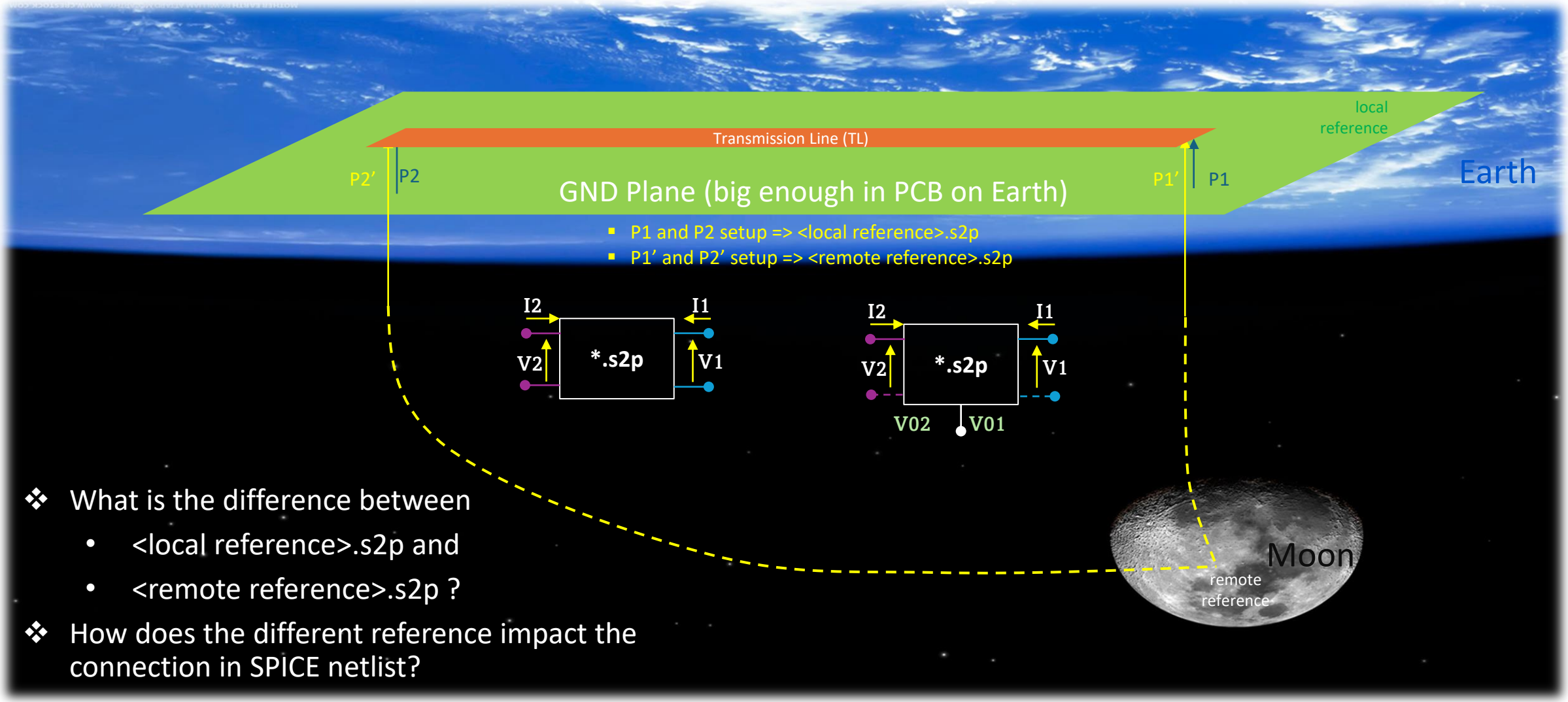
Problem Statement & Goal

- S-parameter models are widely used in Signal Integrity (SI) & Power Integrity (PI) analysis. The confusion is often arisen on how to correctly connect S-parameter models in SPICE netlists, typically due to the insufficient understanding of electromagnetic field (EMF) principles or port setups during S-parameter models extraction.
  - Can a port be set up with the reference point on the Moon, for a transmission line (TL) with GND reference plane on the Earth? What is the difference than the reference point on GND plane in adjacent layer(s) in the same PCB stackup on the Earth?
  - If so, how to make the connection with a lumped component, such as a capacitor with the S-parameter model of a TL with the reference point on the Moon?
- The goal of this presentation is to
  - Bridge EMF with Circuit from 1st principle.
  - Principles of EMF and Circuit
  - S-parameter port setup and implications
    - TL vs. Waveguide
    - Global reference vs. Local reference
  - Case study
  - Takeaway

Maxwell's Equations

Differential form	Integral form
$\vec{\nabla}\cdot\vec{E}=\rho\frac{\rho}{\varepsilon_0}$	$\vec{\emptyset}\cdot\vec{\nabla}=d\bar{A}=\int_S^{\tilde{}} d\vec{A}\,\frac{Q_{enc}}{\varepsilon_0}$
$\vec{\nabla}\cdot\vec{B}=0$	$\vec{\emptyset}\times\vec{E}=-\frac{\partial B}{\partial t}=-\frac{d}{dt}\int\vec{S}_B\frac{dA}{dA}$
$\vec{\nabla}\times\vec{E}=-\frac{\partial B}{\partial t}$	$\vec{\emptyset}\times\vec{B}=\bar{\mu}_0+\mu\frac{\bar{E}}{\varepsilon_0}\int_S^{\tilde{}}\mu_0\vec{I}_{nc}+\frac{I_{enc}}{\partial E}$
$\vec{\nabla}\times\vec{B}=\mu_0 J+\mu_0\frac{\partial E}{\partial t}$	$\vec{\emptyset}\cdot\vec{B}=\mu_0\frac{I_{enc}}{\varepsilon_S}+\frac{\mu_0 I_{enc}}{\mu_0\varepsilon E}d\frac{d\partial}{\partial t}$

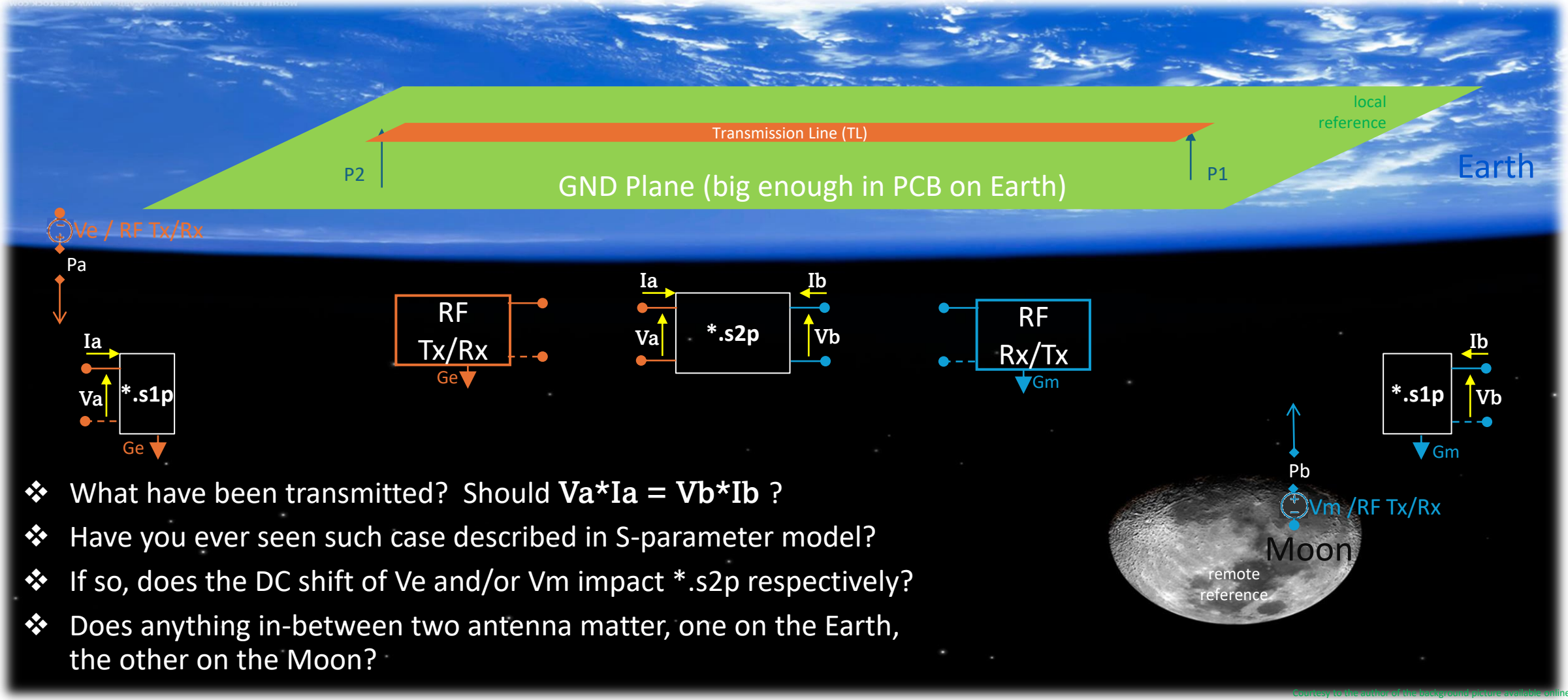
Port setup with Different Reference Points for TL



- What is the difference between
  - <local reference>.s2p and
  - <remote reference>.s2p ?
- How does the different reference impact the connection in SPICE netlist?

S-element .snp has connections of 2N, or N+1 terminals, possible N terminals, never of 2N+1 terminals.

Port setup with Different Reference Points for Antenna



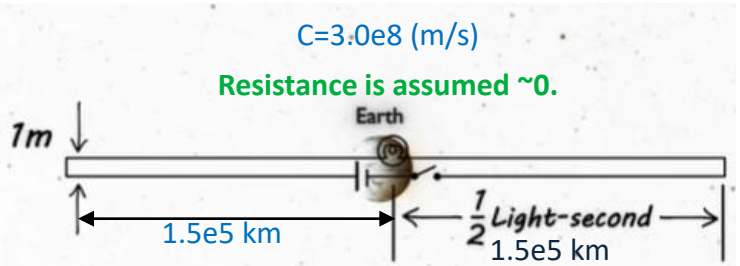
- What have been transmitted? Should **Va*Ia = Vb*Ib** ?
- Have you ever seen such case described in S-parameter model?
- If so, does the DC shift of Ve and/or Vm impact *.s2p respectively?
- Does anything in-between two antenna matter, one on the Earth, the other on the Moon?

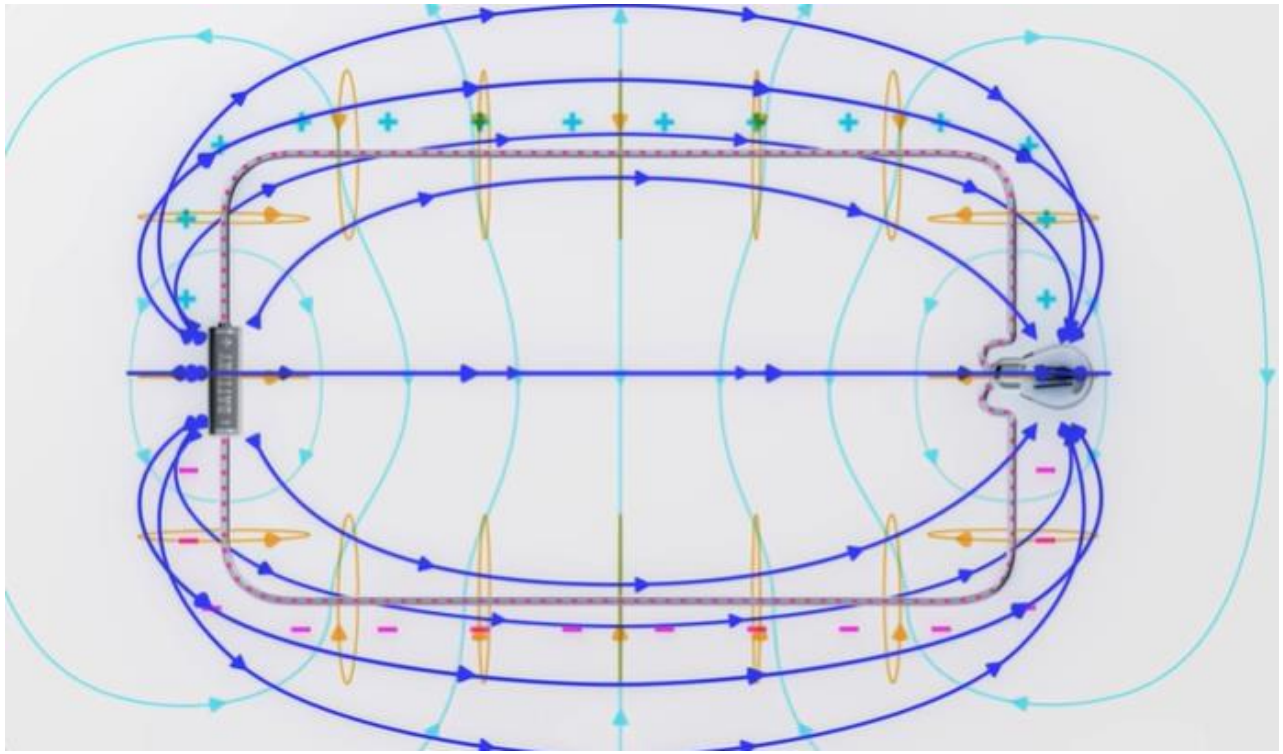
Courtesy to the author of the background picture available online.

S-element .snp has connections of 2N or N+1 terminals, possible N terminals, never of 2N+1 terminals.

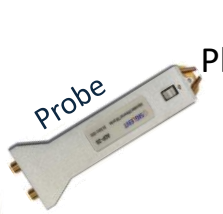
The Big Misconception About Electricity

A) 0.5 s
B) 1 s
C) 2 s
D) 1/c s
E) None of the above





- Electromagnetic waves, Poynting vector
- https://youtu.be/bHIhgxav9LY



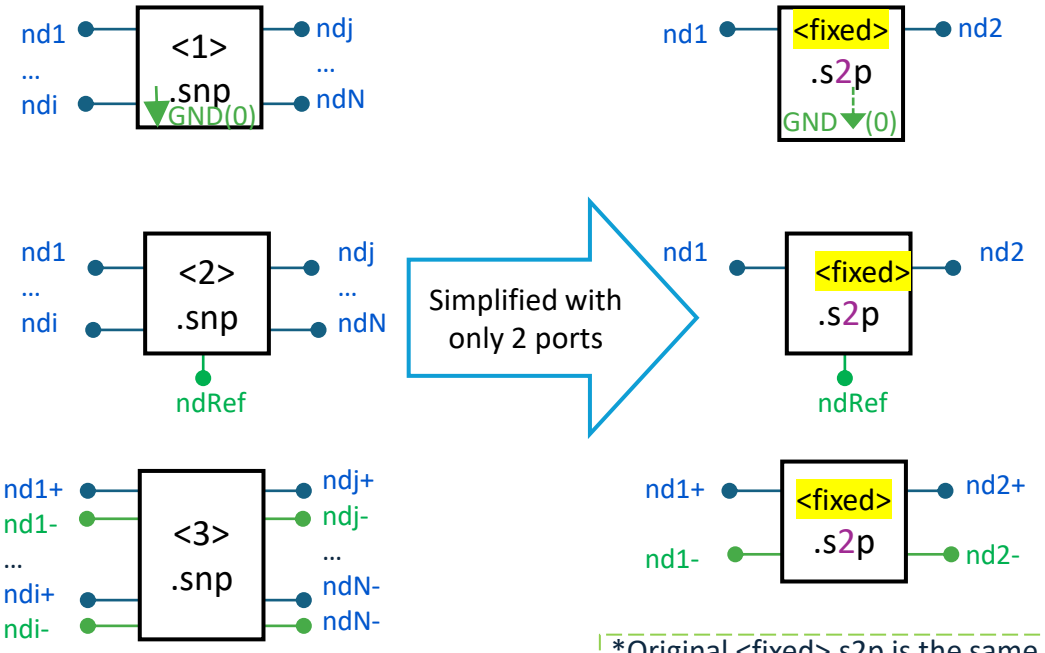
If **Pa** set up as “Open”,

What is measured at **Pb**? “Open” as well?

Courtesy to the authors of the pictures available online, used in this slides set.

S-element Syntax: Brief of 3 Connections

- Note that "GND", "0", and "ground" are reserved words in HSPICE, and refer to the universal or ideal node which is required in any HSPICE netlist.
- IBIS-ISS copies this language, so we need to be able to support all three options in any structures in IBIS, including IBIS-ISS, EMD, and IBIS Interconnect.
- The problem is that IBIS Interconnect and EMD keywords support having only one reference node per circuit, so at least one of these S-element connections is illegal in IBIS today. --- Michael Mirmak



Only N, N+1 and 2N terminals are legal for .snp in HSPICE netlist.

*Original <fixed>.s2p is the same in 3 different netlist connections.

So does the setup for S-parameter extraction from physical structure.

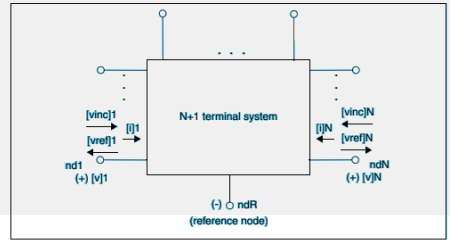
S-element Syntax

Use the following S-element syntax to show the connections within a circuit:

```
Sxxx nd1 nd2 ... ndN ndRef
+ [ENFORCE_PASSIVE=0|1]
+ [MNAME=Smodel_name] [FQMODEL=sp_model_name]
+ [TYPE=[s|y]] [Z0=[value| vector_value]]
+ [FBASE = base_frequency] [FMAX=maximum_frequency]
+ [PRECFAC=val] [DELAYHANDLE=[1|2|0|ON|OFF]]
+ [DELAYFREQ=val]
+ [INTERPOLATION=STEP|LINEAR|SPLINE|HYBRID]
+ [INTDATTYP=[RI|MA|DBA]] [HIGHPASS=[0|1|2|3|4]]
+ [LOWPASS=[0|1|2]3] [MIXEDMODE=[0|1]]
+ [DATATYPE=data_string] [XLINELENGTH=val]
+ [NOISE=[1|0]] [NoiPassiveChk=1|0] [DTEMP=val]
+ [PASSIVE=[0|1]] [PASSIVE_TOL=val] [COLSUM_LIMIT=val]
+ [RATIONAL_FUNC=[0|1|2]] [RATIONAL_FUNC_REUSE=[0|1]]
+ [RATIONAL_FUNC_WINDOWING=[0|1]]
+ [RATIONAL_FUNC_FOR_AC=0|1]
+ [STAMP=[S|Y|YSTS|SSTS|DEEMBED|AUTO]] [M=int]
+ [SMOOTH=val] [SMOOTHPTS=val]
+ [RATIONAL_FUNC_CACHE_DIR = dir_str]
+ [CACHE_DIR = path]
+ [CAUSALITY=[0|1]]
+ [CAUSALITY_FMAX_SCALE = val]
+ [WRITE_CAUSALITY_ENFORCED_FILE = [0|1]]
+ [CAUSALITY_ENFORCED_FILE_NAME = file_name]
```

HSPICE® Signal Integrity User Guide
Version A-2007.12, December 2007

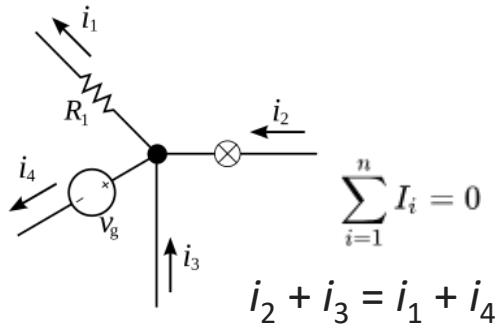
Figure 17 Terminal Node Notation



Parameter	Description
nd1 nd2...ndN	Nodes of an S-element (see Figure 1) and S-element Example. Three kinds of definitions are present: • With no reference node ndRef, the default reference node is GND. Each node ndi (i=1~N) and GND construct one of the N ports of the S-element. • Defines ndRef with one reference node. Each node ndi (i=1~N) and the ndRef construct one of the N ports of the S-element. • With an N reference node, each port has its own reference node. You can write the node definition in a clearer way as: nd1+ nd1- nd2+ nd2- ... ndN+ ndN- Each pair of the nodes (ndi+ and ndi-, i=1~N) constructs one of the N ports of the S-element.
ndRef	Reference node

Kirchhoff's Laws

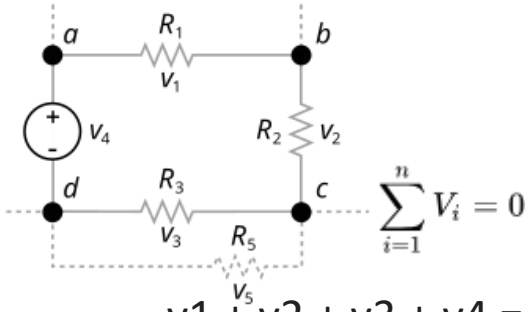
- KCL
  - The sum of all the current entering and existing a node must equal to zero.
  - Derivation of Kirchhoff's current law
  - Kirchhoff's Current law from Maxwell's equation (youtube)



$i_2 + i_3 = i_1 + i_4$

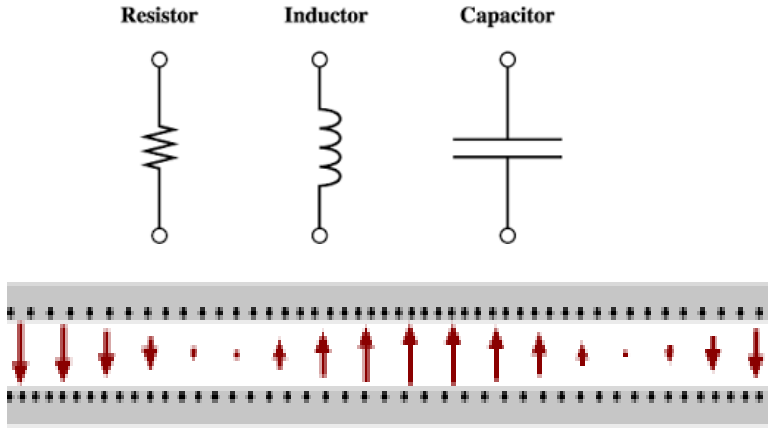
- KVL
  - The sum of all the voltages around a loop is equal to zero.
  - Derivation of Kirchhoff's voltage law

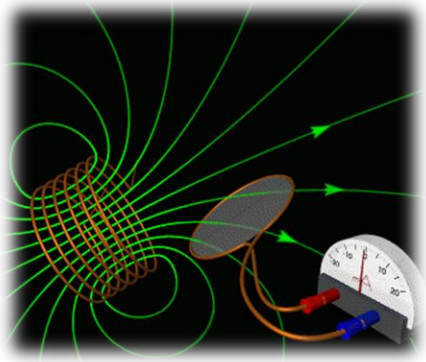
$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} = \mathbf{0} \qquad \sum_i V_i = -\sum_i \int_{\mathcal{P}_i} \mathbf{E} \cdot \mathrm{d}\mathbf{l} = \oint \mathbf{E} \cdot \mathrm{d}\mathbf{l} = 0 \qquad V_{a\to b} = -\int_{\mathcal{P}_{a\to b}} \mathbf{E} \cdot \mathrm{d}\mathbf{l}$$



v1 + v2 + v3 + v4 = 0

- Limitations
  - Started for Lumped-element models
  - In a TL, the net charge in different parts of the conductor changes with time. In the direct physical sense, this violates KCL.
  - The induced electric field, produced by an inductor with time-varying magnetic fields, neither confined nor negligible, violates KVL.

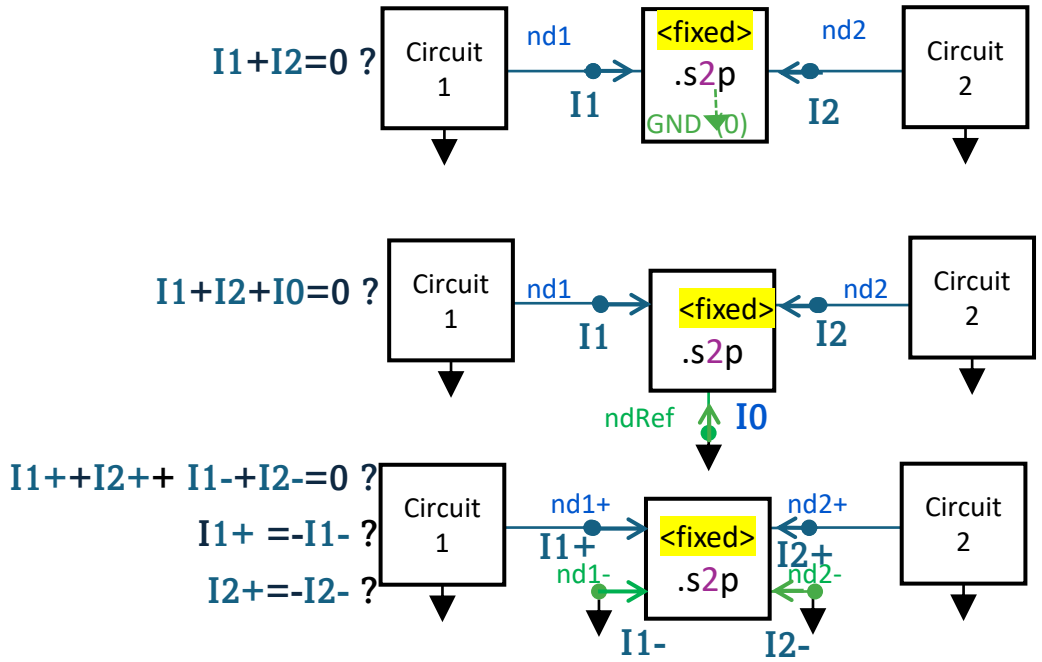




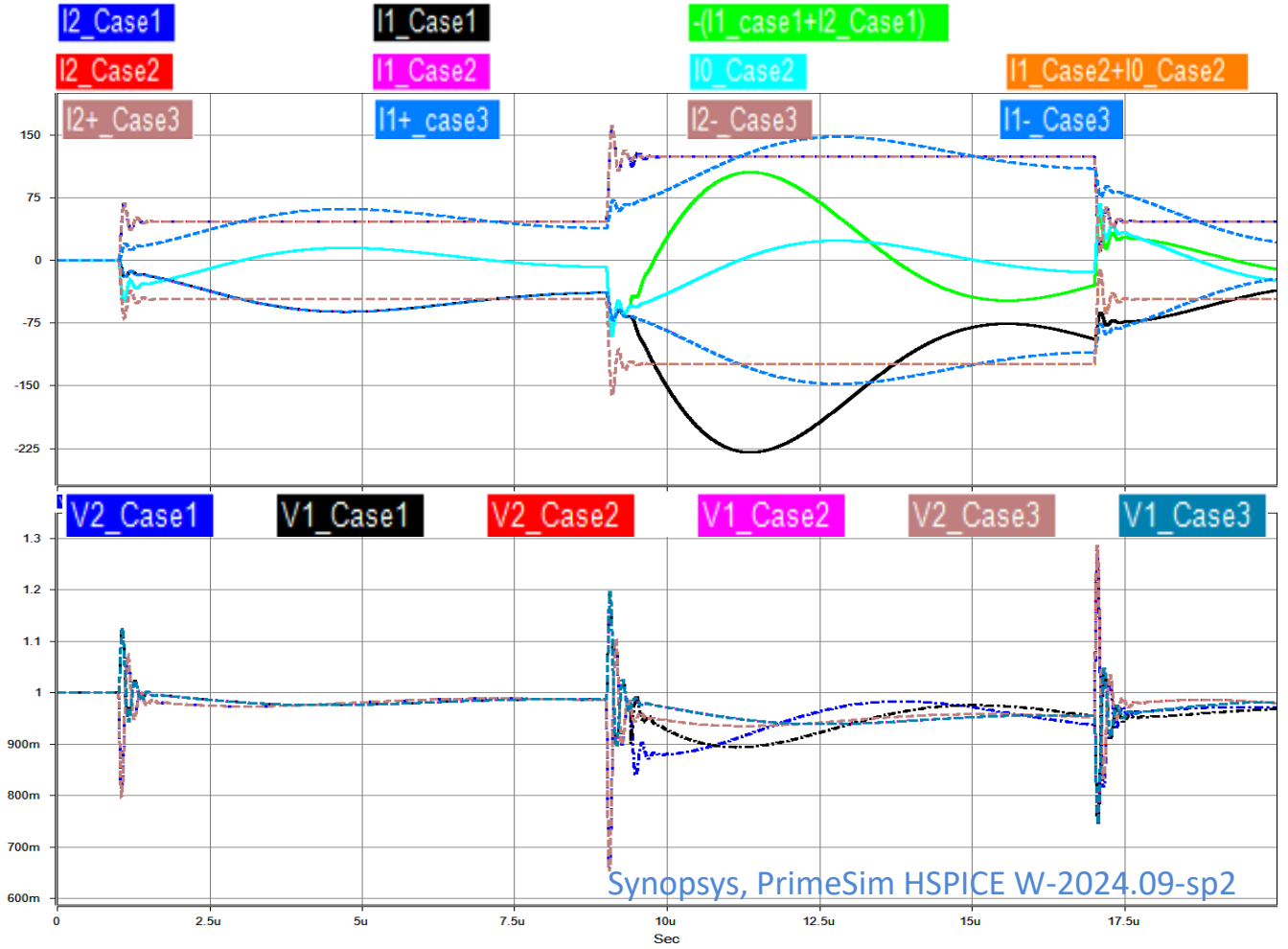
S-element Syntax: KCL Analysis

Does KCL $\sum_{i=1}^{n} I_i = 0$ holds in 3 various connections?

1. I1+I2=0 ? (No) --- Shall this connection not be recommended?
2. I1 I2+I0=0 ? (Yes)
3. I1++I2++ I1-+I2-=0 ?; I1+ =-I1- ?; I2+=-I2- ? (Yes)

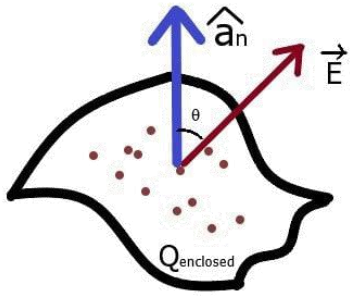


<fixed>.s2p is a PDN with Decoupling capacitors stuffed.



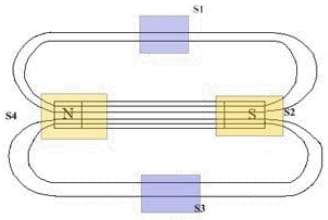
- I2 is a loading, keeps unchanged. So does V2.
- I1 in Case_1 varies from that in Case_2/3.
- V1 in Case_1 varies from that in Case_2/3.
- Case_2 and Case3 are identical, with I0=I1-+I2-.

Maxwell Equations, and EMF in Particular Structures



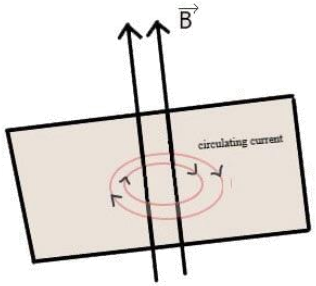
$\nabla \cdot \mathbf{E} = \rho / \varepsilon_0$

Gauss Law of Electricity



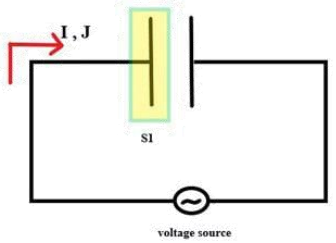
$\nabla \cdot \mathbf{B} = 0$

Gauss Law of Magnetism



$\nabla \times \mathbf{E} = -\partial \mathbf{B} / \partial t$

Faraday's Law of Induction



$\nabla \times \mathbf{B} = \mu_0 \mathbf{J} + \mu_0 \varepsilon_0 \partial \mathbf{E} / \partial t$

Ampere's Law

Given $Z_{C1}=Z_{C2}=Z_0$

$V_{i1}= \frac{1}{2} [V_1+I_1(Z_0)]$

$V_{r1}= \frac{1}{2} [V_1-I_1(Z_0)]$

$I_{i1}= \frac{1}{2} [V_1+I_1(Z_0)]/Z_0$

$I_{r1}= \frac{1}{2} [V_1-I_1(Z_0)]/Z_0$

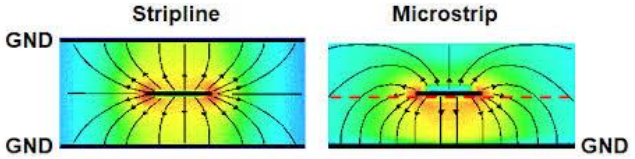
$I_1= -I_2=I$ (Not always true)

$V_{i2}= \frac{1}{2} [V_2+I_2(Z_0)]$

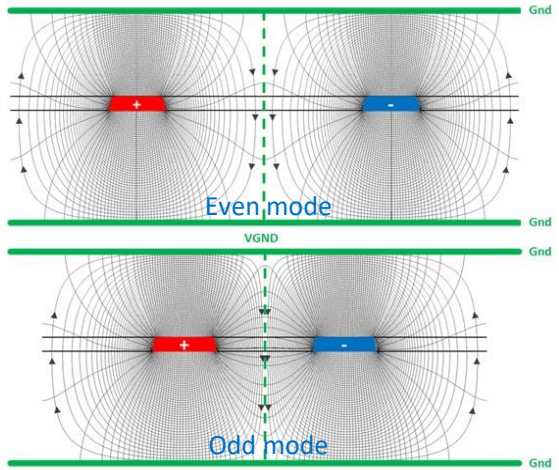
$V_{r2}= \frac{1}{2} [V_2-I_2(Z_0)]$

$I_{i2}= \frac{1}{2} [V_2+I_2(Z_0)]/Z_0$

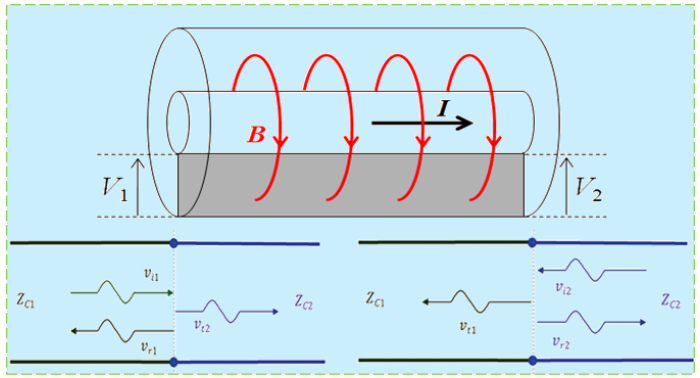
$I_{r2}= \frac{1}{2} [V_2-I_2(Z_0)]/Z_0$



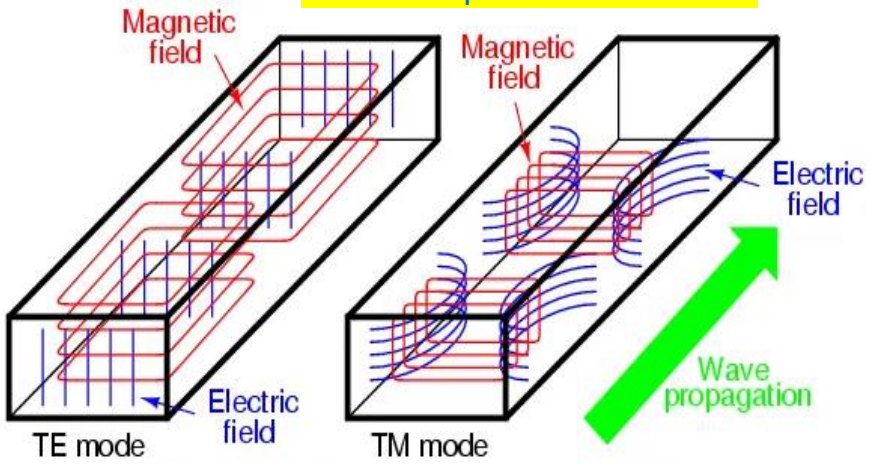
EMF is fundamental for power propagation!



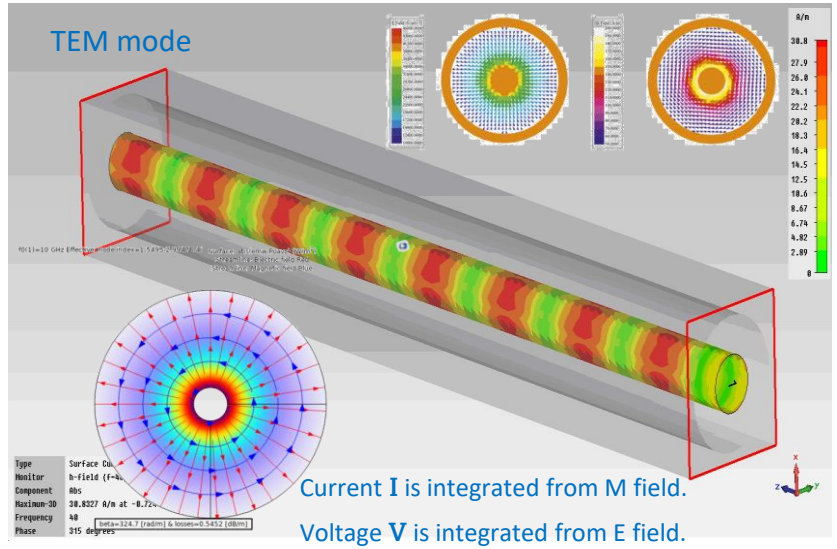
V and **I** are derived/integrated from EMF!



Current **I** and **V** is arbitrary, without separated conductors



Magnetic flux lines appear as continuous loops
Electric flux lines appear with beginning and end points



Current **I** is integrated from M field.

Voltage **V** is integrated from E field.

Courtesy to the authors of the pictures available online, used in this slides set.

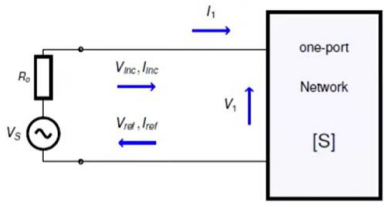
S-parameter vs. V and I, https://www.youtube.com/watch?v=EXdNOORhWco

Power / Normalize Wave of S-Parameters — Simple to Understand

Instantaneous one-port terminal voltage & current are related to the incident & reflected voltage & current components by

$$V_1 = V_{inc} + V_{ref}$$

$$I_1 = I_{inc} - I_{ref}$$



Considers the case of a transmission line system having a real characteristic impedance, *Zo*, then the incident and reflected components are related to this characteristic impedance by:

$$\frac{V_{inc}}{I_{inc}} = \frac{V_{ref}}{I_{ref}} = Z_o$$

Power / Normalize Wave of S-Parameters — Simple to Understa

$$V_1 = V_{inc} + V_{ref} \qquad I_1 = I_{inc} - I_{ref} \qquad \frac{V_{inc}}{I_{inc}} = \frac{V_{ref}}{I_{ref}} = Z_o$$

$$V_1 = V_{inc} + I_{ref} Z_o$$
$$= V_{inc} + (I_{inc} - I_1) Z_o$$
$$= V_{inc} + I_{inc}(Z_o) - I_1(Z_o)$$
$$= V_{inc} + V_{inc} - I_1(Z_o)$$
$$2V_{inc} = V_1 + I_1(Z_o)$$
$$V_{inc} = \frac{1}{2}[V_1 + I_1(Z_o)]$$

$$V_{ref} = V_1 - V_{inc}$$
$$V_{ref} = V_1 - \frac{1}{2}[V_1 + I_1(Z_o)]$$
$$V_{ref} = \frac{1}{2}[V_1 - I_1(Z_o)]$$
$$I_{inc} = \frac{V_{inc}}{Z_o} = \frac{1}{2Z_o}[V_1 + I_1(Z_o)]$$
$$I_{ref} = \frac{V_{ref}}{Z_o} = \frac{1}{2Z_o}[V_1 - I_1(Z_o)]$$

Power / Normalize Wave of S-Parameters — Simple to Understa

$$V_{inc} = \frac{1}{2}[V_1 + I_1(Z_o)] \qquad I_{inc} = \frac{V_{inc}}{Z_o} = \frac{1}{2Z_o}[V_1 + I_1(Z_o)]$$

$$V_{ref} = \frac{1}{2}[V_1 - I_1(Z_o)] \qquad I_{ref} = \frac{V_{ref}}{Z_o} = \frac{1}{2Z_o}[V_1 - I_1(Z_o)]$$

Power waves are normalized versions of voltage and current waves

$$a_n = \frac{V_{inc}}{\sqrt{Z_o}} \qquad b_n = \frac{V_{ref}}{\sqrt{Z_o}}$$

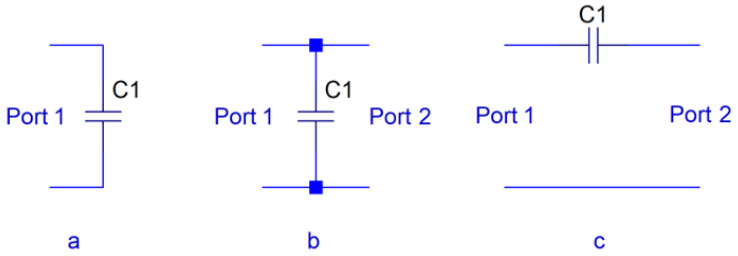
$$P = \frac{V_{inc}^2}{Z_o} = |a_n|^2$$

$$s = \frac{a}{b}$$

$a_n = ½ [V_n/\sqrt{Z_0} + I_n \sqrt{Z_0}]$

$b_n = ½ [V_n/\sqrt{Z_0} - I_n \sqrt{Z_0}]$

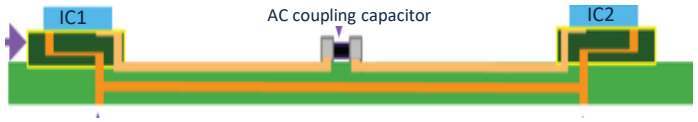
For *.s1p, only **V1** and **I1** **KVL/KCL variables** are defined, different concepts from **V**inc/**V**ref & **I**inc/**I**ref, or from **b**n and **b**n.



a) Capacitor in PDN

b) Capacitor in PDN

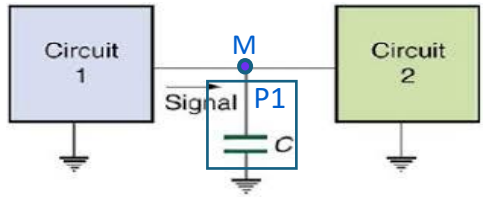
c) Capacitor in SI channel PCIe



Only Cap model-c applicable

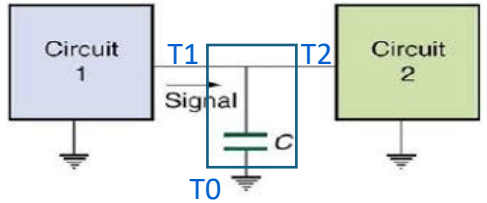
a—The capacitor connects to the IC using a VCC plane.

All Cap model-a/b/c applicable



1) √ KCL@M

2) √ KCL@M



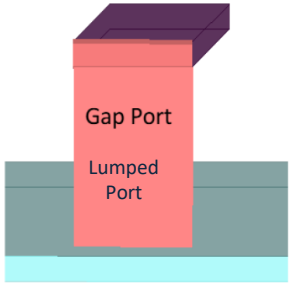
1) x KCL@ s2p

2) √ KCL@ s2p

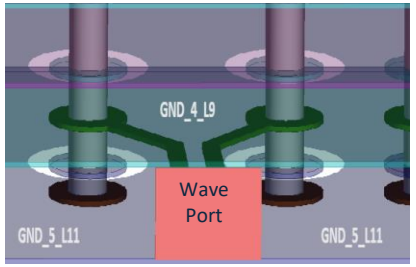
1)N terminals vs. 2)N+1 terminals

Port Setup for S -parameter Extraction for SI, and PI Analysis

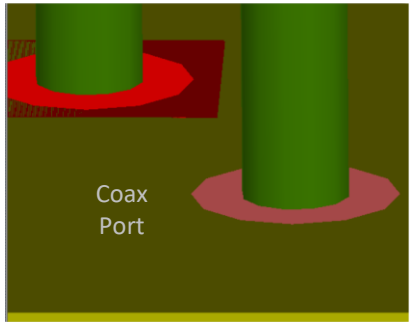
- Starts from one Transmission line aka single-ended, differential, SL, & ML
- Lumped(/Gap/Edge) port, Wave(/Edge) port, Coax(/Gap) port, Circuit Port, Waveguide port (Driven Modal)



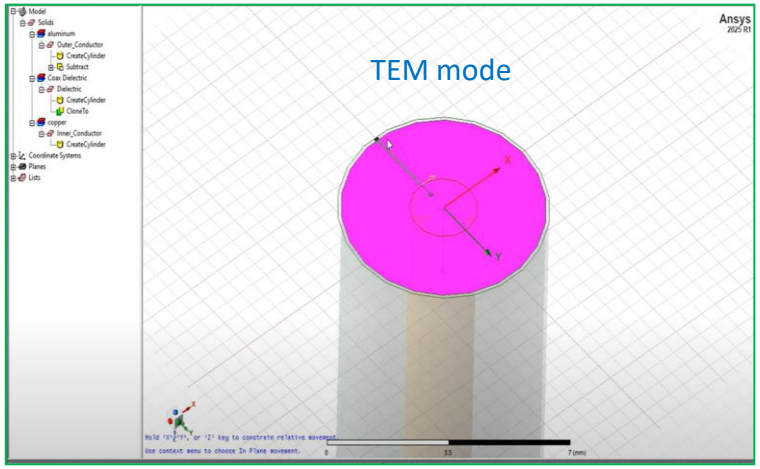
Driven terminal (Gap only), or Driven modal (no terminals) Lump (Gap) port setup anywhere. Not suitable for SL, wave port instead.



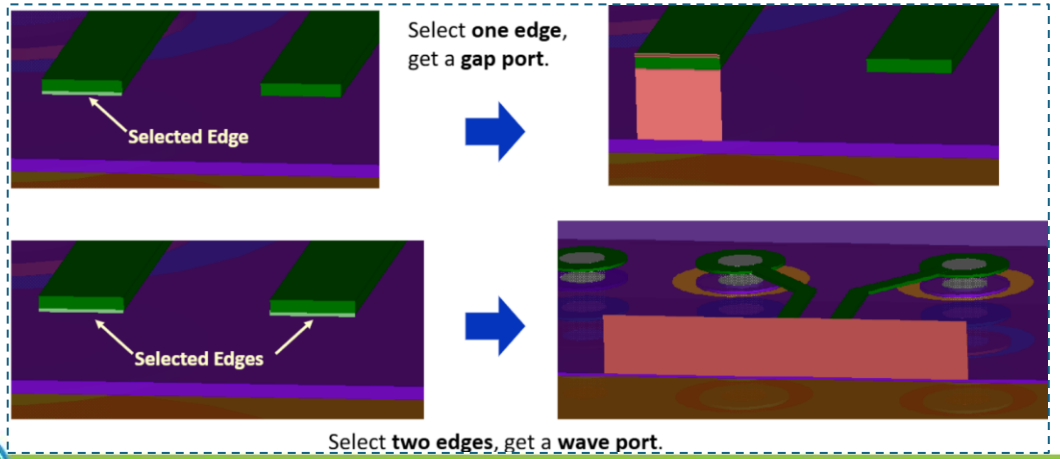
Waveport good for both MS & SL, has reference planes, extent factors, at structure edge, not on the extents, many excitation terminals, backed by PEC, Deembedding (negative/positive).

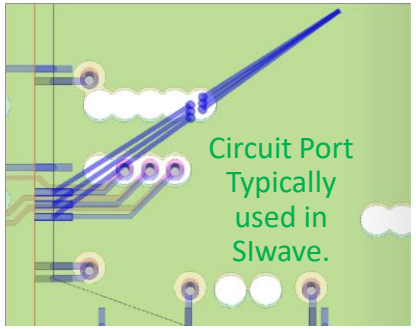


BGA antipad with existing GND layer or extend to create a coax structure.

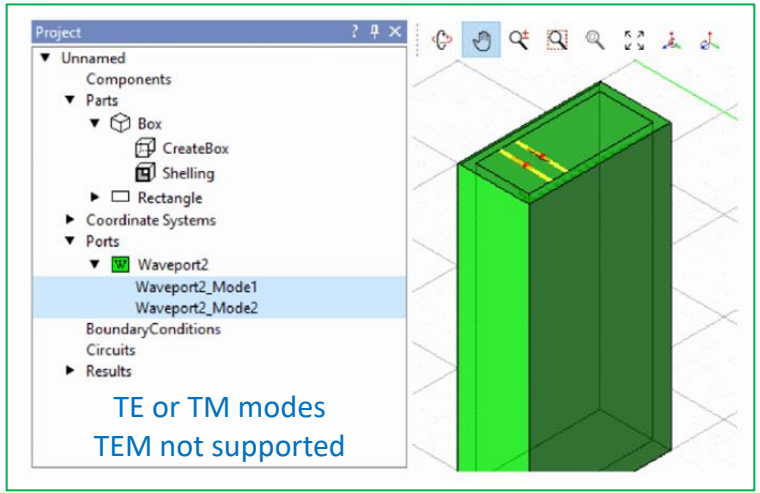


Driven Terminal is **V I** based, while Driven Modal **Power** based. **P=V*I**.





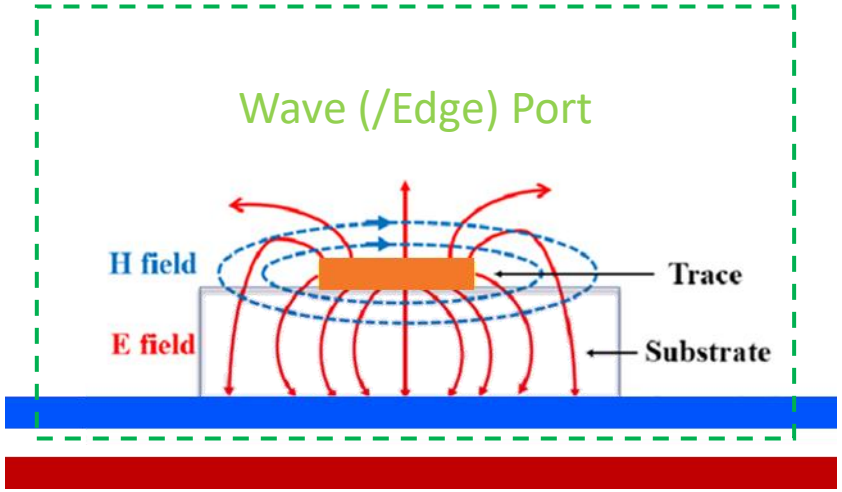
Circuit port set up between points without constraints, penetrate through GND plane.

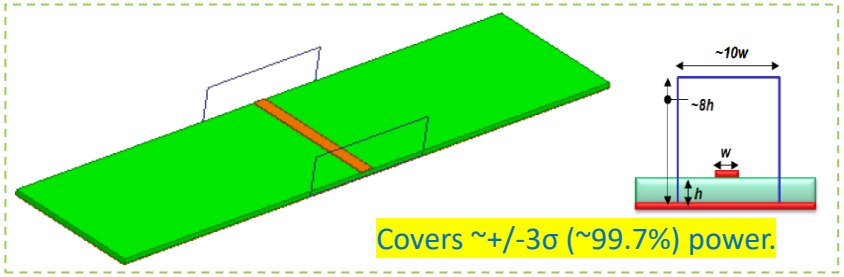


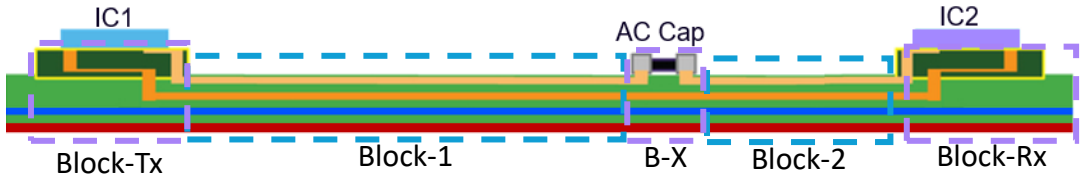
Courtesy to the authors of the pictures available online, used in this slides set.

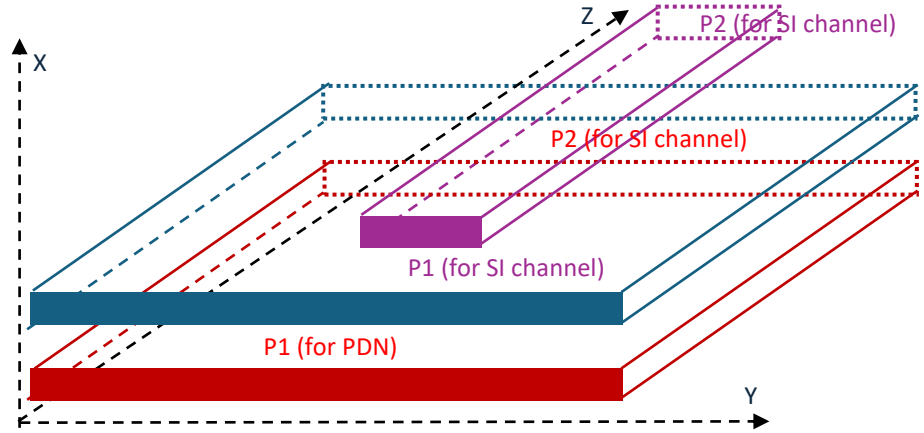
Typical Routing TL & PDN, with 2-port Setup for Separated SI/PI Models

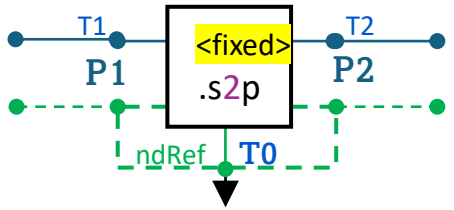
- PCIe SI channel, differential TL, with AC coupling capacitors
- Starts from 2-port setup for single-ended TL, for segmented blocks, being cascaded in SPICE
- Similar 2-port setup applicable for individual power delivery network (PDN)

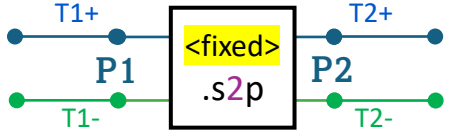












Typical Routing TL & PDN, with 4-port Setup for Merged SI/PI Model

- In modern platform electrical modeling, local reference has been used in setting ports in both SI channel and PDN S parameter modeling, to more accurately reflect the reference variations.
- For S-element, with local reference setup, connection (b) is recommended to use in netlists, reduces to connection (a), if all ports are set up with same global reference, as equal potential.

```
| Port_1 Terminal definition
VCC3_1     AK1
VSS_VCC3_1  AM1 AM4 AK4
| Port_2
VCC3_2     BY39 BV39 BW40
VSS_VCC3_2  CB41 BY41 BP41 BY42 BY44 BT44
|Port_3
VCC3_3     AC10 AE10 AB12
VSS_VCC3_3  AB8 AD8 AF8
|Port_4
VCC3_4     AK2
VSS_VCC3_4  AM1 AM2 AM4
|
...
| ...
```

- Not all GND pins are used as GND reference in ports set up.
- Each port has local its own GND reference, for more accuracy.
- It may hold true for both SI channel and PDN S-pm modeling.

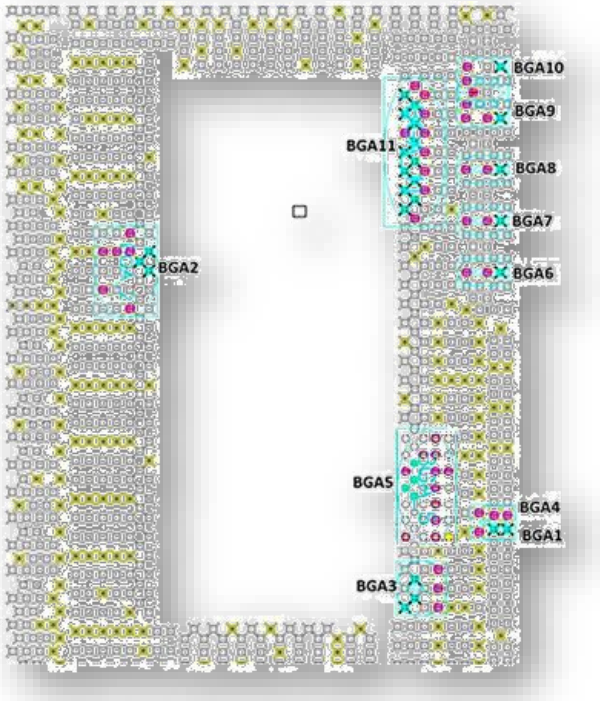
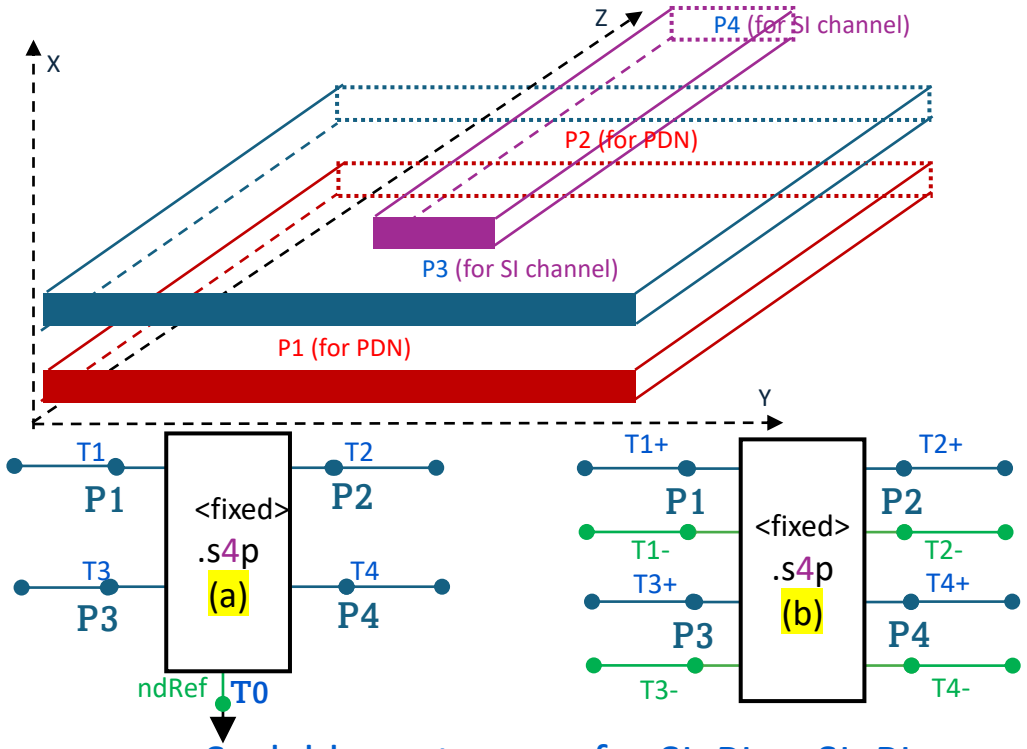


Figure 60 – Example Clusters at Pin Level, *in BIRD223.1*



Scalable up to .snp, for SI, PI or SI+PI.

Case Study-1: Netlist Connection of W-element, and/or S-element

2N-port S-parameters representing connectors

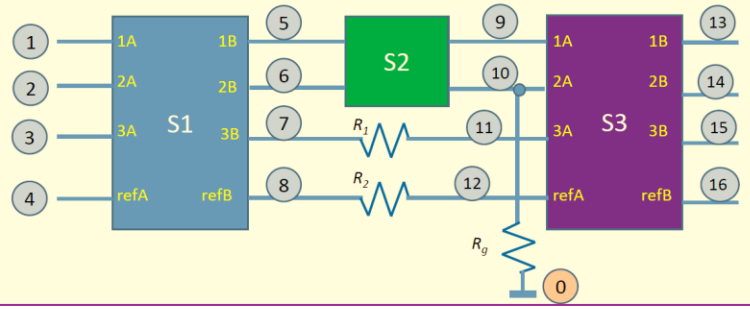
Subcircuits, S Parameters, and T line Models: Why and How We Set References

Vladimir Dmitriev Zdorov, DesignCon IBIS Summit, Santa Clara, California, February 02, 2018

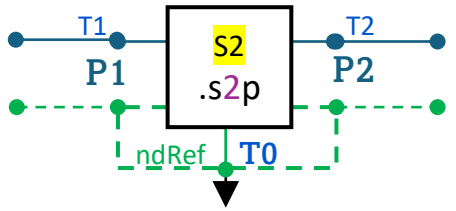
Nestlisting S-parameters describing connectors: use one reference terminal for each "side":

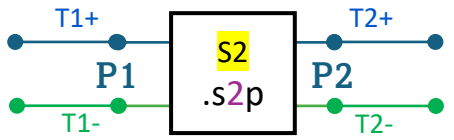
```
S1 1 4 2 4 3 4 5 8 6 8 7 8 mname = SmodelS1 *6-port model with 8 terminals
S3 9 12 10 12 11 12 13 16 14 16 15 16 mname = SmodelS3 *6-port model with 8 terminals

S2 5 6 9 10 mname = SmodelS2 *2-port model with 4 terminals
R1 7 11 20
R2 8 12 10
RG 10 0 1E6
* Need to continue: define what's to the left of S1 and to the right of S3
```

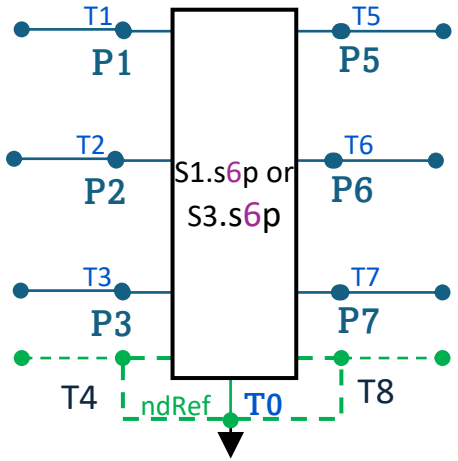
Shall S1/S2/S3 be connected differently?

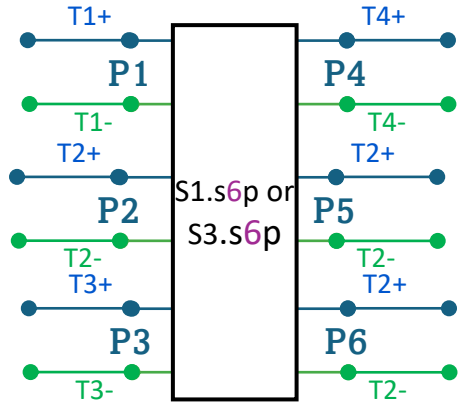


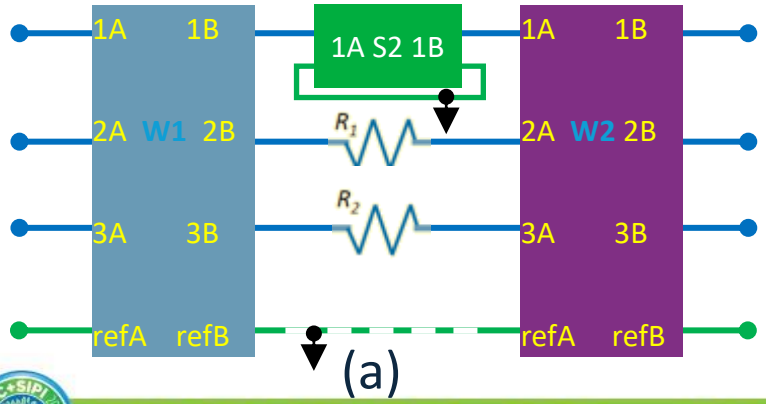
14

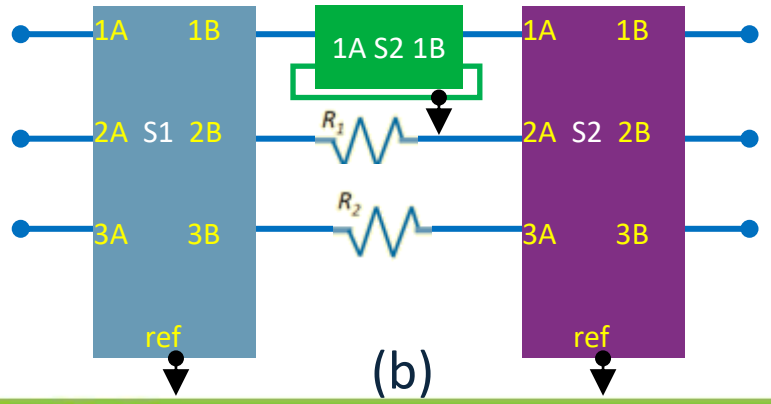


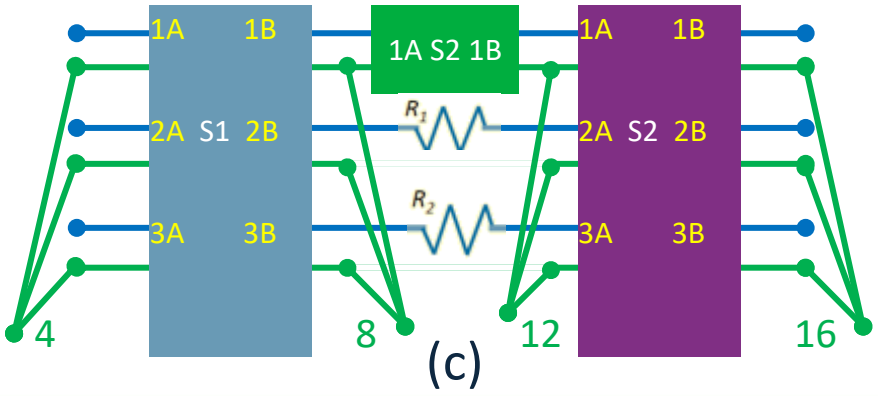












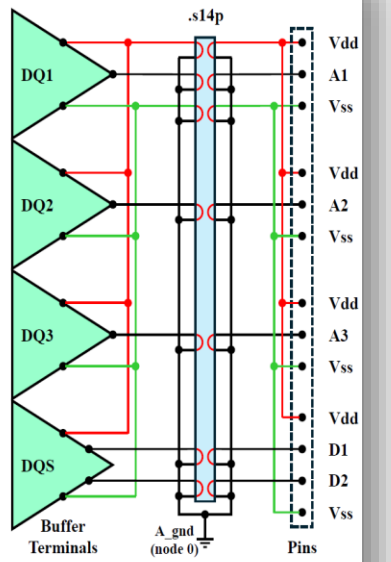
Courtesy to the authors of the pictures available online, used in this slides set.

Case Study-2: *.snp, 2N and N+1 Connections

Problems with the Touchstone examples
in the IBIS v7.2 specification
IBIS-ATM teleconference, January 7, 2025

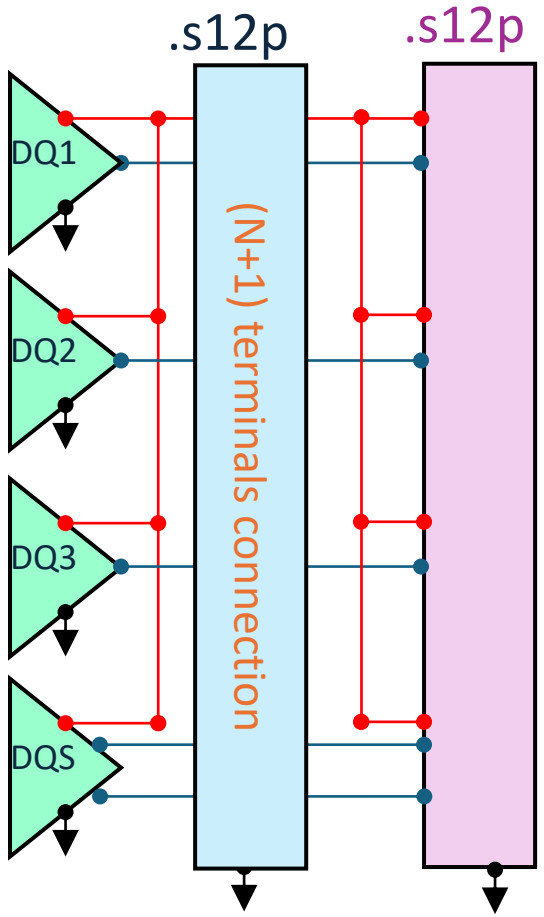
New [Interconnect Model] example 2b (pg. 360)

```
| Example 2b: Same as Example 2 except using File_TS with a single, common
|             reference for all ports
|
[Interconnect Model Set]      Full_TS_PDN_sn_2b
|-----
[Interconnect Model]          Full_TS_buf_pin_2b
File_TS         full_buf_pin.s14p
Number_of_terminals = 15
|
1  Pin_I/O      pin_name     A1   |  DQ1          DQ
2  Pin_I/O      pin_name     A2   |  DQ2          DQ
3  Pin_I/O      pin_name     A3   |  DQ3          DQ
4  Pin_I/O      pin_name     D1   |  DQS+         DQS
5  Pin_I/O      pin_name     D2   |  DQS-         DQS
|
6  Pin_Rail     signal_name  VDD  |  VDD          POWER
7  Pin_Rail     signal_name  VSS  |  VSS          GND
|
8  Buffer_I/O   pin_name     A1   |  DQ1          DQ
9  Buffer_I/O   pin_name     A2   |  DQ2          DQ
10 Buffer_I/O   pin_name     A3   |  DQ3          DQ
11 Buffer_I/O   pin_name     D1   |  DQS+         DQS
12 Buffer_I/O   pin_name     D2   |  DQS-         DQS
|
13 Buffer_Rail  signal_name  VDD  |  VDD          POWER
14 Buffer_Rail  signal_name  VSS  |  VSS          GND
15 A_gnd
|
[End Interconnect Model]
[End Interconnect Model Set]
```



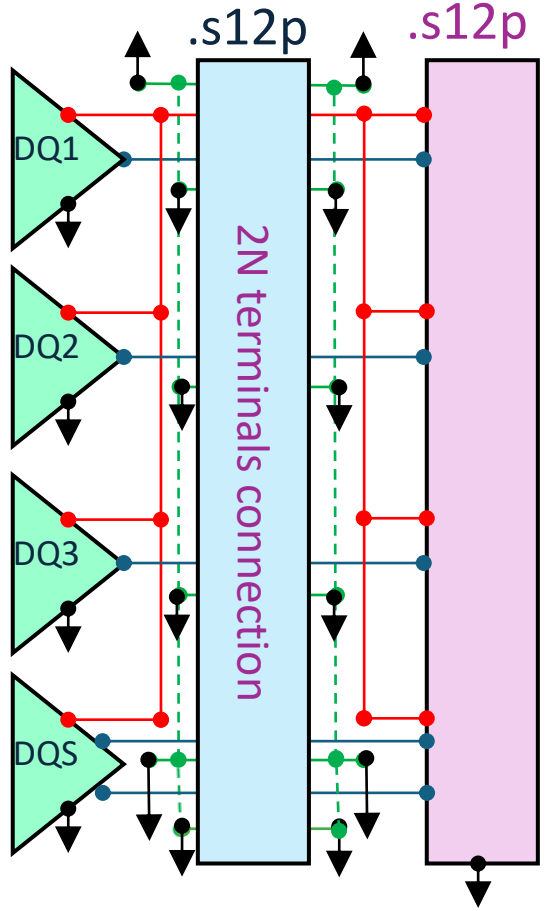
Note that this will be the only example that illustrates a full power aware [Interconnect Model] (for an IBIS package). It is consistent with the [EMD Model] example on pg. 408.

- Set one port for Vdd and another port for Vss is extremely rare case for PI (+SI) sim.
- If Vss was set up for a dedicated port, what is the reference for all signal ports?
- .s14p seems for 2N connection, not for N+1 terminals, in Figure.
- Only N+1 Terminals connection is defined in IBIS File_TS.



Pins/connector shall be a model. there is no physical 1:1 matching.

VSS pins usually grouped in modeling (for 2N terminals), if not all be used as reference for N+1.



Even in 2N terminals connection, the N' will be extremely rare to 1:1 exactly matching GND terminal of DQ buffer.

The model of pins/connector may have more than enough ports defined.

Courtesy to the authors of the pictures available online, used in this slides set.

Take-aways

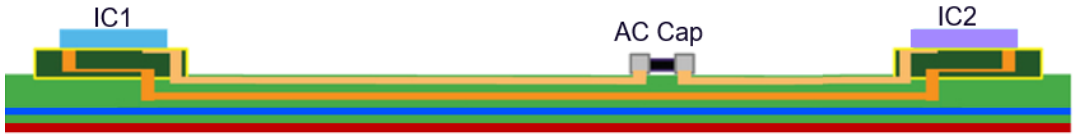
- 2 out of 3 HSPICE defined connections of S-element, with N+1 and 2N terminals, satisfy KCL.
- S-parameter models in SI & PI analysis, include 1+ conductors for reference, and 1+ more conductors for signal or power, but not waveguide (which only supports TE or TM).
- Setup of one port for Power, and another port for GND is extremely rare case for PI (+SI) sim. Instead, one port setup for Power net is usually reference to GND, so is for ports setup for signal nets.
- To properly make connection of S-element, it starts from ports setup for S-parameter modeling, in terms of local reference vs. global reference, and driven modal vs. driven terminal.
- S-parameter modeling usually makes little difference for SI channel, global refence vs. local reference, between fully GND reference, and Power & GND dual reference.
- SPIM modeling definition in BIRD223.1 used local reference, in order to improve the PI analysis accuracy, when the separated Spkg is combined with Spcb at platform, to correlate with S(pkg+pcb).
- Both N+1 and 2N terminals connection of .snp shall be supported.

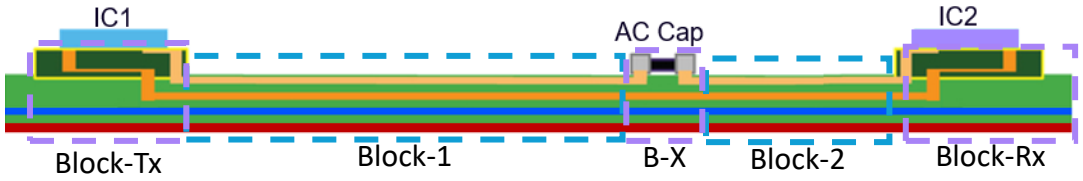
Backup

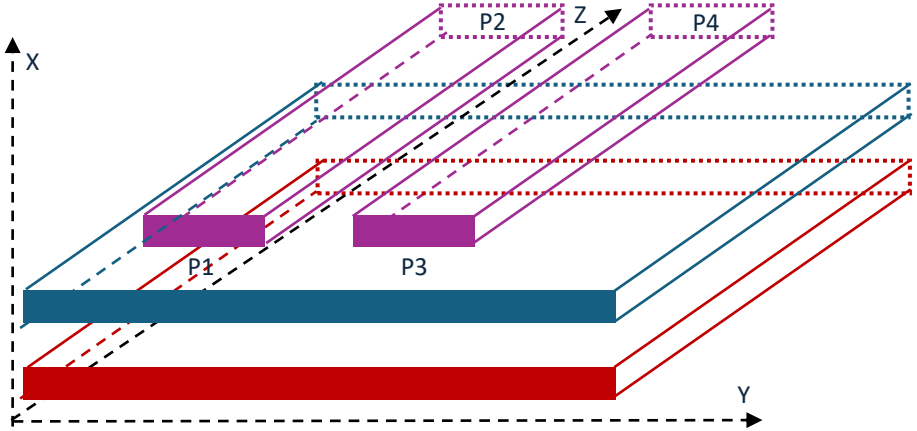
Courtesy to the authors of the pictures available online, used in this slides set.

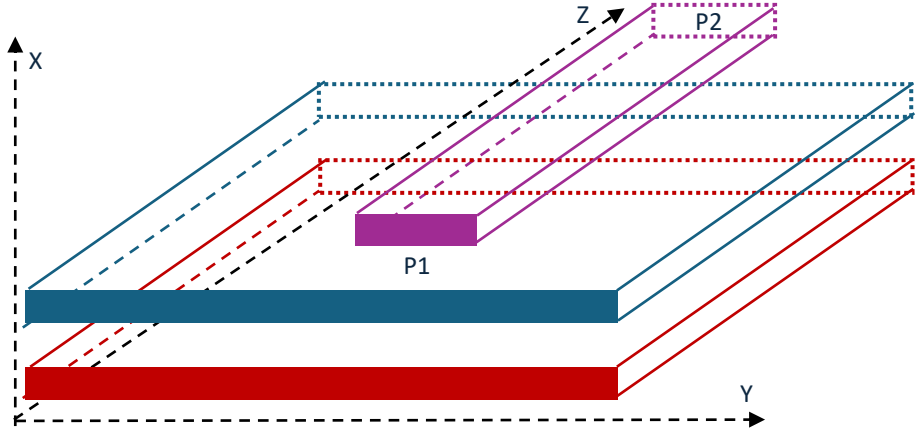
Typical TL Routing, and 2-port setup

- PCIe SI channel, which in differential TL, with AC coupling capacitors
- Starts from 2-port setup for single-ended TL, for segmented blocks, being cascaded in Spice
- Similar 2-port setup applicable for individual power deliver network (PDN)





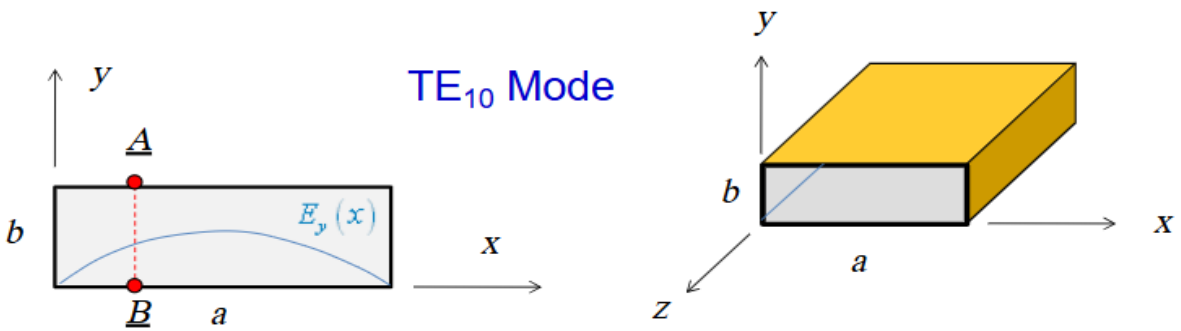




Voltage & Current are not Uniquely Defined in Waveguide

Waveguide Transmission Line Model (cont.)

For a waveguide mode, voltage and current are not uniquely defined.



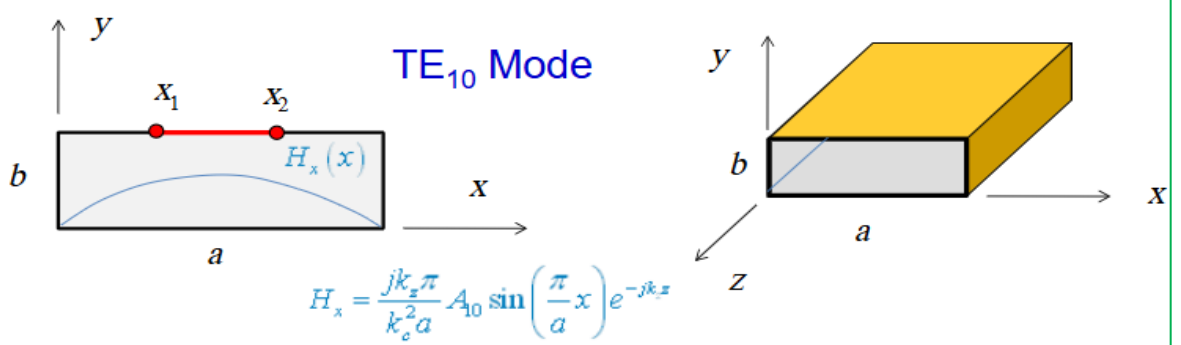
$$E_y = -\frac{j\omega\mu\pi}{k_c^2 a} A_{10} \sin\left(\frac{\pi}{a}x\right) e^{-jk_z z}$$

$$V(z) = V_{AB}(z) = \int_{\underline{A}}^{\underline{B}} \underline{E}\cdot d\underline{r} = \int_b^0 E_y\, dy = \left(\frac{j\omega\mu\pi}{k_c^2 a} A_{10}\right) b \sin\left(\frac{\pi}{a}x\right) e^{-jk_z z} = V_0 \sin\left(\frac{\pi}{a}x\right) e^{-jk_z z}$$

The voltage depends on *x*!

Waveguide Transmission Line Model (cont.)

For a waveguide mode, voltage and current are not uniquely defined.



$$H_x = \frac{jk_z\pi}{k_c^2 a} A_{10} \sin\left(\frac{\pi}{a}x\right) e^{-jk_z z}$$

Current on top wall: $$I(z) = \int_{x_1}^{x_2} J_{sz}^{top}(x)\,dx = \int_{x_1}^{x_2} H_x(x)\,dx = \int_{x_1}^{x_2} \frac{jk_z\pi}{k_c^2 a} A_{10} \sin\left(\frac{\pi}{a}x\right) e^{-jk_z z}\,dx$$

Note: If we integrate around the entire boundary, we get zero current.

$$= \left(\frac{jk_z\pi}{k_c^2 a} A_{10}\right)\left(-\frac{a}{\pi}\right)\left[\cos\left(\frac{\pi}{a}x_2\right) - \cos\left(\frac{\pi}{a}x_1\right)\right] e^{-jk_z z}$$

$$= \frac{I_0}{2}\left[\cos\left(\frac{\pi}{a}x_1\right) - \cos\left(\frac{\pi}{a}x_2\right)\right] e^{-jk_z z}$$

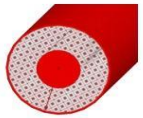
The current depends on the length of the interval!

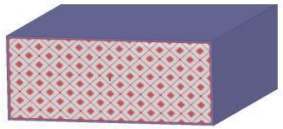
https://slideplayer.com/slide/7530735/

Same *.snp will have totally different meaning, & different application

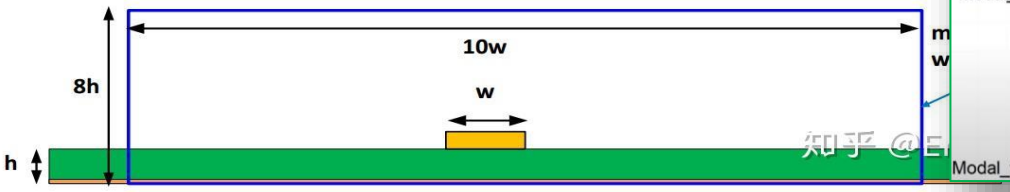
Wave Port Sizing

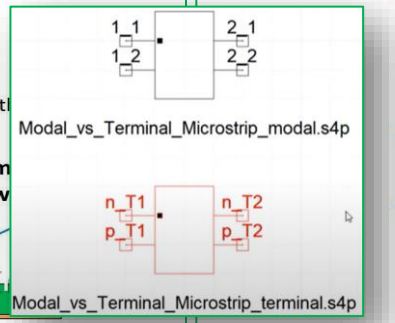
- **Closed Transmission Line Structures**
  - The boundary enforced on the port's edge implies the transmission line modeled by the Wave Port always sits inside a waveguide structure. The enclosing material forms the port's edge boundary.


Coax

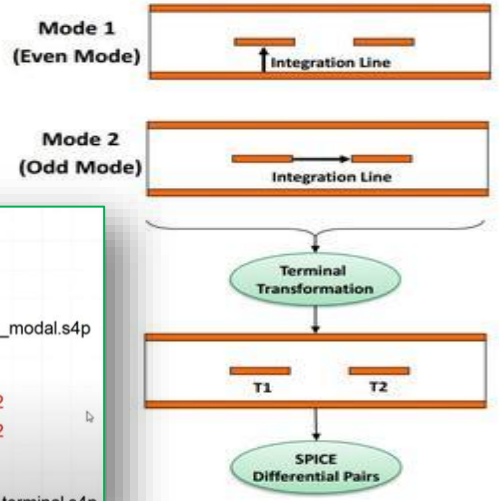

Waveguide

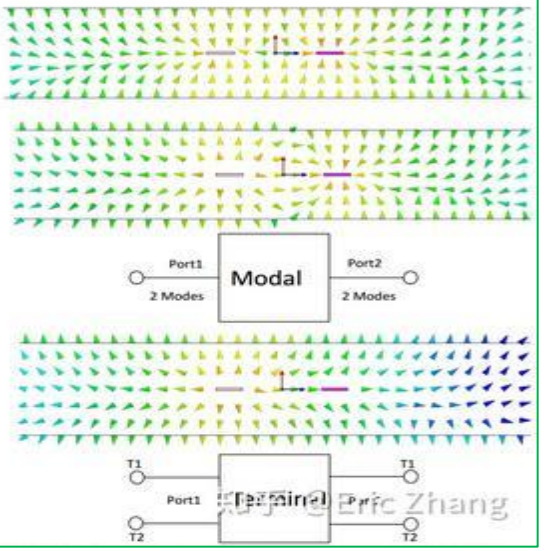
- **Open transmission line structures require additional consideration**
  - Microstrip, Co-Planar Waveguide, Slotline
  - Wave Ports must be large enough to capture the entire transmission line's field structure
    - For open transmission line structures the Wave Port must surround the entire structure.
    - Make sure the transmission line fields are not interacting with the port's boundary condition.
    - Wave Ports too small can lead to incorrect characteristic impedances, and add additional reflection to t





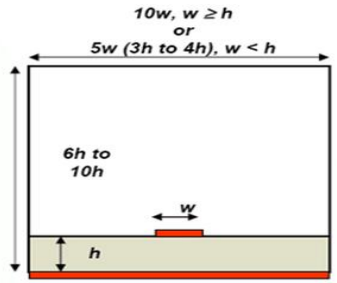
Excitations: Modal vs. Terminal in Stripline

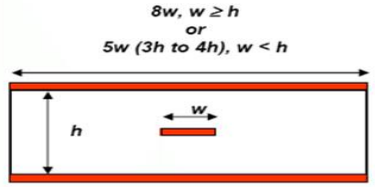




Wave Port Sizing Guidelines

- **Microstrip port height between 6h and 10h**
  - Tend towards upper limit as dielectric constant drops and fringing fields increase
  - Make bottom edge of port co-planar with upper face of ground plane
- **Microstrip port width**
  - 10w for w ≥ h
  - 5w, or on order of 3h to 4h, for w < h
- **Extend stripline port height from upper to lower groundplane (h)**
- **Stripline port width**
  - 8w for w ≥ h
  - 5w, or on order of 3h to 4h, for w < h
- **Can also make side walls of port Perfect H boundaries**





Port sizing guidelines are not inviolable rules. If meeting height and width requirements result in rectangular aperture larger than λ/2 in one dimension, the substrate and trace may be ignored in favor of a waveguide mode. When in doubt, run a ports-only solution to determine which modes are propagating.

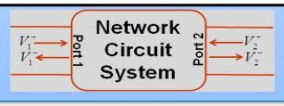
HFSS Excitation Methods, Propagation, and Solution Type

Driven Modal

- Fields based transmission line interpretation
- Port's signal decomposed into incident and reflected waves
- Excitation's magnitude described as an incident power

Modal Propagation

- Energy propagates in a set of orthogonal modes
- Modes can be TE, TM and TEM w.r.t. the port's normal
- Mode's field pattern determined from entire port geometry
- Each Mode has its own column and row in the S, Y, and Z parameters.



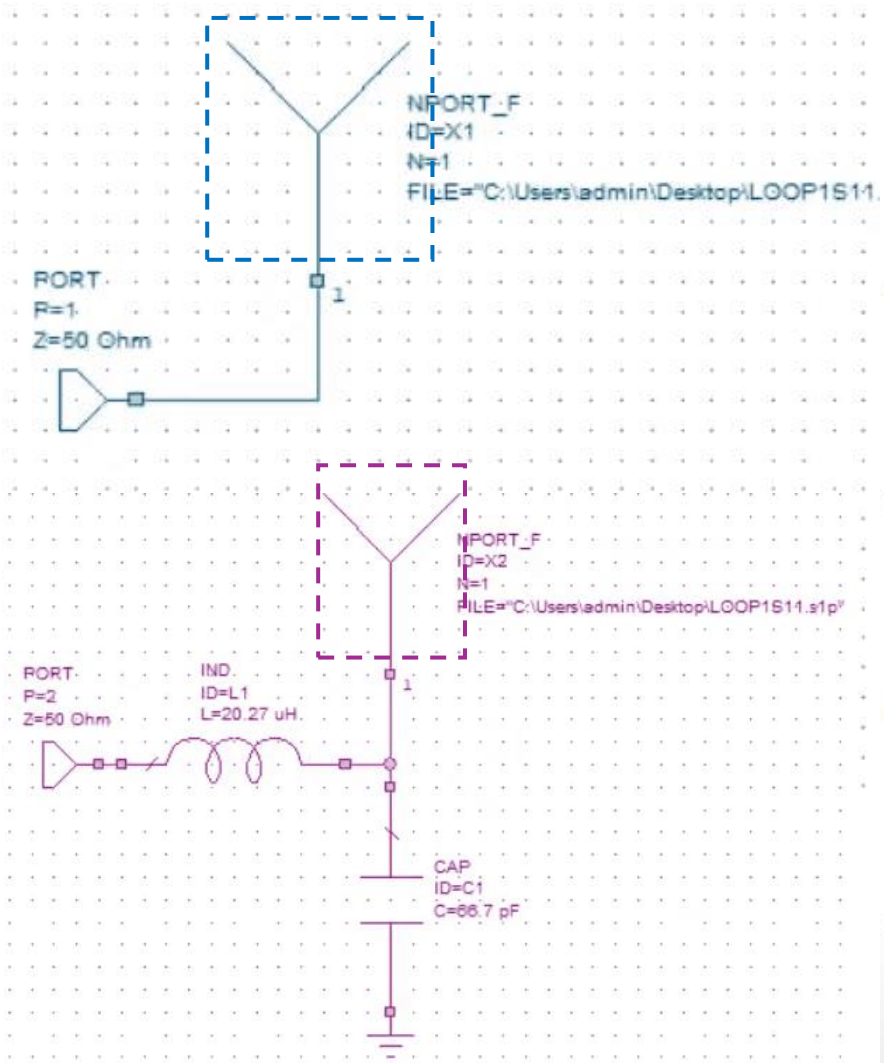
Driven Terminal

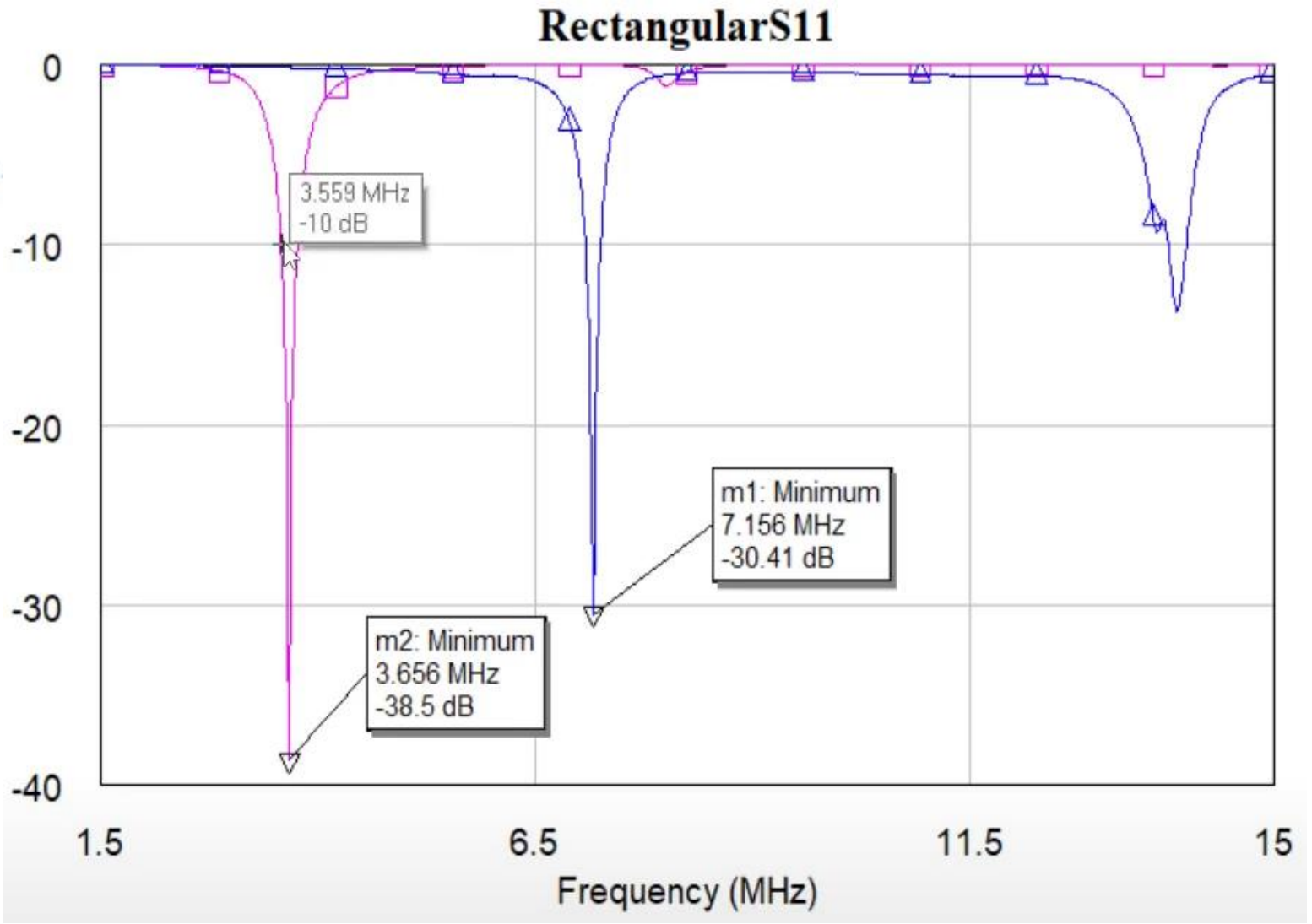
- Circuit Based transmission line interpretation
- Port's signal interpreted as a total voltage (Vtotal = Vinc + Vref)
- Excitation's magnitude described as either a total voltage or an incident voltage
- Supports Differential S-Parameters

Terminal Propagation

- Each conductor touching the port is considered a terminal or a ground
- Energy propagates along each terminal in a single TEM mode
- Each Terminal has its own column and row in the S, Y and Z parameters
- Does not support symmetry boundaries or Floquet Ports

Antenna Simulation with *s1p





Courtesy to the authors of the pictures available online, used in this slides set.

Thank You!

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