Hybrid IBIS Summit

@ IEEE EMC SIPI 2025 Conference

IBIS Power Integrity Introduction

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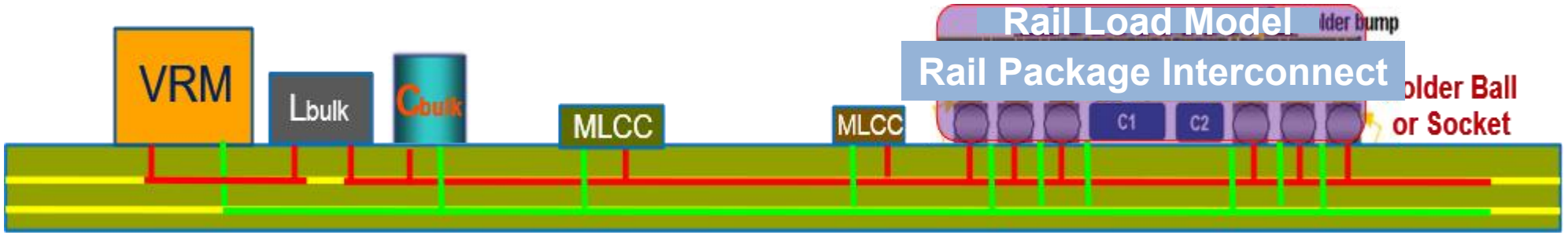
Power Delivery Network



Overview

- Power Integrity Models of Silicon and Package
- Examples of Analysis That Can Be Done With These Models
- Rail Package Interconnect Model
- Rail Load Model
- Example of Rail Interconnect and Load Model
- Discussion Points, Next Steps

Power Integrity Models of Silicon and Package

- Power Integrity Analysis tools require models of silicon current requirements and the package interconnect model between chip rail bumps and pin rail balls.
- Rail Load Model
  - DC Load(s)
  - PWL (Current vs Time Waveforms)
  - Subsystem DC Load(s)
  - Rules
- Rail Package Interconnect Models
  - Bump pads can be grouped into subsystems (obfuscate IP)
  - Pin balls can be grouped to limit complexity of the model
  - Interconnect model between bumps and balls can be
    - Touchstone file
    - IBIS-ISS SPICE subckt
    - Resistor matrix

Examples of Analysis That Can Be Done With These Models

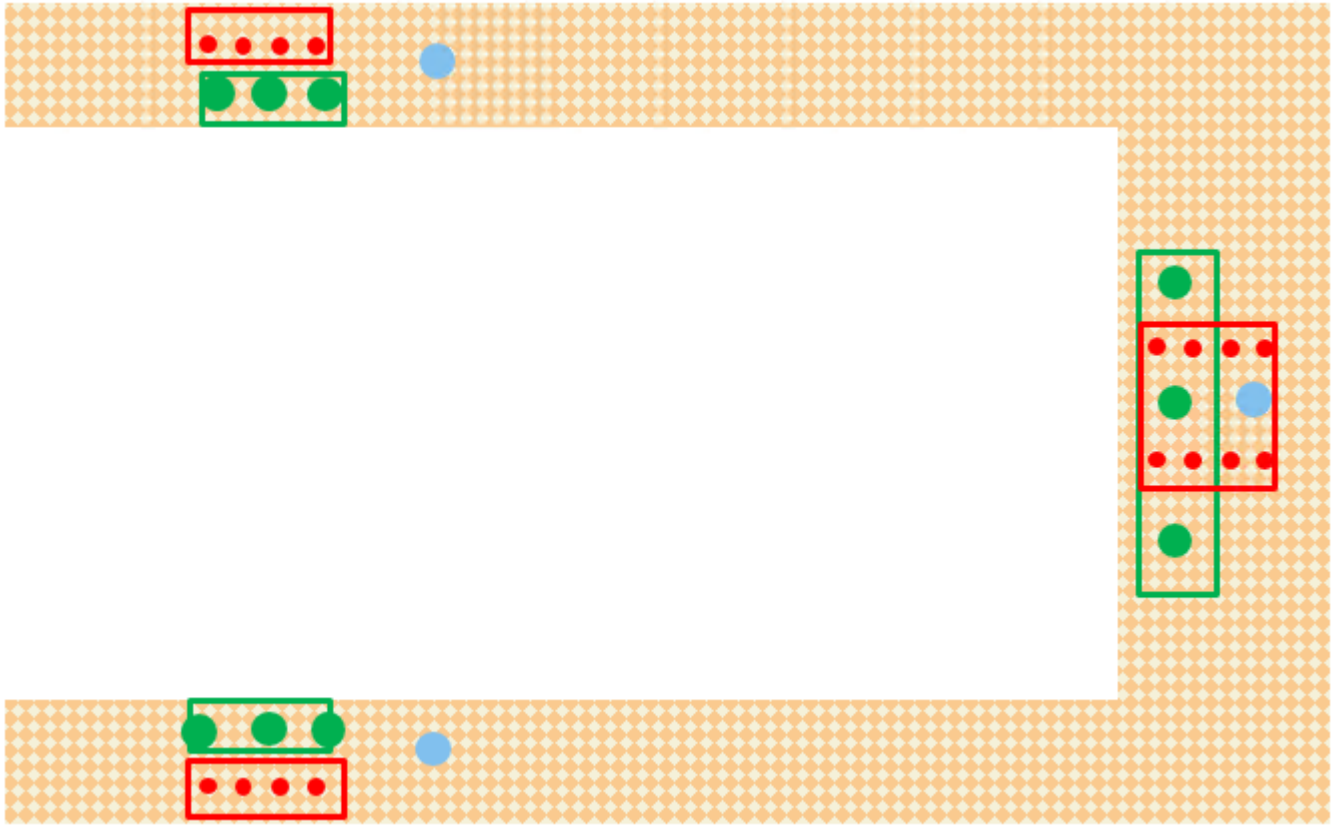
- DC analysis
  - IR Drop
  - Thermal Hot Spots
- AC (Frequency Analysis)
  - Determine the impedance of PDN at VRM and Die
- TD (Time Domain Transient analysis)
  - Vendor supplied current vs time PWL
  - User created current vs time PWL

Models Can Supply Rules To Apply To Analysis Results.

Rail Package Interconnect Model

- SPICE subckt or a Touchstone file
- Includes on die capacitance
- Rail bump pads are grouped into one or more “Current Source Ports”.
  - The Rail Load Model is the container for the currents and rules applied to these ports.
- Rail ball pins can be grouped into one or more “Board Ports”
  - It is the responsibility of the EDA tool to mate the “Board Ports” of this model to the Board PDN model.
  - The Rail Load Model contains rules applied to these ports.
- In addition to Current Source and Board Ports, there can be additional “Probe Ports”
  - The Rail Load Model contains rules applied to these ports.
- Can be for .ibs files or .emd files

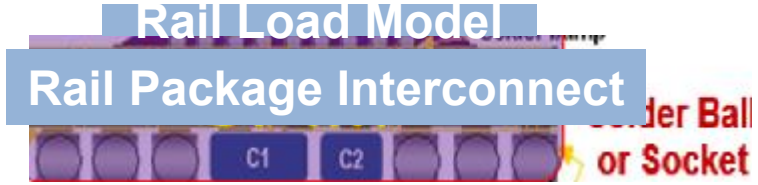
A Modern Package Interconnect for one Rail Net Size ~2”x2”



- Red Dots are Bumps (Pads)
- Green Dots are Balls (Pins)
- 3 Bump Group Ports (Red Rectangles)
- 3 Ball Group Ports (Green Rectangles)
- 3 Probe Ports (Blue)

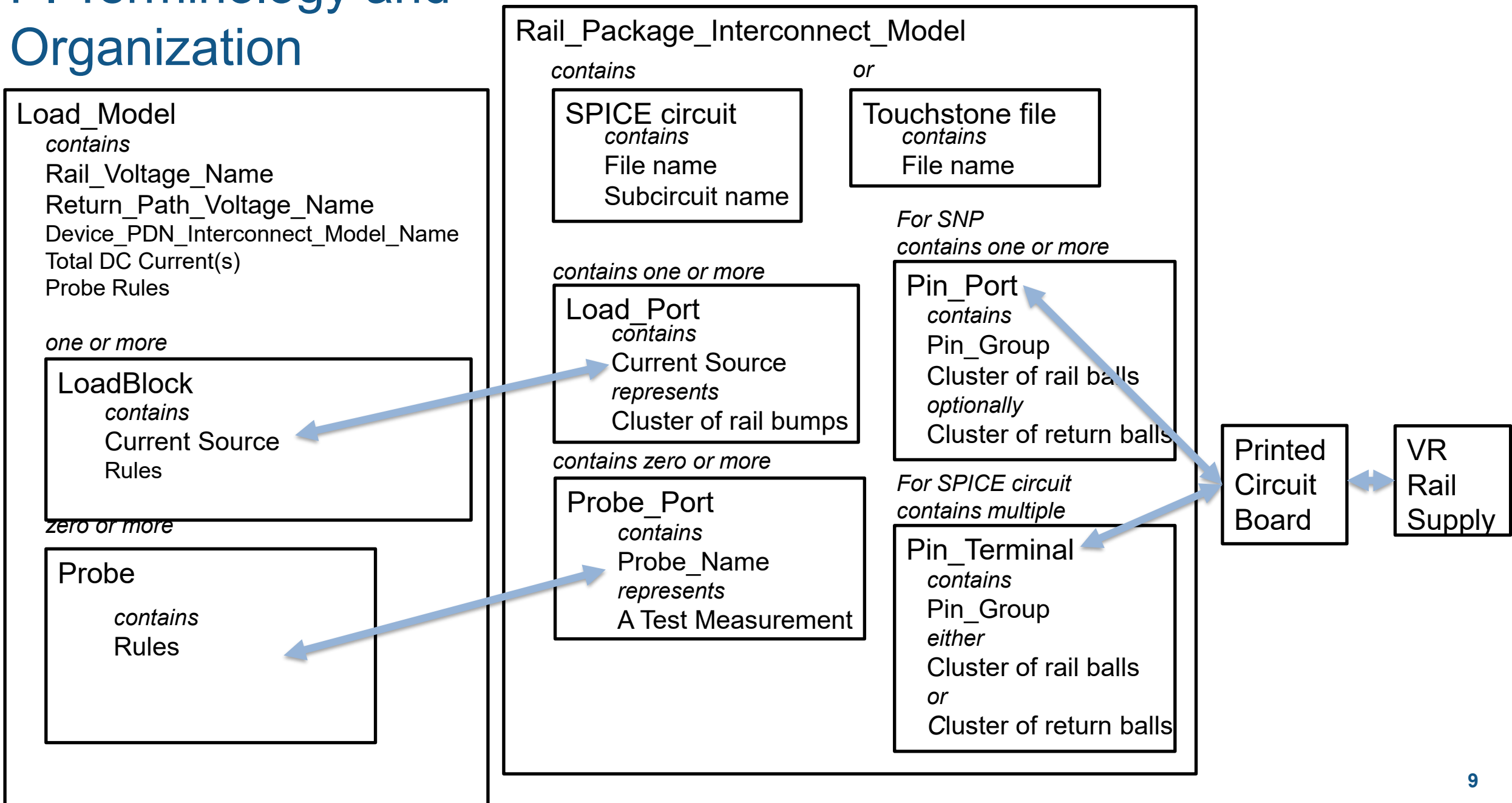
- The Balls Connect to the PCB at the Green Dots, Require Pin Numbers to Mate to Board
- The Pads Connect to the Load and the XY coordinates on the Chip are Obfuscated from the User

Rail Load Model



- Pairs with “Rail Package Interconnect Model”
- One or more Current Sources (aka subsystems)
  - Each subsystem can change DC Current Levels independently
  - A current source is connected to a package model current source port
  - Multiple current sources can be combined to a single Package Model current source port
  - DC Current Levels
  - Rise and fall time from one DC level to another DC level
  - PWL current vs time waveforms
    - IC Vendor can supply waveforms as a stress test
    - User can generate their own PWL waveforms to emulate subsystems changing levels
- Rail Rules
  - Voltage range rule
  - Impedance target/mask rule
  - Max Current/Pin Rule
- Rules
  - Can be associated with any Port (Current Source, Pin, Probe)
  - Can override Rail rules (Global/Local)

PI Terminology and Organization



One Possible Format of a Rail Interconnect and Load Model Pair

```
[Rail Interconnect Model]    VDD_s3p
        File_TS                  VDD.s3p
        Analysis_type            DC AC TD
        Number_of_ports = 3
                1 Pin_Signal_Name      VDD
                  | Can be All, One or Group of VDD Pins
                  |  Reference terminal is optional and can be:
                  |          All, One or Group of VSS Pins
                  | EDA tool mates ports and their reference terminals with Board PDN
                2 Pad_Current_Source   <Name optional>
                  | Can have multiple current source ports
                  | Multiple current sources can connect to one port
                3 Probe                <Name optional>
[End Rail Interconnect Model]

[Rail Interconnect Model]      VDD_iss
        | Can separate ground return path losses
        File_IBIS-ISS            VDD.ckt
        Analysis_type            DC AC   TD
        Number_of_terminals = 3
                1 Pin_Signal_Name      VDD
                  | Can be All, One or Group of VDD or VSS Pins
                  | EDA tool mates pin terminals with Board PDN
                2 Pad_Current_Source   <Name optional>
                  | Can have multiple current source terminals
                  | Multiple current sources can connect to one terminal
                3 Probe                <Name optional>
[End Rail Interconnect Model]
```

```
[Rail Signal Name]       VDD              | VDD is data book signal name
        [Load Model]   Load_Model_1                    | Can have multiple Load Models
                Analysis_type        DC AC TD          | Can limit to any one or two of these
                Rail_Interconnect_Model      VDD_iss   | This Load Model also works with VDD_s3p

                [Current Source]             VDD       | Can have multiple Current Sources
                        Terminal             2         | Can be differential to two terminals
                        [Current Levels]
                                Idle     1
                                Thermal 4
                                Turbo    6
                        [End Current Levels]
                        RiseTime                 10n   | For user generated current waveforms,
                                                       | FallTime is optional,
                        Current_waveform_file    FileName1    WaveformName1 | Can be flattened in Model
                [End Current Source]

                [Impedance Target Mask]      ImpedanceTargetName1          | Can reference file name
                        | frequency          typ          min          max
                        1.0e4                6.9e-3       5.0e-3       8.0e-3
                        …
                        2.0e7                28.5e-3      20.0e-3      40.0e-3
                [End Impedance Target Mask]

                [Rule Name] Rule1
                        |                    V(target)  V(min)  V(max)
                        Voltage_target       1.8        1.7     1.9      | Rules can be local or global
                        DC_max_pinCurrent    0.25
                        Impedance_Target     ImpedanceTargetName1
                [End Rule Name]

                [Rule Ports]   Terminal(s)/Port  | This example applie same rule to all three Terminal(s)/Port
                        Rule1        1     | Can be between two terminals
                        Rule1        2     | Can be applied to a Pin Port, Current Source Port or Probe Port
                        Rule1        3
                [End Rule Ports]
        [End Load Model]
[End PI Rail]
```

Discussion Points, Next Steps

- Are we missing anything?
- Can/will IC Vendors supply this data?
- Need to handle return paths correctly!
- Can you use these models to do the analysis/simulation that you want/need to do?

- Next steps
  - Resolve any issues raised by this presentation
  - Review proposed BIRD
    - Names of keyword, parameters and rules
    - Does it meet the requirements specified above?