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Neural Network meets IBIS-AMI
: Data-driven Approach to Nonlinear Buffer Modeling

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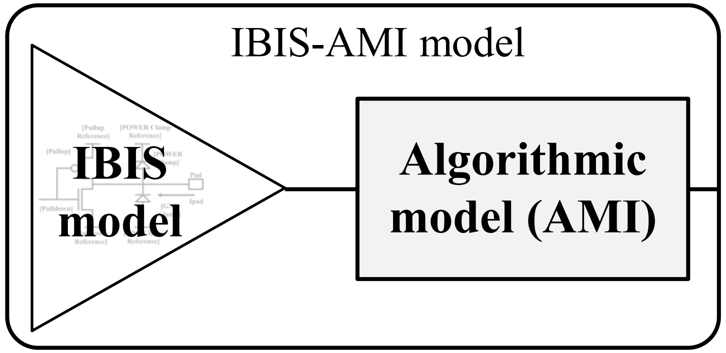
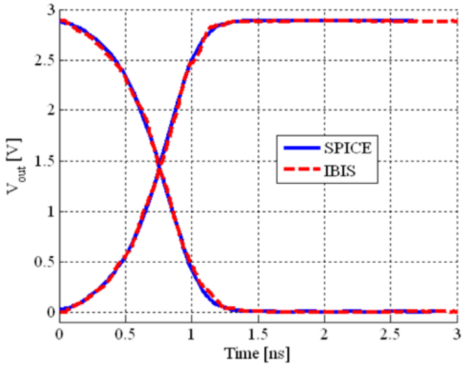
Outline

- Introduction
- Transformer Model Architecture
- IBIS-AMI simulation implementation method
- Verification
- Conclusion

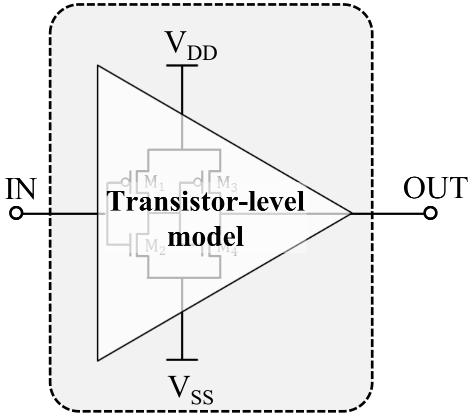
IBIS – AMI Model

❖ I/O Buffer Information Specification (IBIS) – Algorithmic Model Interface (AMI)

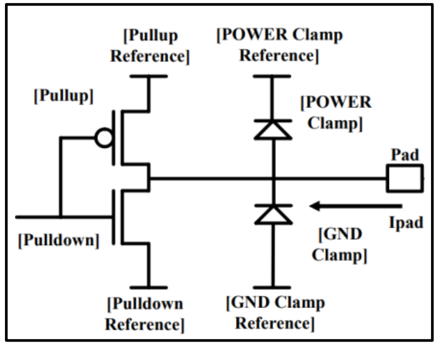




SPICE circuit model



Behavior model

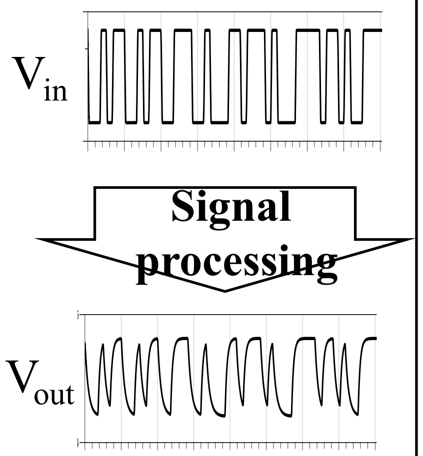


.ami file

Define algorithm mode
- CTLE
- FFE ...
- DFE

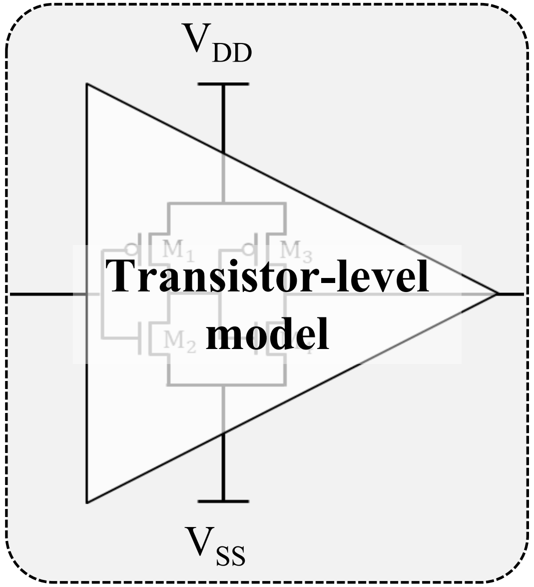
Control parameters
- CTLE : pole/zero value
- FFE : tap coefficient
- DFE : tap coefficient

.dll file



Limitations of the Conventional IBIS-AMI & NN-based Models

Buffer model

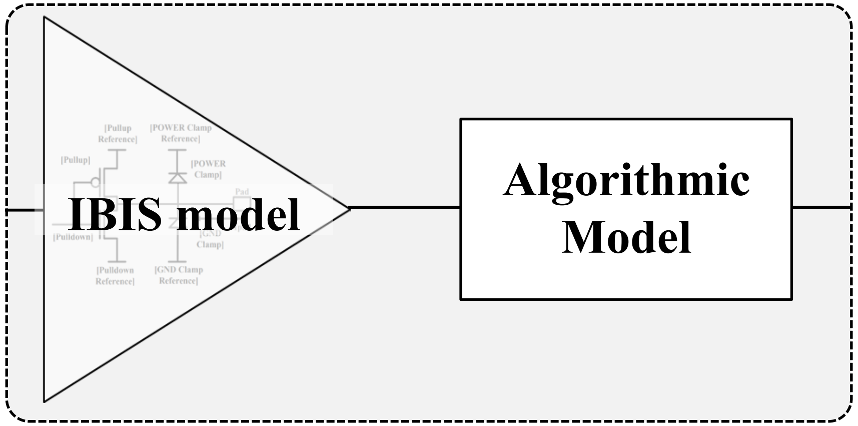


Complicated & Nonlinear

Closed-form modeling requiring **detailed domain knowledge**

High modeling effort to build nonlinear models

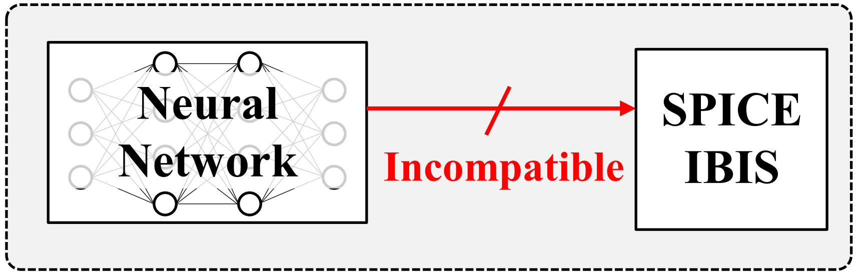
Conventional **IBIS-AMI** model



Incompatibility with standard SPICE/IBIS-AMI flows

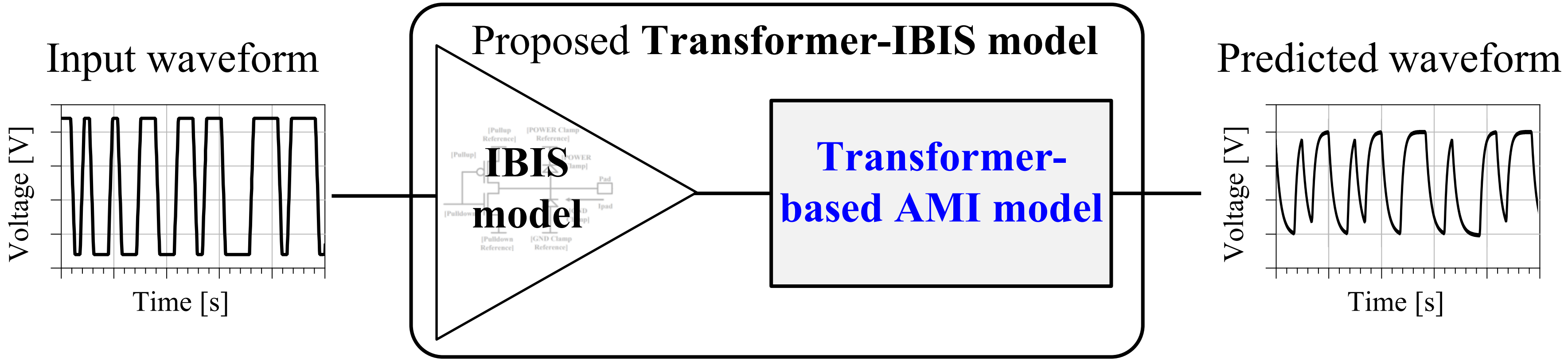
Separate model construction for each PVT condition

Conventional **NN-based** model



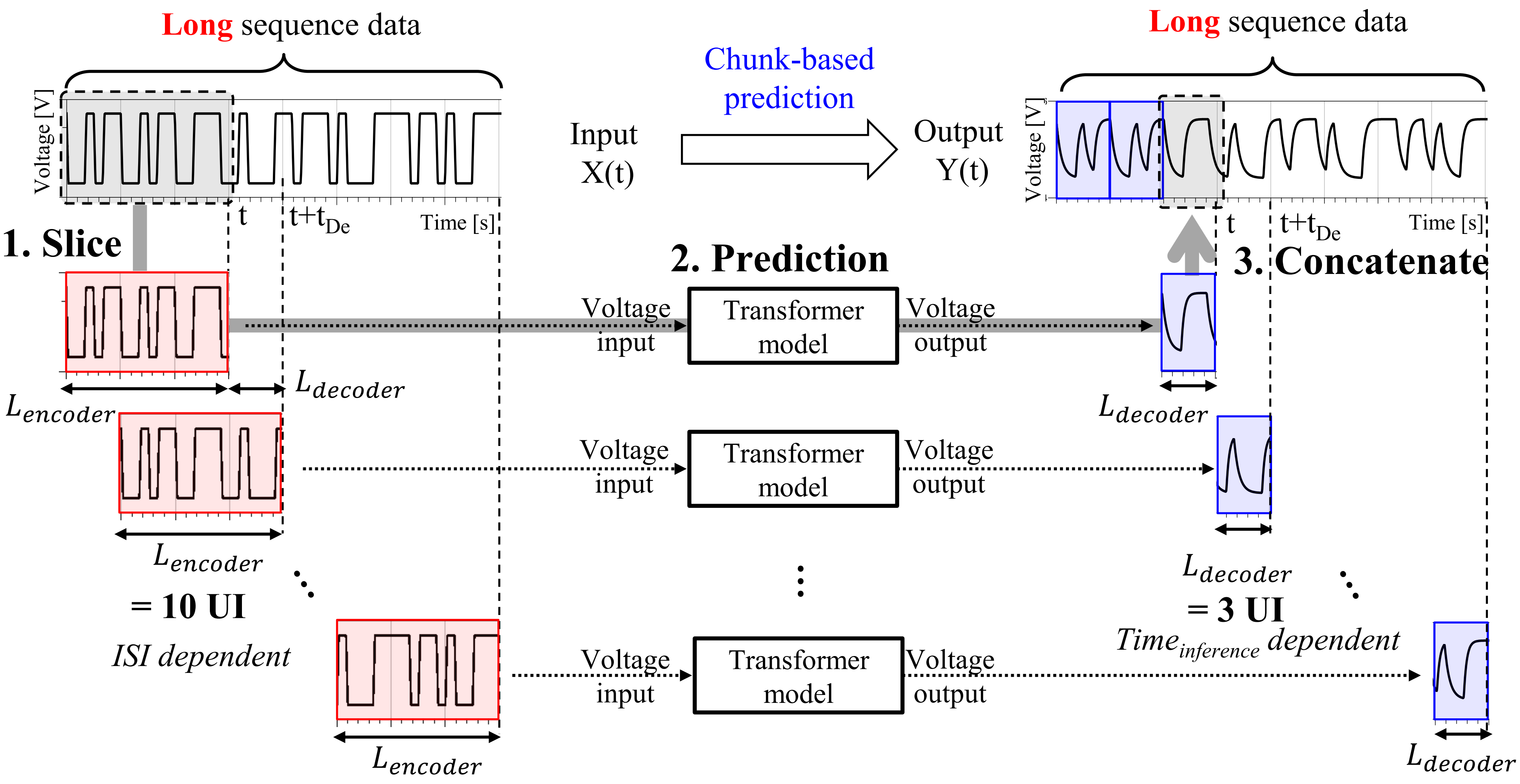
Objective

- Objective:
  - Accurate nonlinear buffer modeling **without domain-knowledge** based manual equation.
  - **Direct compatibility with the standard IBIS-AMI flow** by implementing the NN model into AMI.
  - **Reduced modeling effort** via supervised training on simulated waveform datasets.
  - **A single model covering all PVT corners** through operating-condition embedding



< Proposal of NN-enabled IBIS-AMI modeling framework >

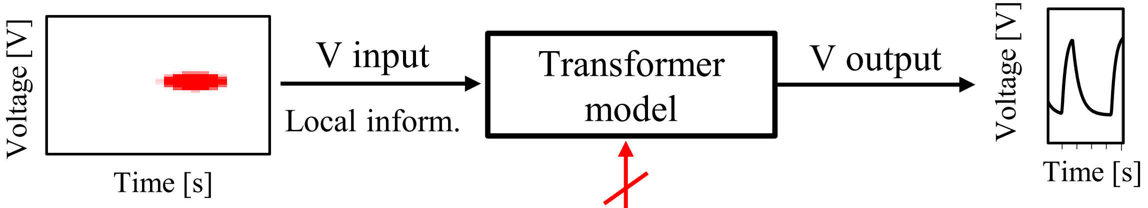
Chunk-based Transformer for Voltage Sequence Prediction



< Conceptual image of chunk-based voltage sequence prediction using transformer model >

Limitation of Chunk-based Transformer

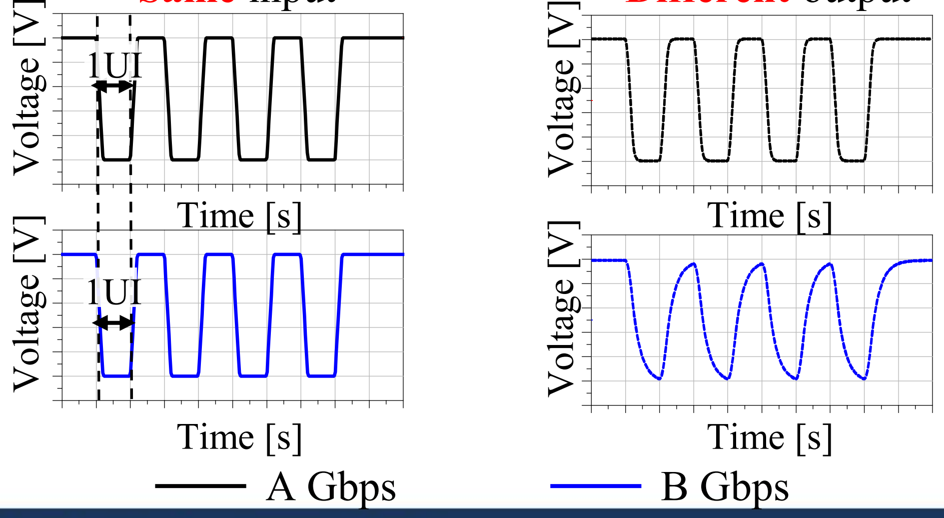
< Limitation 1 : Lack of global information >



Global information : Datarate, V_{swing} , $Type_{corner}$, …

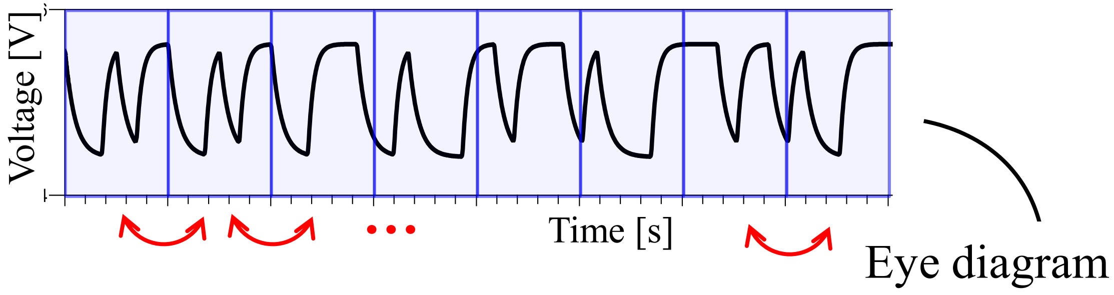
Represent characteristics of voltage sequence or driver

Ex) Different datarate

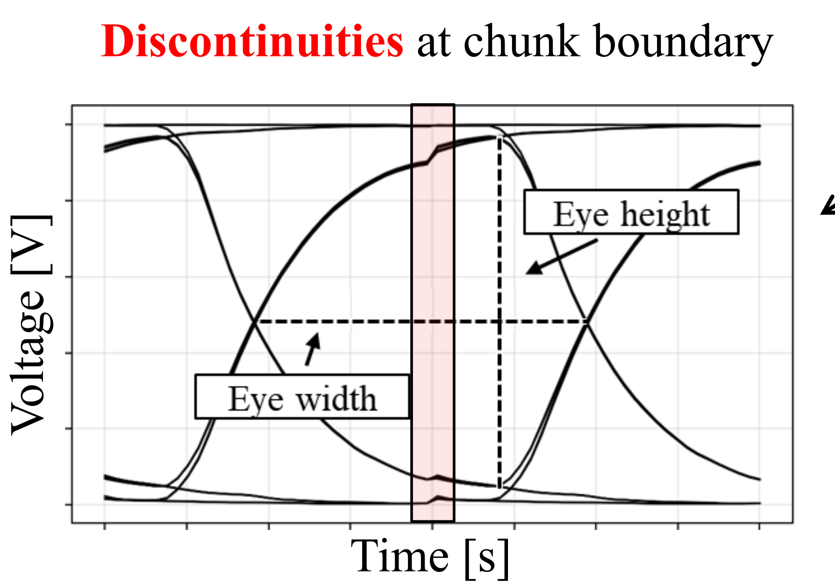


< Limitation 2 : Chunk discontinuity >

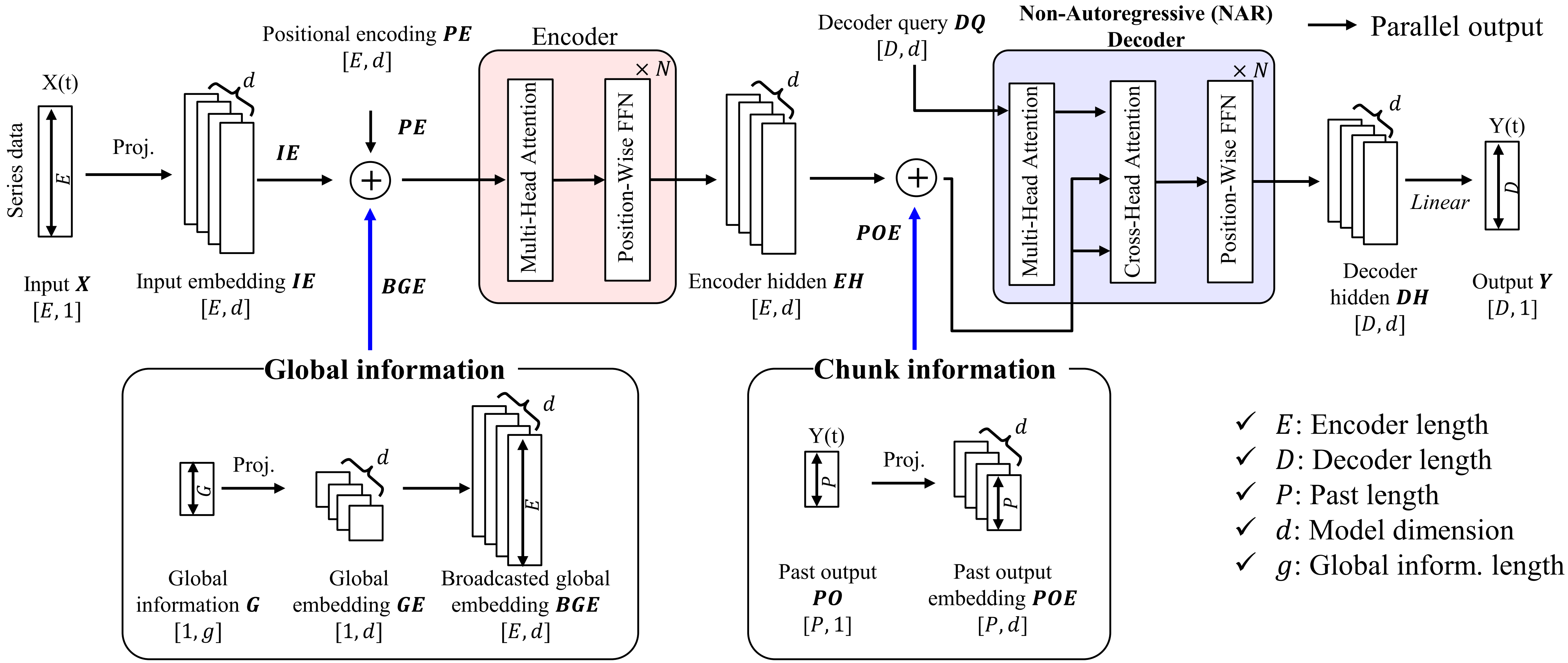
Concatenated output prediction



Discontinuities at chunk boundary



Proposed Transformer Model Architecture



- ✓ E: Encoder length
- ✓ D: Decoder length
- ✓ P: Past length
- ✓ d: Model dimension
- ✓ g: Global inform. length

< Proposed transformer model architecture considering global and chunk information >

Training & Inference Process

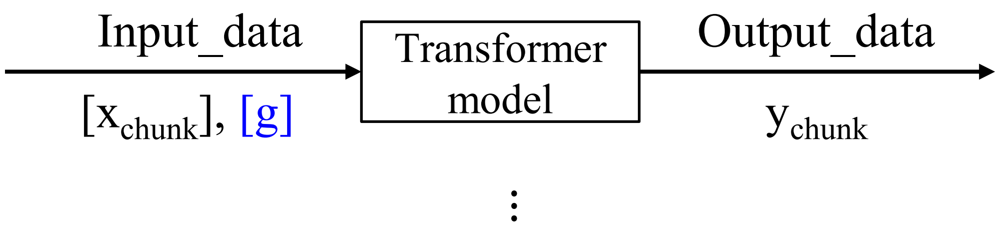
Global information → **Numeric global information : [g]**

- Datarate → $\Delta t \times \alpha$
- V_{swing} → V_{swing}
- $Type_{corner}$ → $Value_{corner} \begin{cases} MIN = -1 \\ TYP = 0 \\ MAX = 1 \end{cases}$

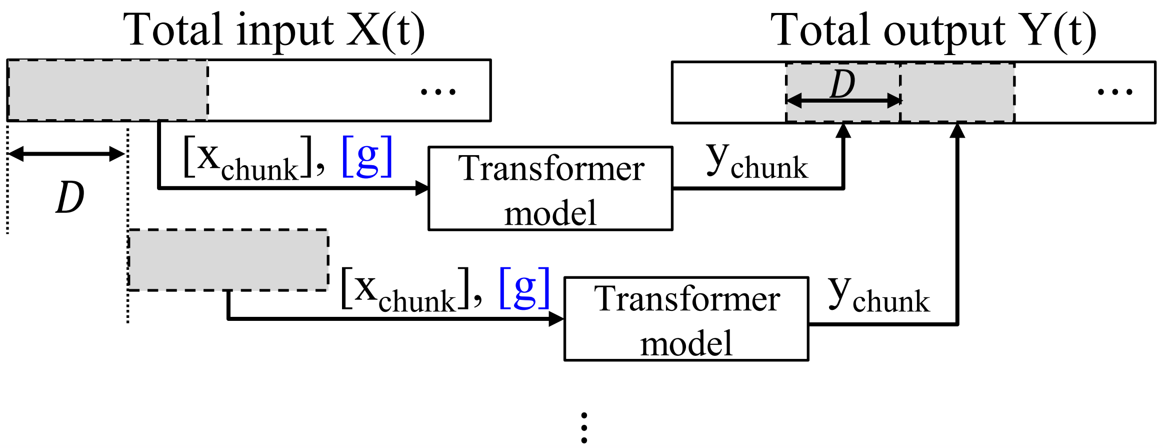
✓ Time step : $\Delta t = \frac{UI}{32}$

✓ Scale factor : $\alpha = 10^{12}$

< Training process >

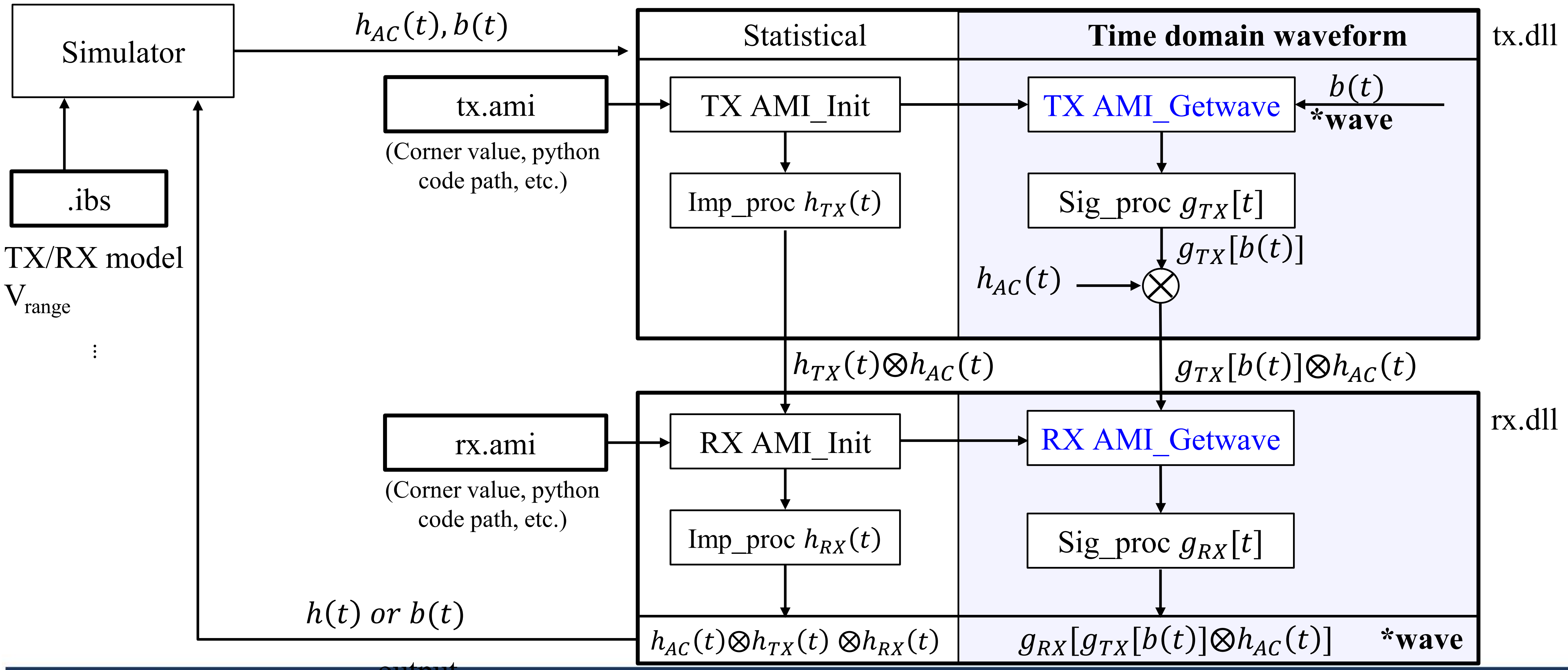


< Inference process >

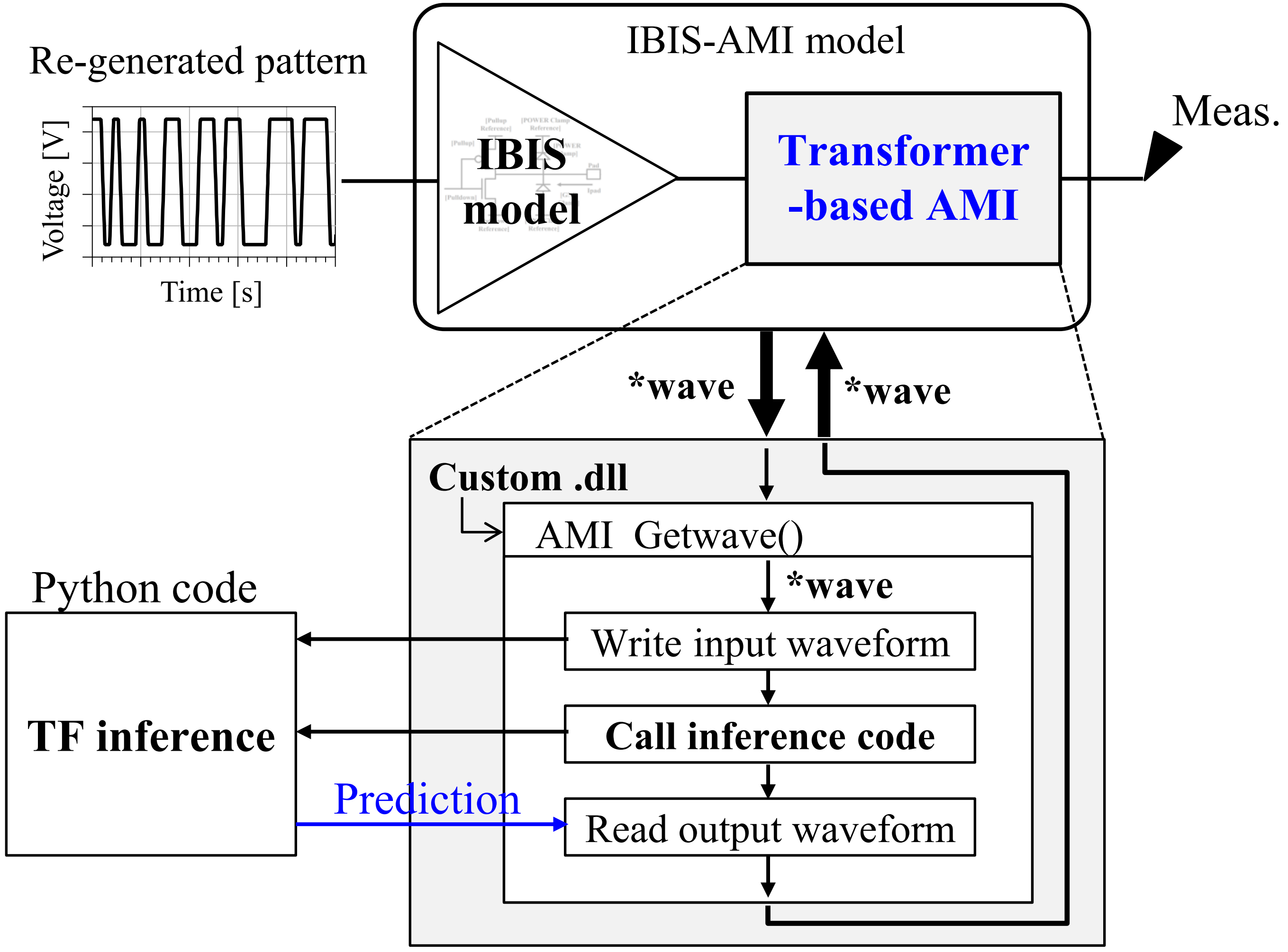


How IBIS-AMI Processes Waveforms

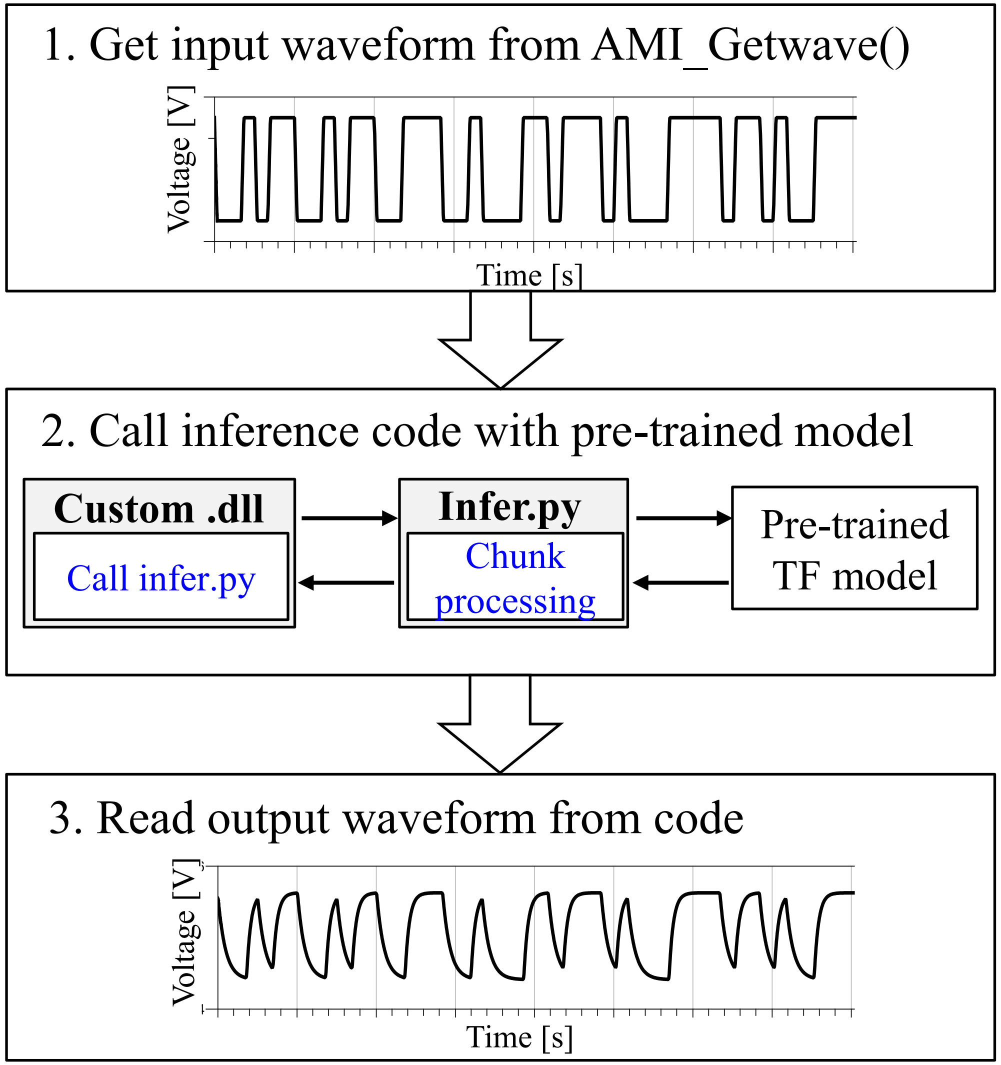
$h_{AC}(t)$: Impulse response of analog channel (Driver + channel)
$b(t)$: Bit stream



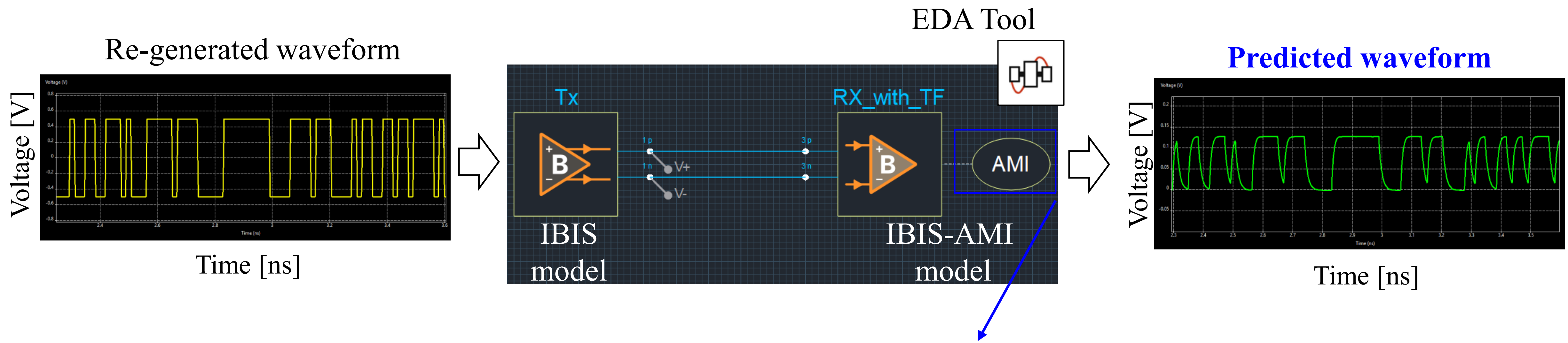
Transformer-based IBIS-AMI Simulation [1/2]



Include **TF-based prediction process** in Custom .dll



Transformer-based IBIS-AMI Simulation [2/2]



Should be same as train data :

- ✓ Time step : $\Delta t = \frac{UI}{32}$
- ✓ Rising/falling time

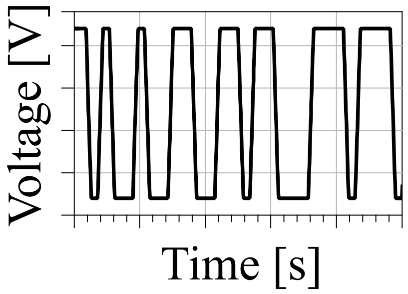
.ami should includes

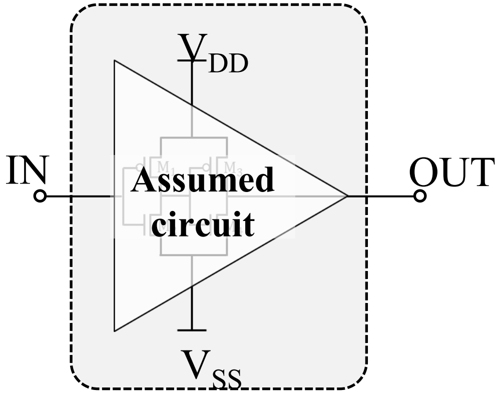
- ✓ Corner : global information
- ✓ Inference code : TF implementation
- ✓ Executable python : TF implementation

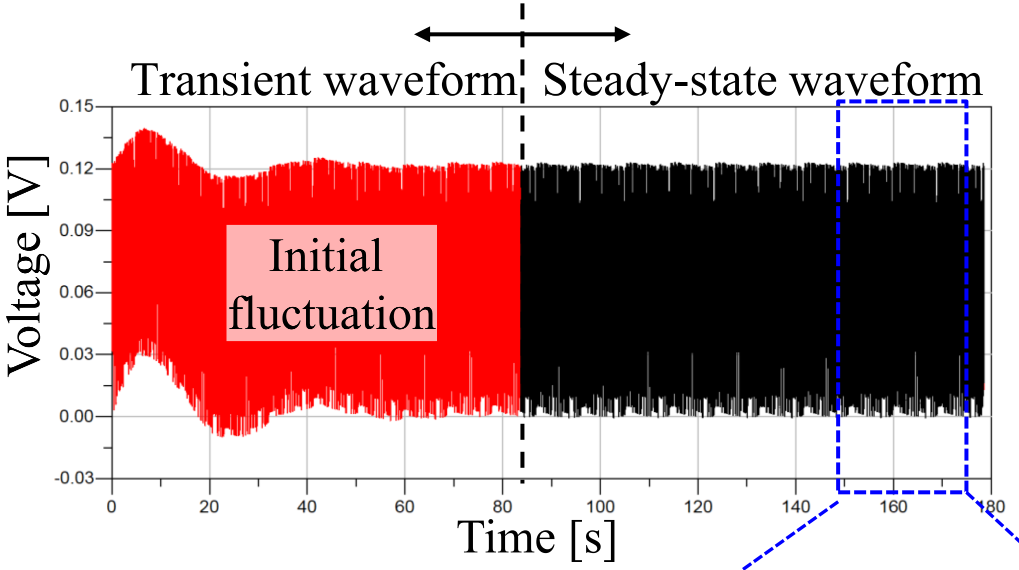
.dll and inference code should be in same location

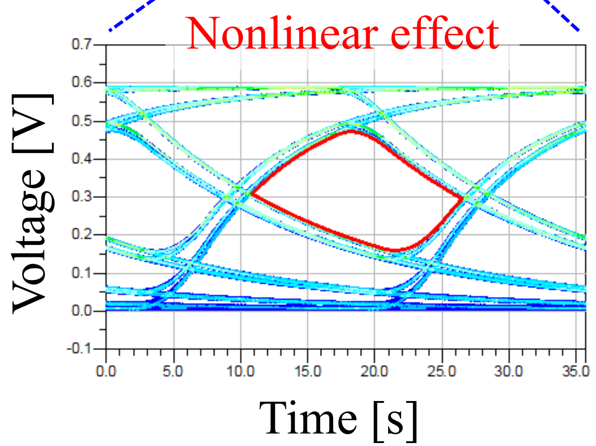
Simulation Setup for Validation

Training data : PRBS15







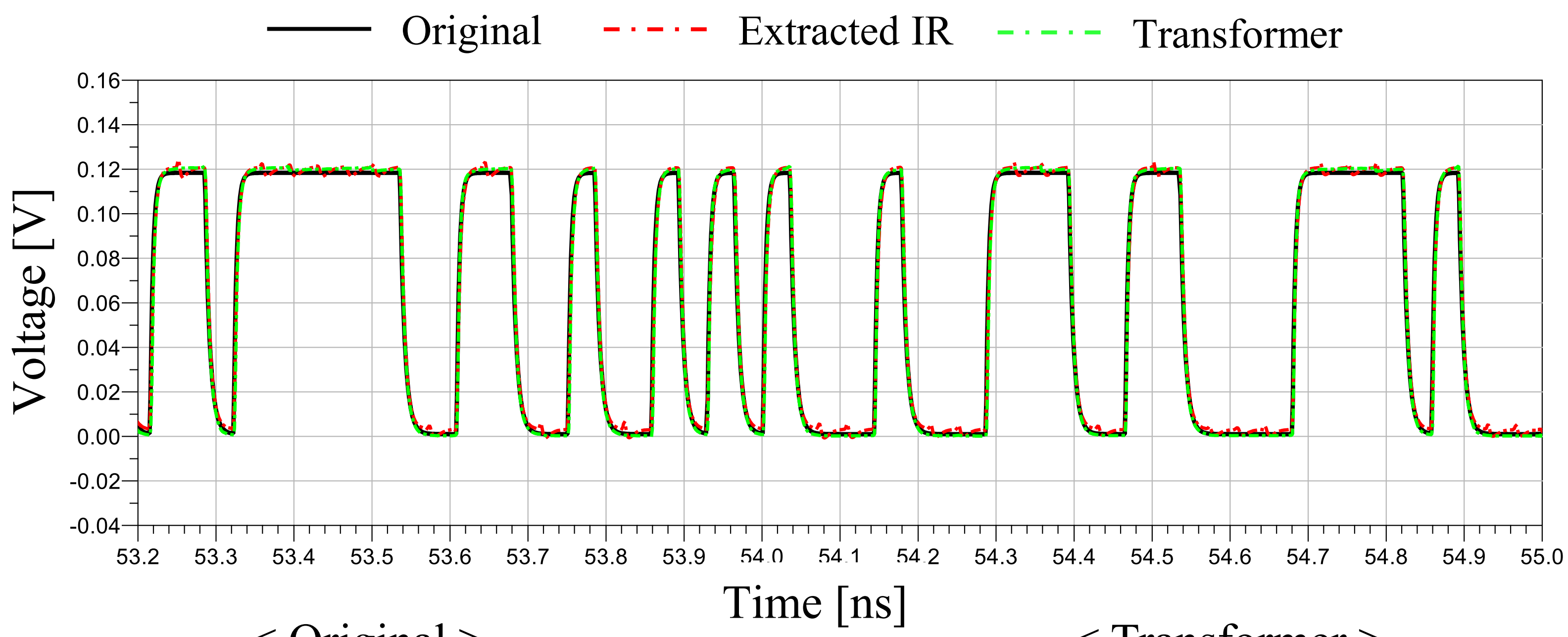


< 56 Gbps / 2 V / MAX case >

Global information

- ❑ Datarate ⟶ [28 Gbps / 56 Gbps / 84 Gbps]
- ❑ V_{swing} ⟶ [1 V / 2 V / 3 V]
- ❑ $Type_{corner}$ ⟶ [MIN / TYP / MAX]

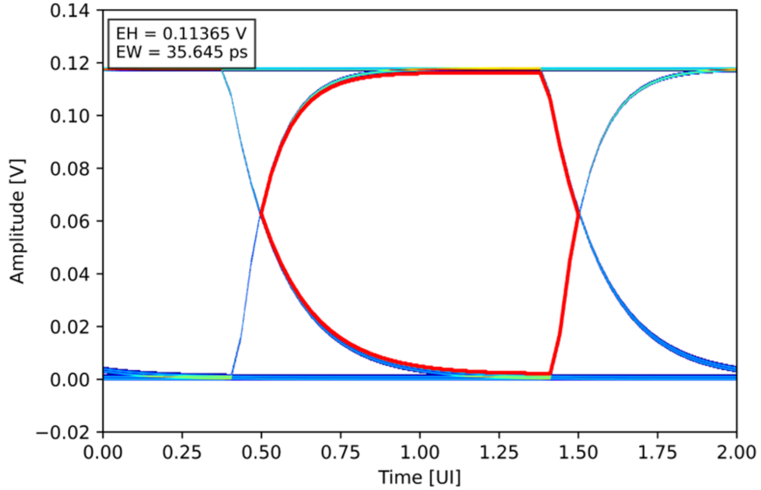
Validation – 28 Gbps / 1V / MIN



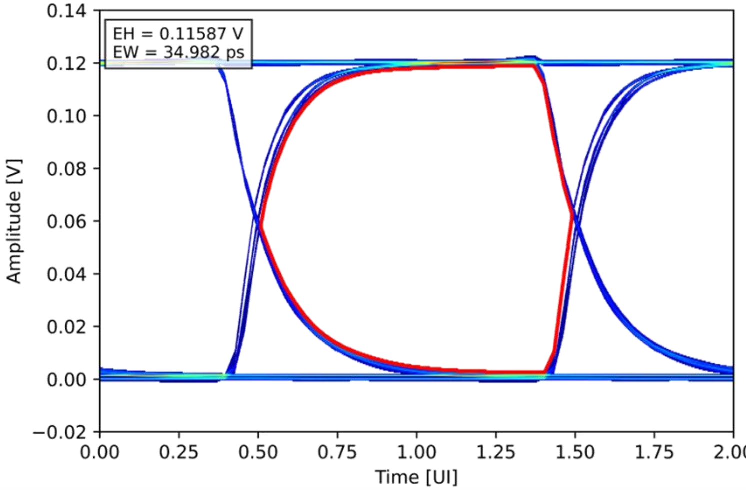
	28 Gbps / 1V / MIN				Time Cost [sec]
	EH [V]		EW [psec]		
Original	0.114		35.64		-
Transformer	0.116	1.75%	34.98	-1.85%	33.12
Extracted IR (LTI)	0.113	-0.88%	35.47	-0.48%	29.14

* Training time : 7 h 32 m

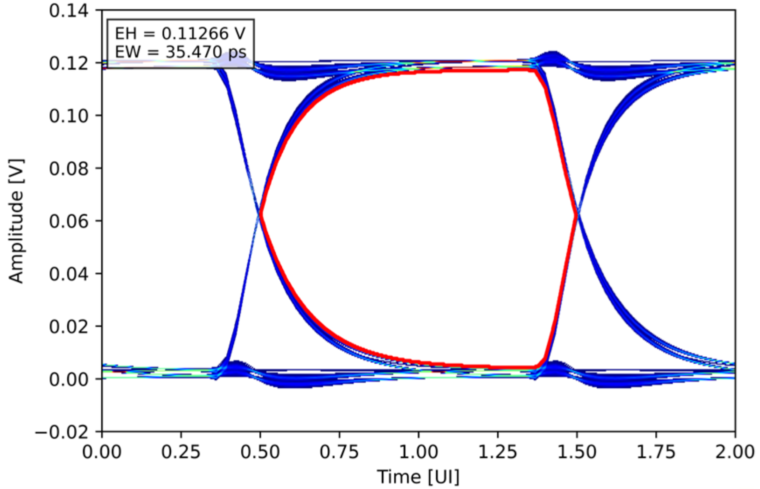
< Original >



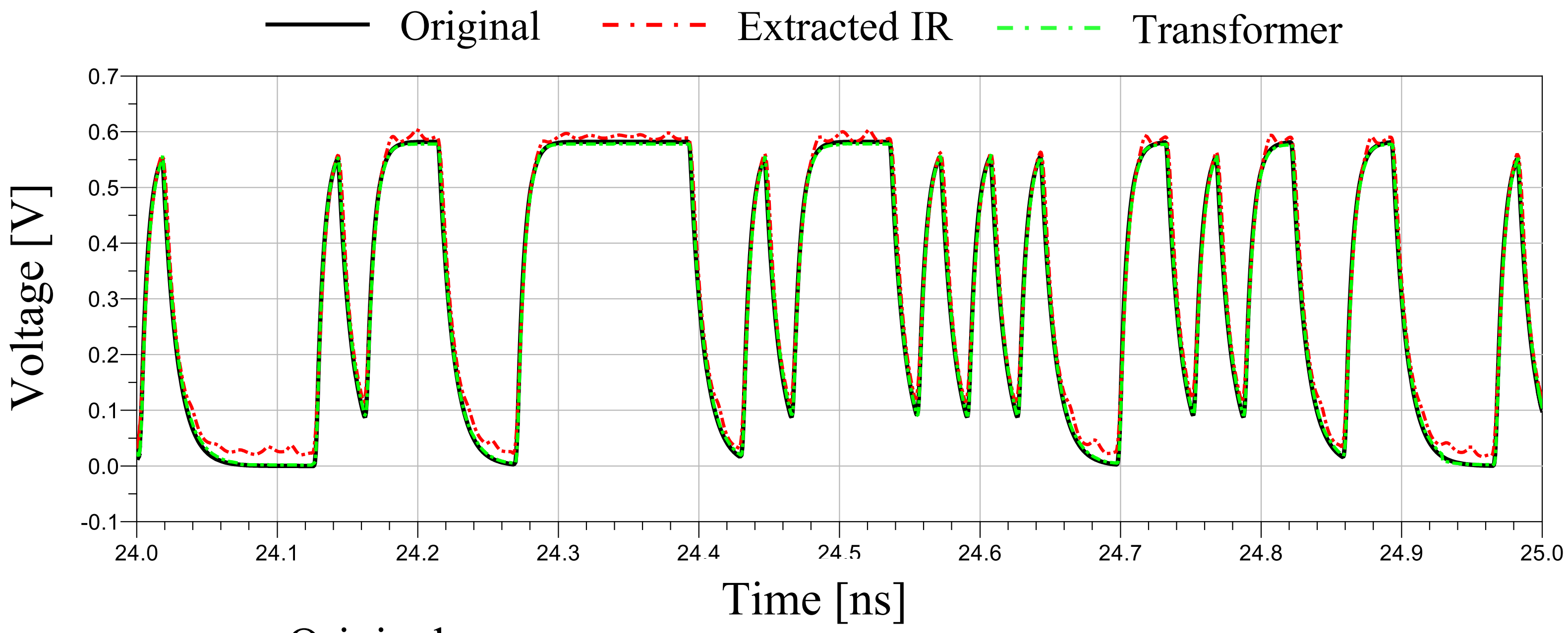
< Transformer >



< Extracted IR >



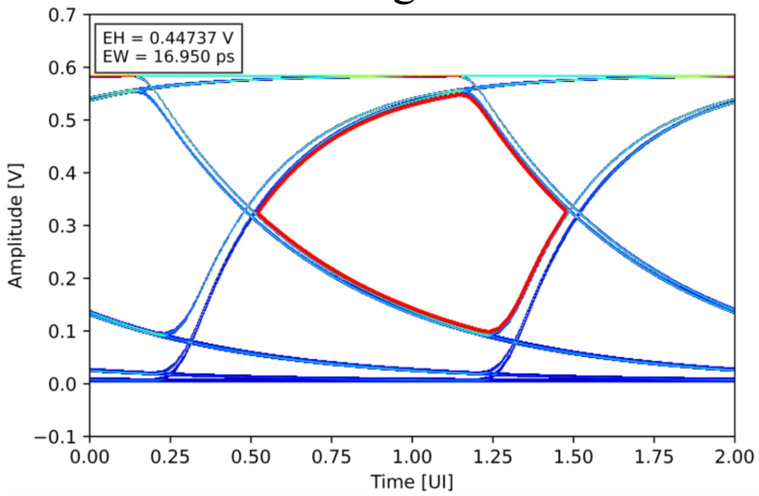
Validation – 56 Gbps / 2V / TYP



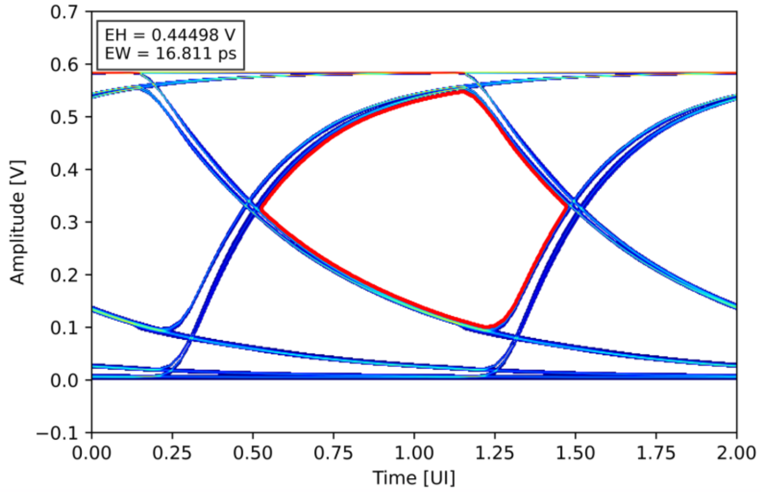
	56 Gbps / 2V / TYP				Time Cost [sec]
	EH [V]		EW [psec]		
Original	0.447		16.95		-
Transformer	0.445	-0.45%	16.81	-0.83%	33.59
Extracted IR (LTI)	0.412	-7.83%	16.46	-2.89%	28.29

* Training time : 7 h 32 m

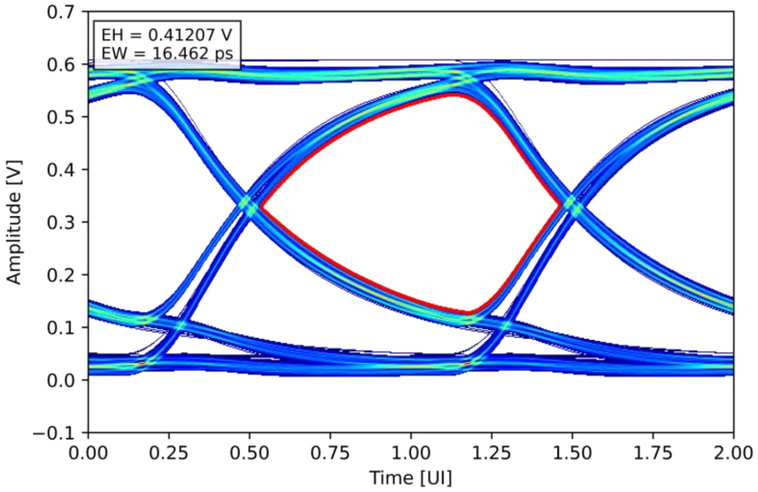
< Original >



< Transformer >

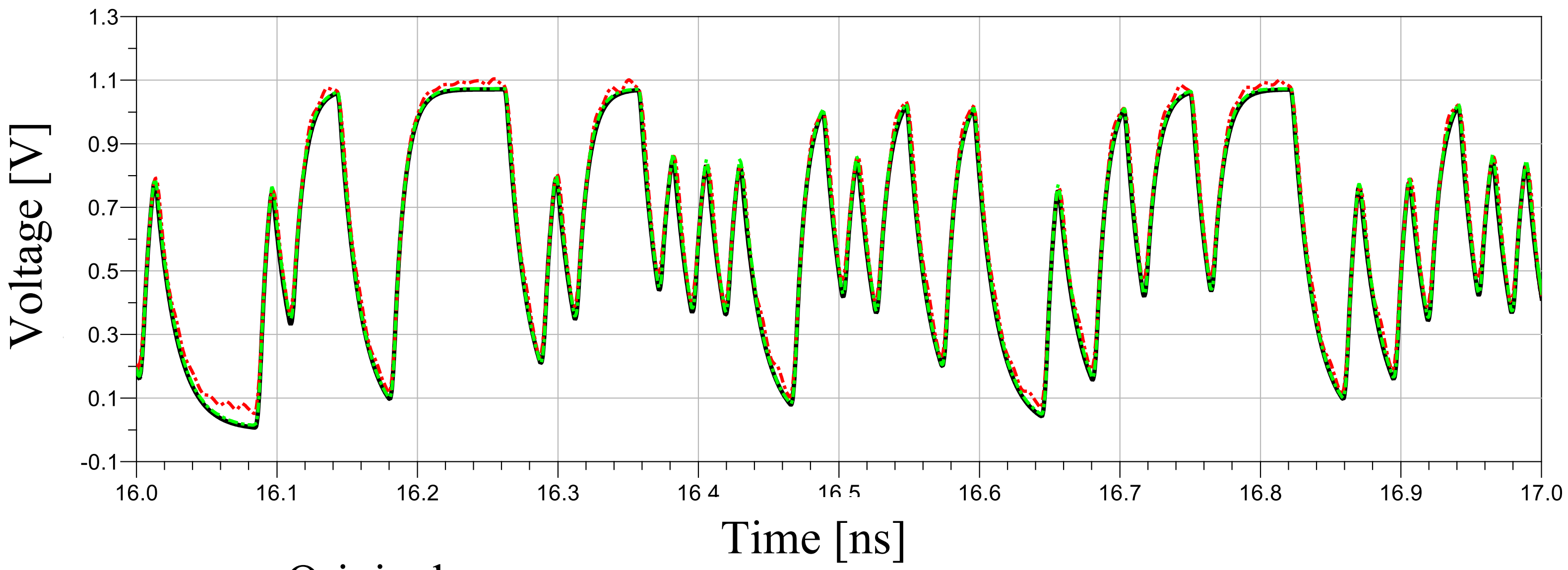


< Extracted IR >



Validation – 84 Gbps / 3V / MAX

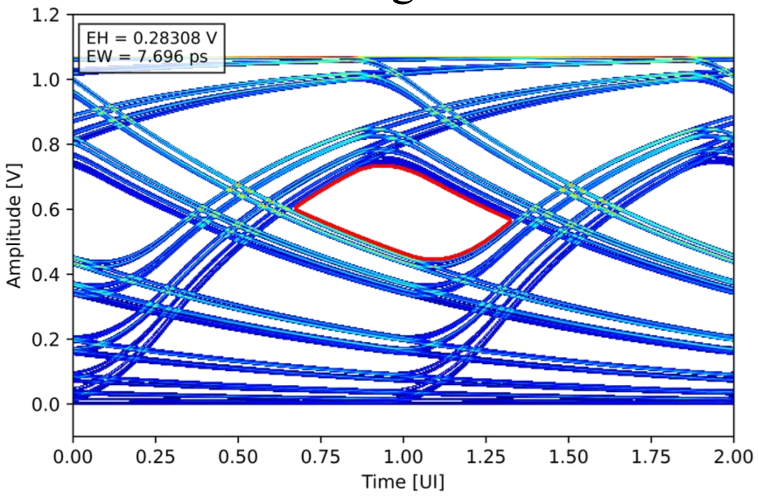
*All waveform extracted by simulator



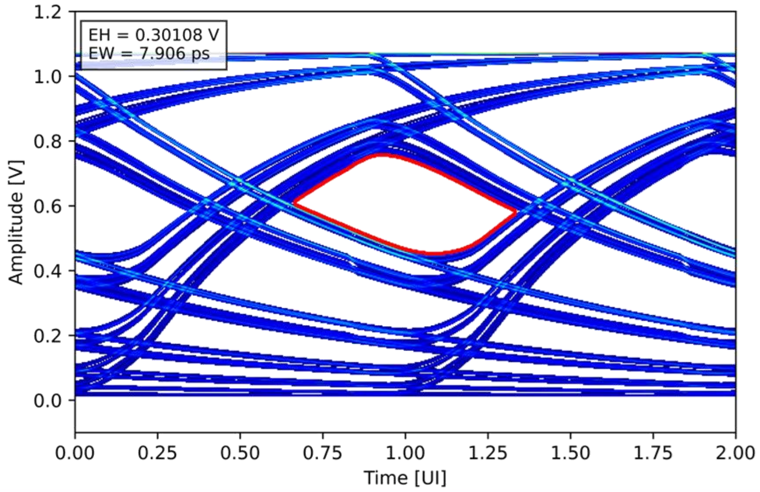
	84 Gbps / 3V / MAX				Time Cost [sec]
	EH [V]		EW [psec]		
Original	0.283		7.70		-
Transformer	0.301	6.36%	7.91	2.73%	31.02
Extracted IR (LTI)	0.235	-17.0%	7.30	-5.19%	29.80

* Training time : 7 h 32 m

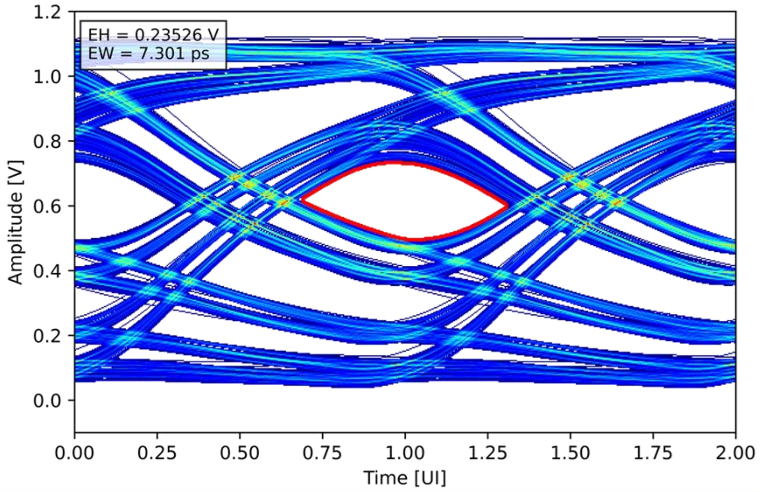
< Original >



< Transformer >



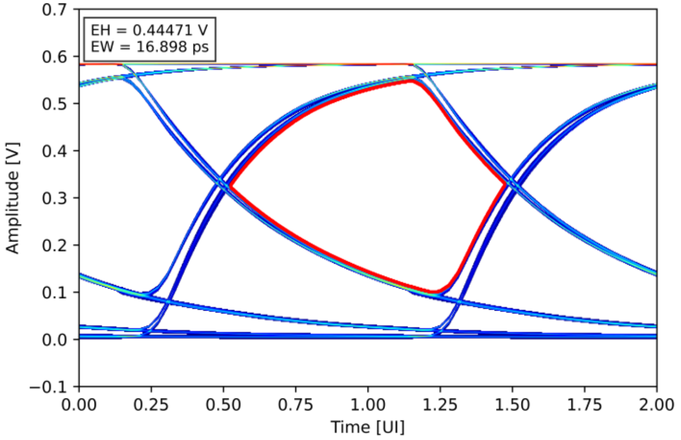
< Extracted IR >

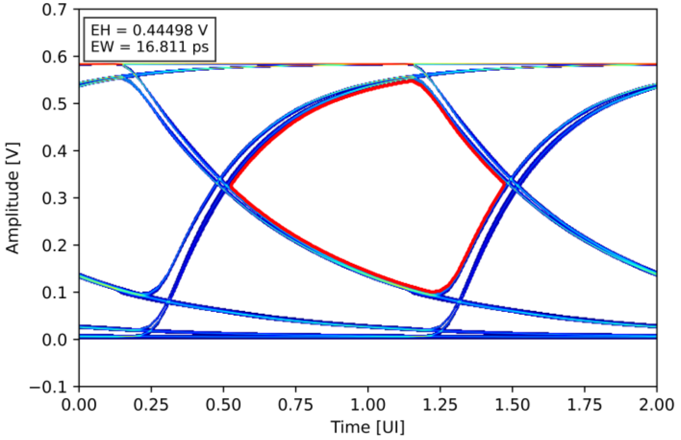


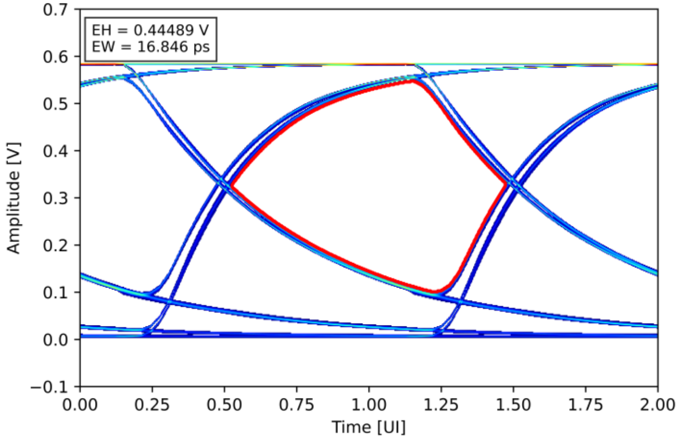
Validation – Un-trained Data : PRBS11 - 31

< PRBS11 – Un-train data >　< PRBS15 – Train data >　< PRBS31 – Un-train data >

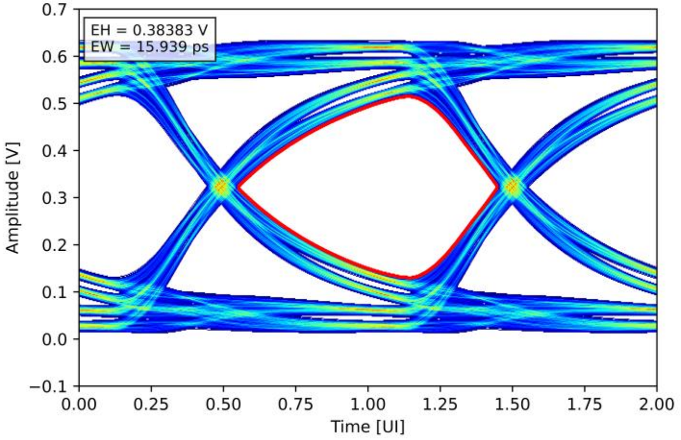
< Transformer >

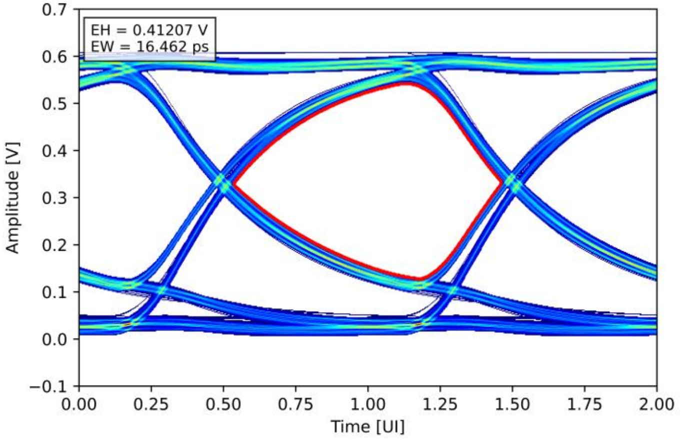


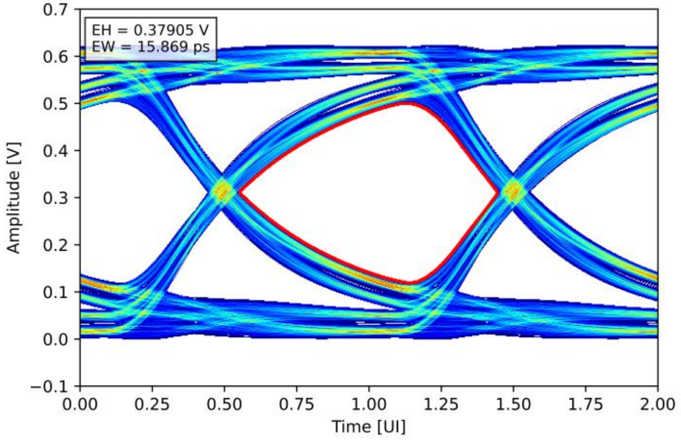




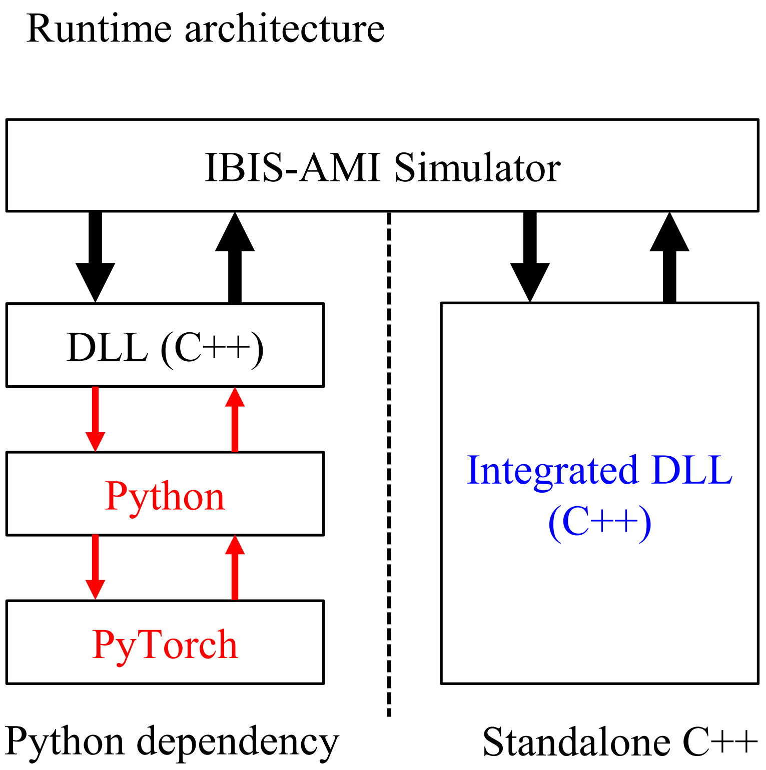
< Extracted IR >

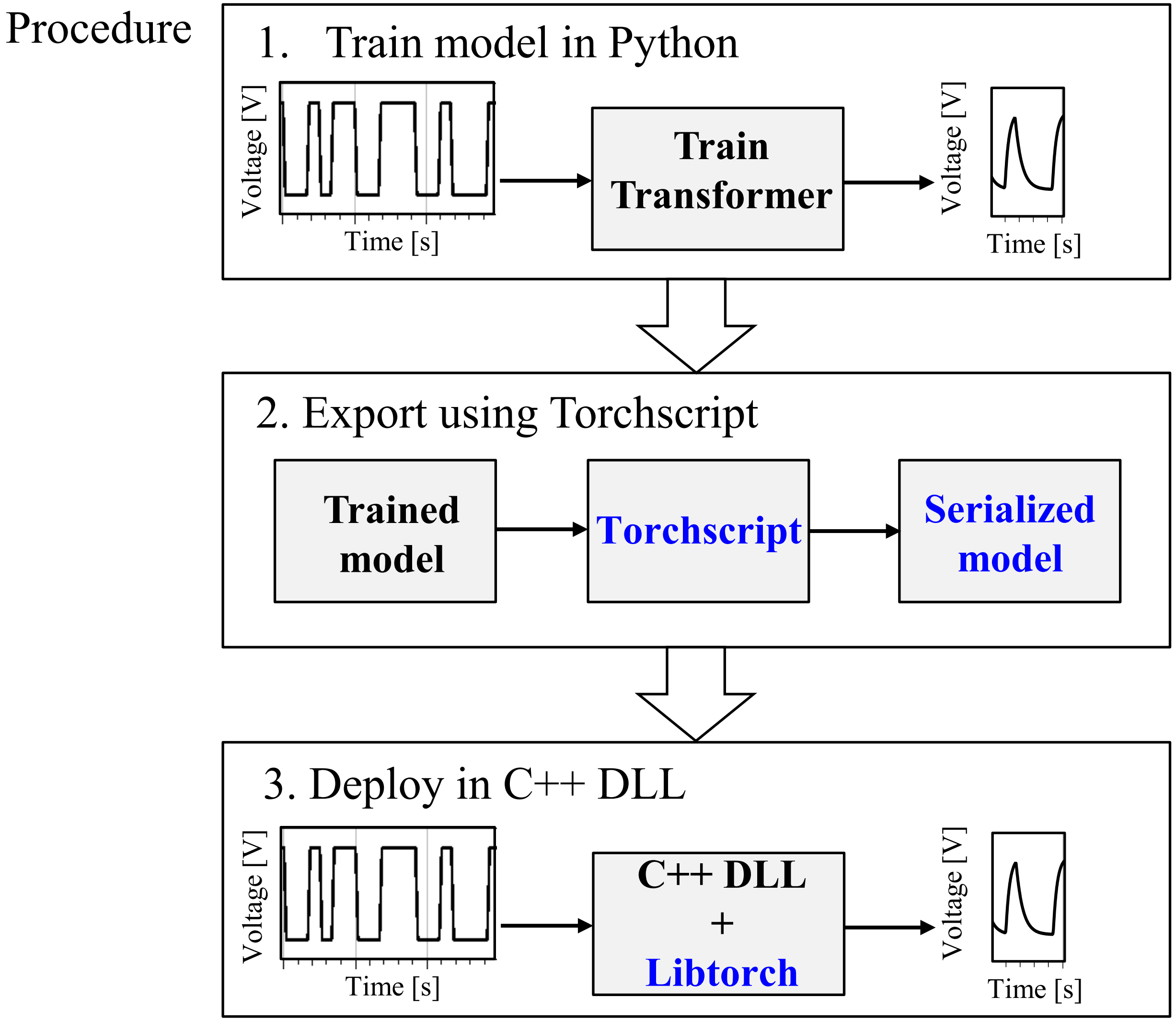






Deploying Transformer in C++





Conclusions

- Proposed a transformer-based IBIS-AMI simulation method
  - Nonlinear characteristic of driver was modeled using transformer network
  - A transformer model was implemented in IBIS-AMI simulation

References

- IBIS Open Forum Committee, “I/O Buffer Information Specification (IBIS) Version 5.0”, August 2008, https://ibis.org/ver5.0/ver5_0.ibs
- S. Sun et al., "LiTformer: Efficient Signal Integrity Analysis for High-Speed Link Transmitters Using Non-Autoregressive Transformer," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Early Access)
- S. Soleimani, S. Alireza Sadrossadat, W. Na and Q. -J. Zhang, "Attention Mechanism Combined With Deep Recurrent Network for Nonlinear Circuit Macromodeling," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 72, no. 9, pp. 4810-4819, Sept. 2025
- A. Vaswani et al., “Attention is all you need,” in Advances in Neural Information Processing Systems 30, 2017, pp. 5998–6008
- Ju, Yue, Alka Isac, and Yimin Nie. "Chunkformer: learning long time series with multi-stage chunked transformer." arXiv preprint arXiv:2112.15087 (2021).

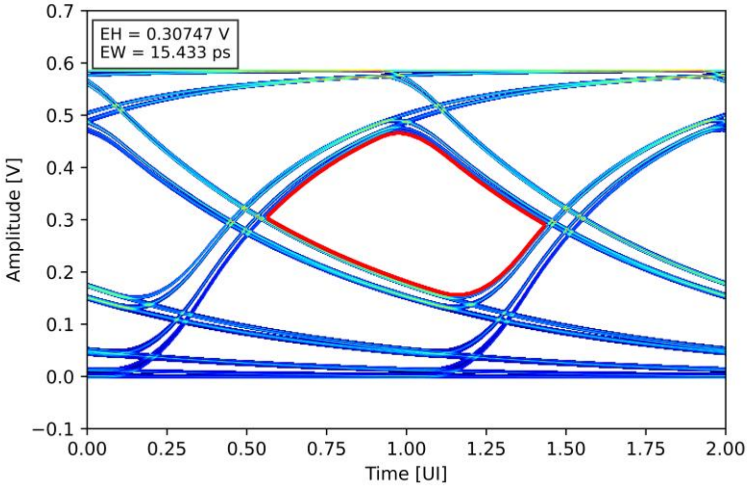
Hyperparameter Set-up

Parameter		Value
Encoder	Input dim d_x	320
	Embed dim d_h	128
	Head, key, value dim M, d_k, d_v	4, 32, 32
	FF dim d_{ff}	512
	Global info. dim	3
Decoder	Input dim d_x	96
	Embed dim d_h	128
	Head, key, value dim M, d_k, d_v	4, 32, 32
	FF dim d_{ff}	512
	Chunk info. dim	8

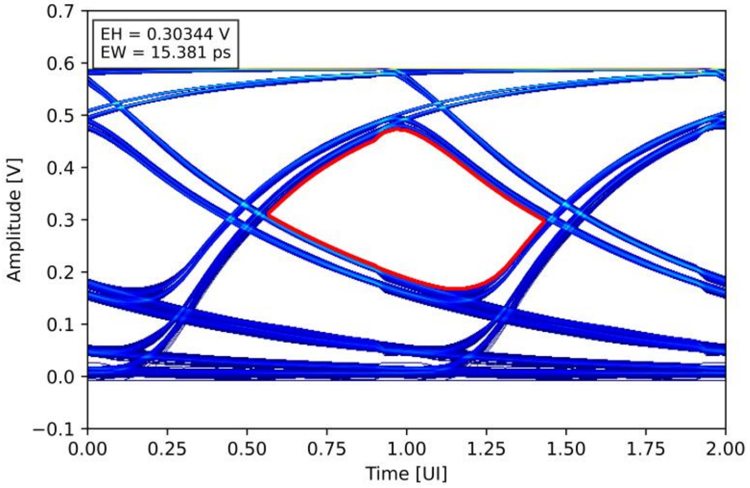
Parameter		Value
Training	Train epoch #	400
	Step per epoch	2048
	Training epoch size	22400
	Validation size	3200
	Initial learning rate	2e-4
	Loss function	Adam

Chunk Information Effect

< Original >



< Baseline >



< Proposed >