Hybrid IBIS Summit at IEEE EMC + SIPI 2026

August 6, 2026

EMC+ SIPI 2026

DALLAS, TEXAS

IBIS-AMI Modeling of Re-driver Circuits via Deconvolution-based Impulse Response Extraction

Sanguk Lee, KAIST EMC Lab

Speaker: Sanguk Lee

Sanguk Lee

Ph.D student, Korea Advanced Institute of Science and Technology (KAIST)
sang960326@kaist.ac.kr

Sanguk Lee received his B.S. degree from Inha University, Incheon, South Korea, in 2021, and the M.S degree from the Cho Chun Shik Graduate School of Mobility, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2023.
He is currently pursuing the Ph.D. degree with KAIST.

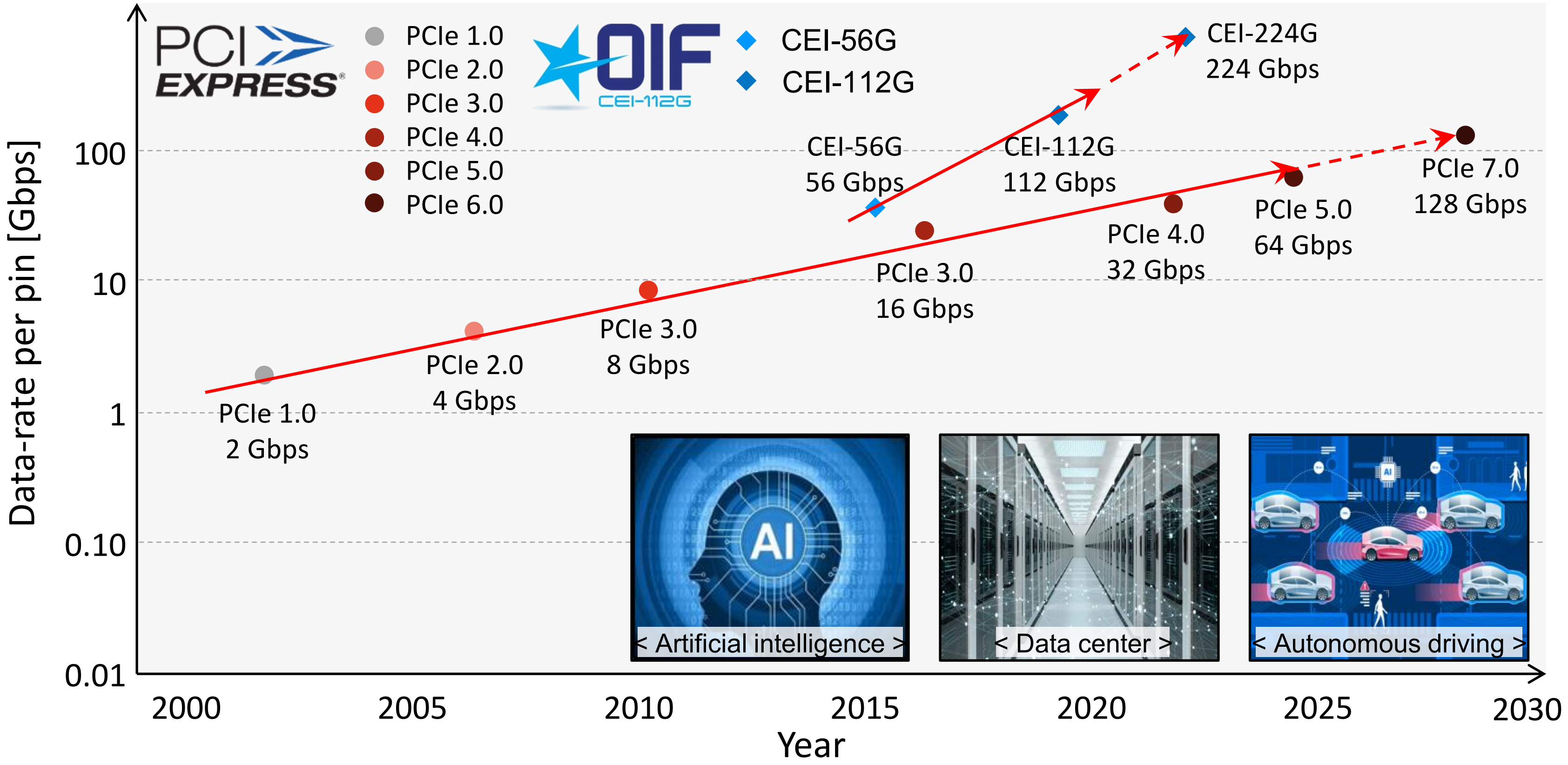
Research interest: Signal and power integrity (SI/PI) design and analysis of HPC System, Passive/Active Components Modeling for Electromagnetic Compatibility Analysis

Contents

Contents

Evolution of High-speed Signaling Protocols

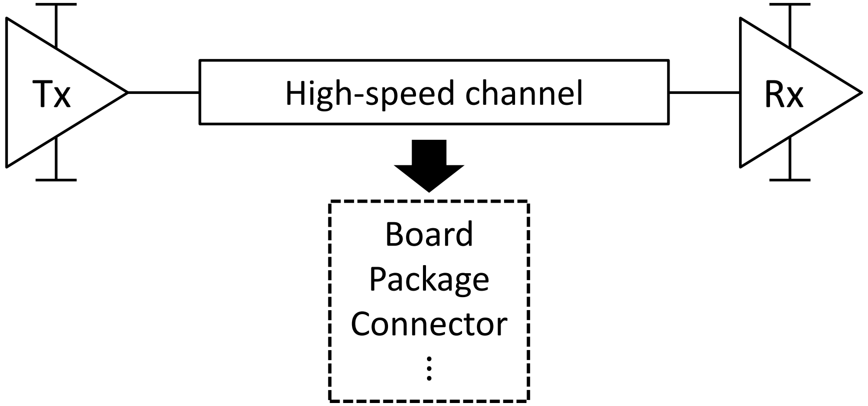
*PCIe: Peripheral component interconnect express
**CEI: Common Electrical Interface

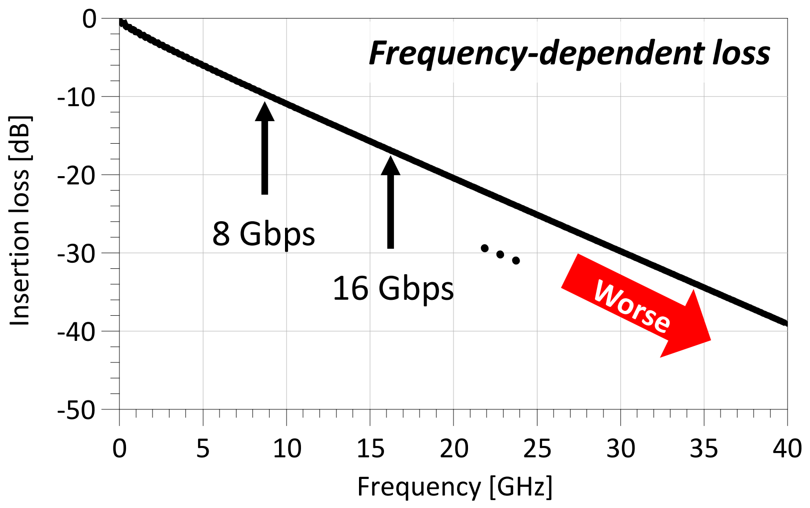


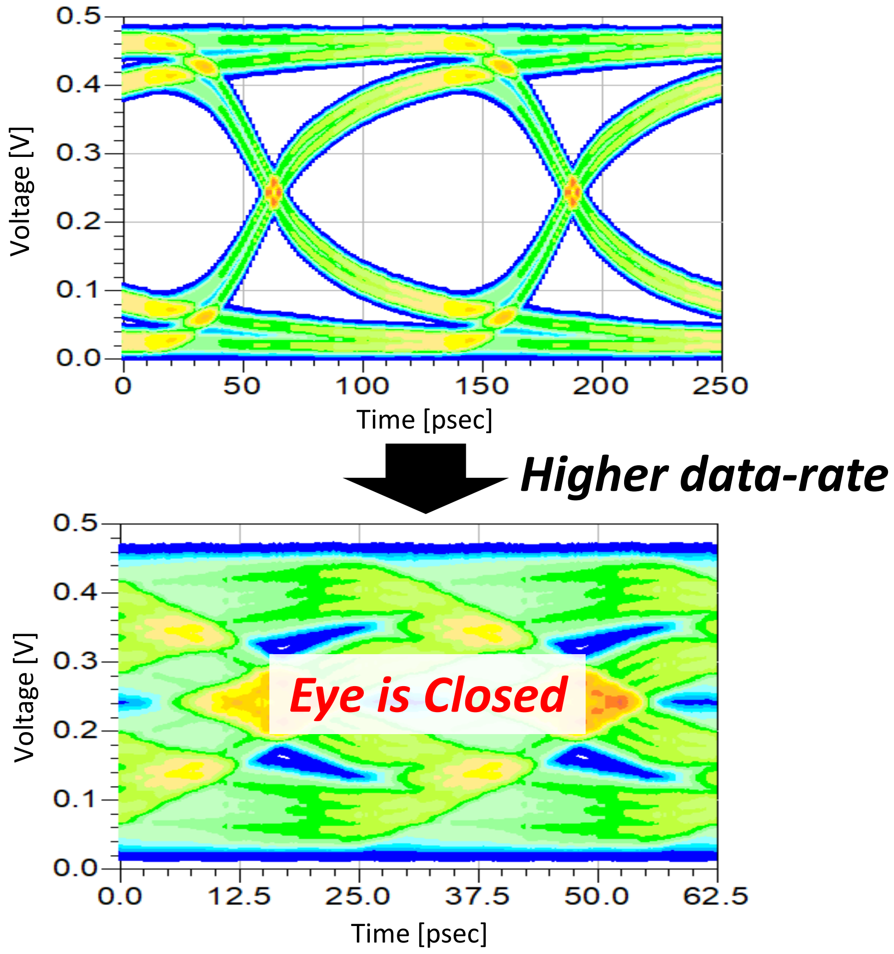
<Data-rate per pin for SerDes over years>

- The per-pin data-rate for high-speed signaling protocol has doubled with each generation and is expected to continue increasing.

Signal Integrity Challenges in High-speed Channel

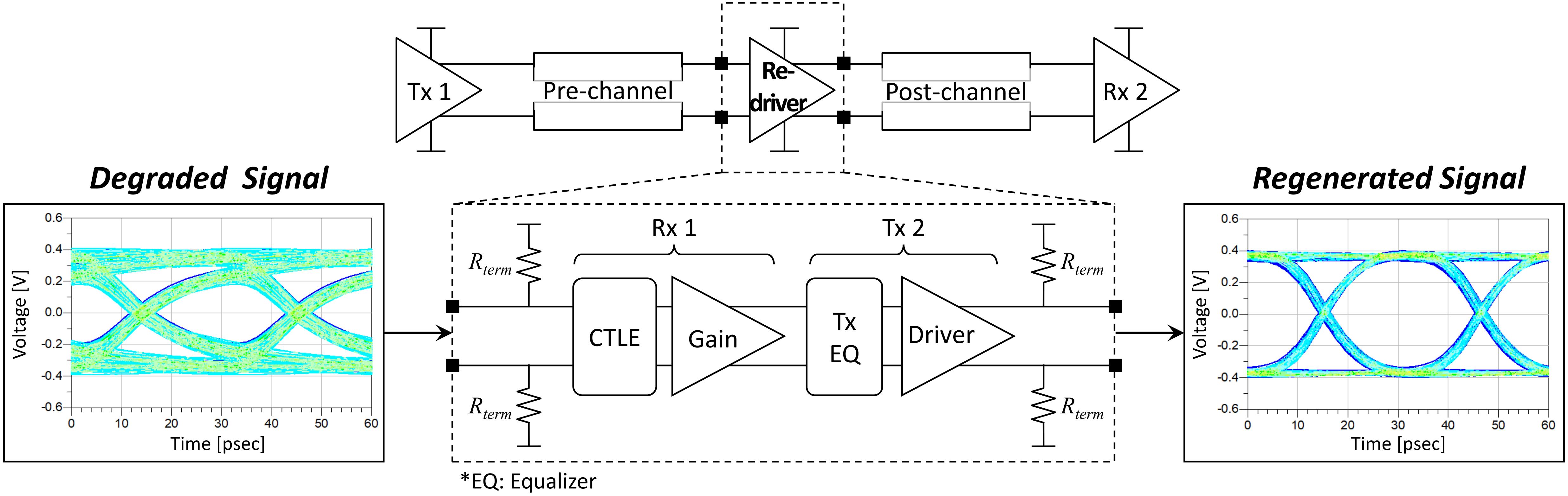






- As the data rate increases, conductor loss and dielectric loss increase, causing the eye to close.

Introduction of Re-driver

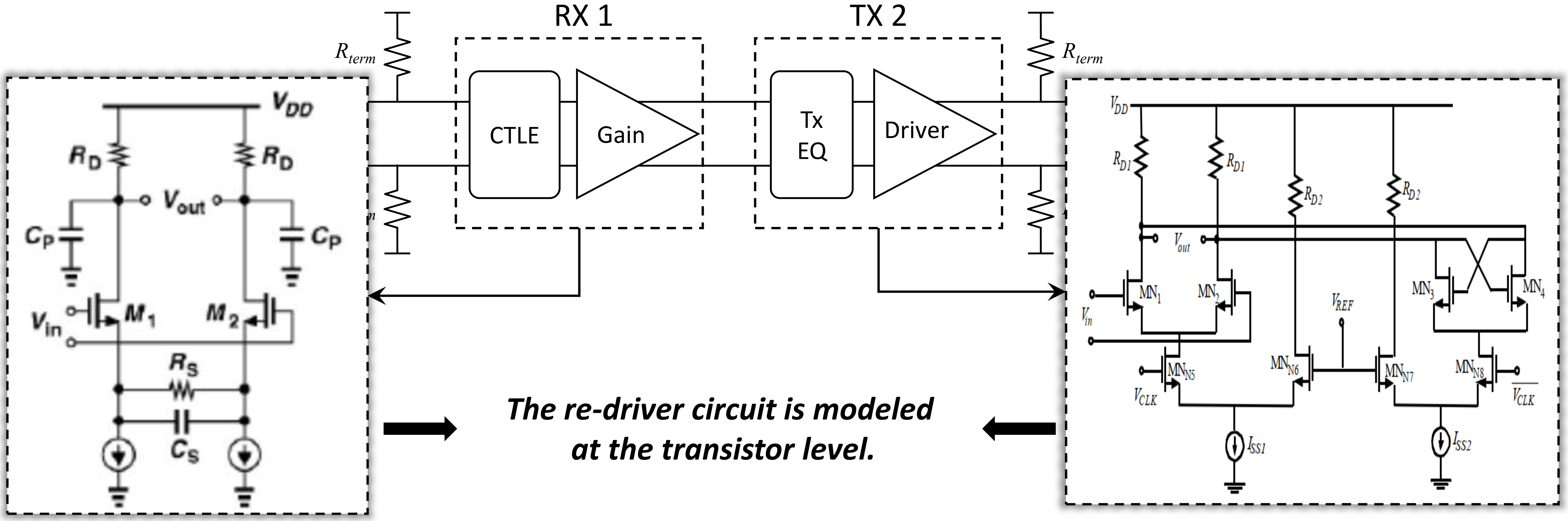


<Re-driver circuit configuration>

- To address these SI issues, repeaters (e.g., redrivers and retimers) are employed to compensate for channel loss and secure SI margins [Ref].

[Ref] Samaan, Samie B., Dan Froelich, and Samuel Johnson. "High-speed Serial Bus Repeater Primer." *Intel Corporation,* 2015.

Need for Transistor-Level Re-Driver Modeling for End-to-End Link Analysis

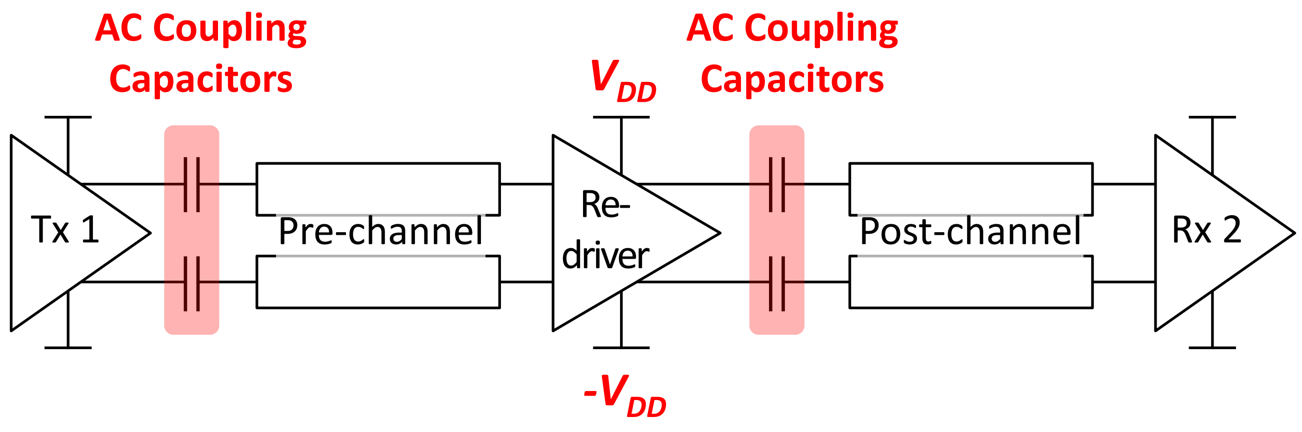


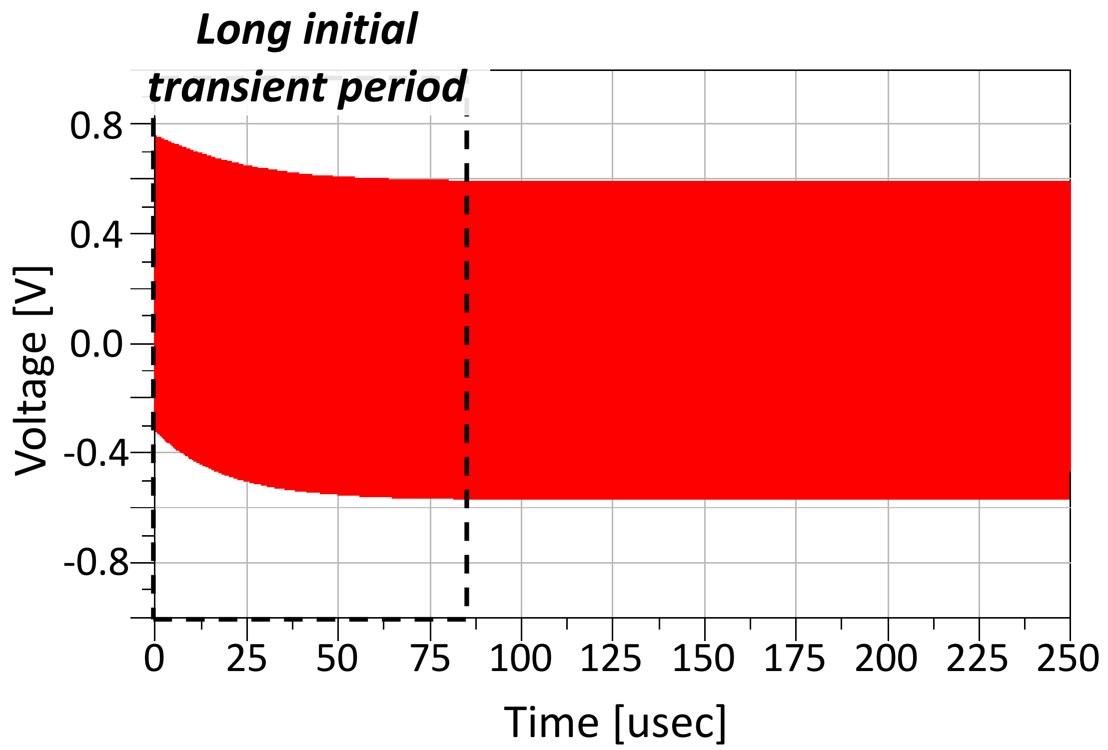
<Transistor-level implementation of the re-driver [Ref.]>

- Accurate end-to-end link analysis requires transistor-level modeling of the re-driver circuit to capture the circuit-level behavior of its internal RX and TX stages.

[Ref] Heydari, Payam, and Ravi Mohavavelu. "Design of ultra high-speed CMOS CML buffers and latches." *2003 IEEE International Symposium on Circuits and Systems (ISCAS)*. Vol. 2. IEEE, 2003.

Long Initial Transient Period in Transistor-Level Simulation



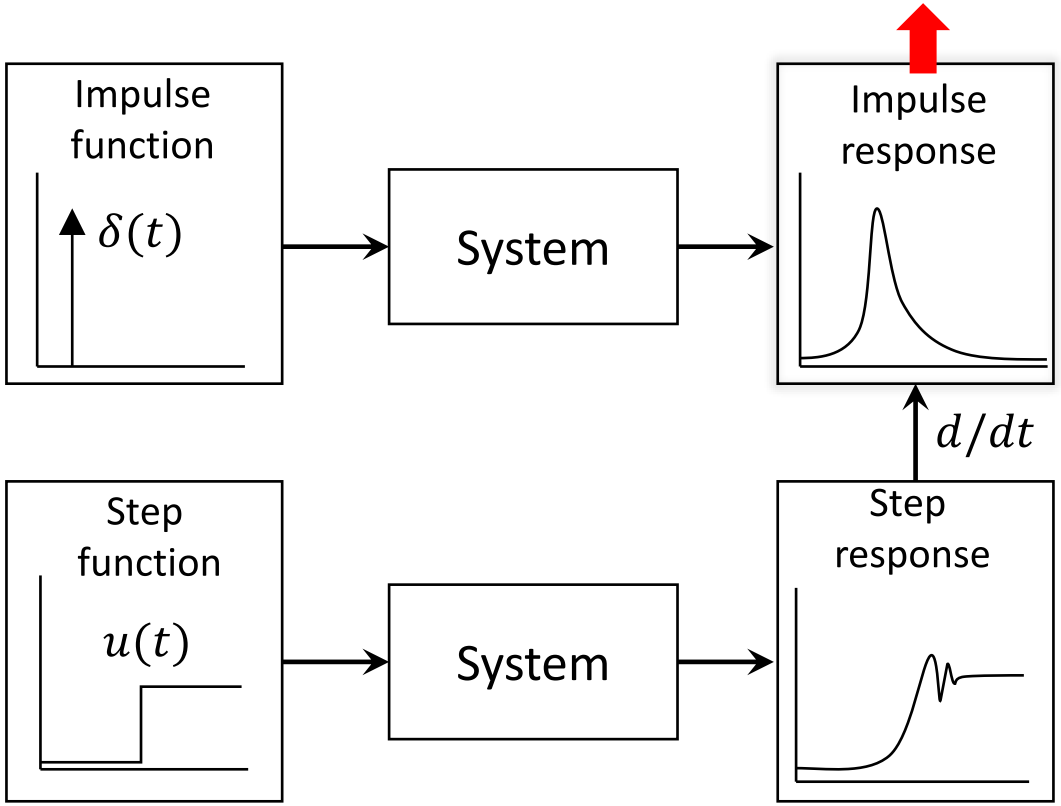


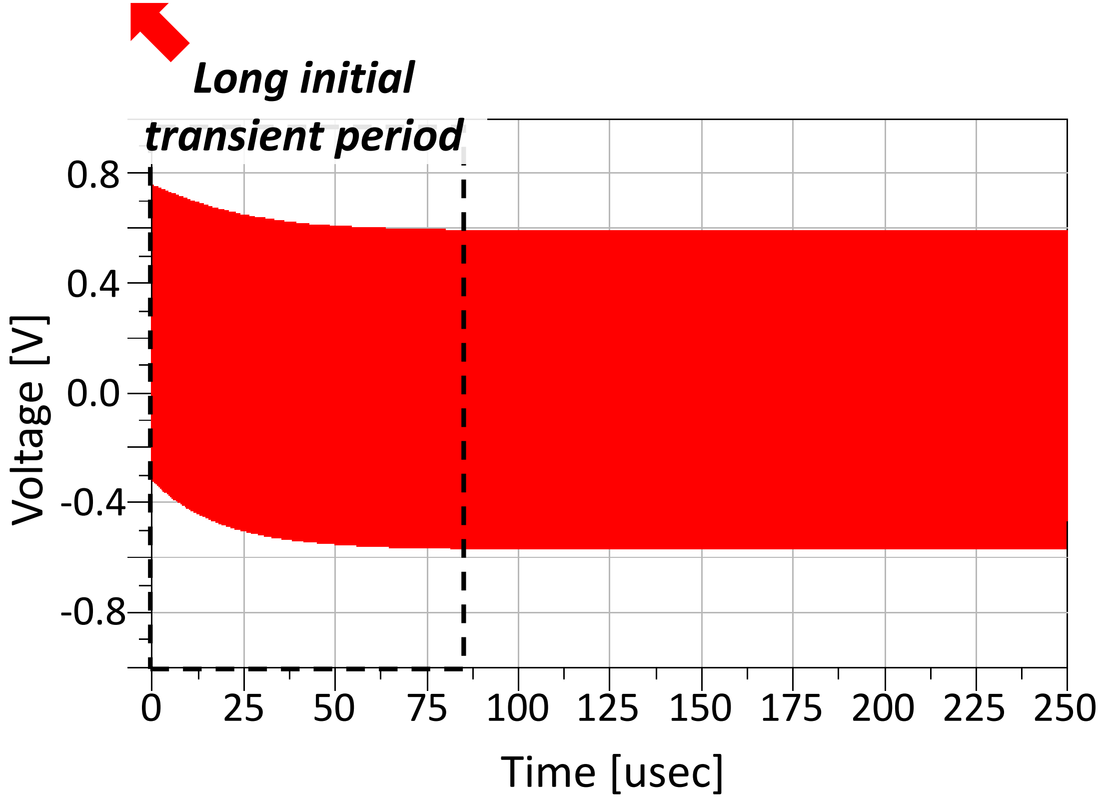
<Long initial transient response caused by AC coupling capacitors and DC biasing>

- The large time constants due to the AC coupling capacitors and DC biasing circuits result in an extremely long initial transient time spanning tens of thousands of bit intervals, which is required to reach steady state.

Challenges in Impulse Response (IR) Extraction

Inaccurate due to long transient time





<Procedure for extracting IR>

- While convolution-based simulators enable fast system-level SI analysis, they cannot accurately represent the behavior of redriver because its impulse response cannot be extracted from transistor-level simulation owing to the extremely long initial transient time.

Research Motivation

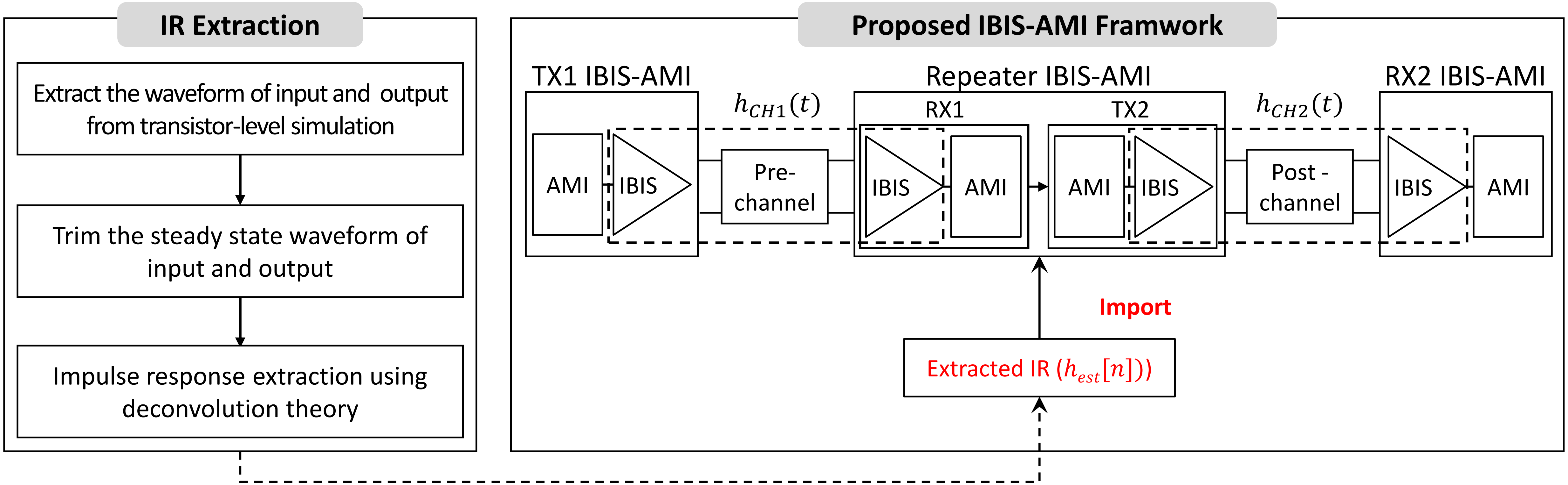
- The continuous increase in the data rate of high speed signaling protocols aggravates frequency-dependent channel loss and significantly reduces SI margins.
- Re-drivers are employed to compensate for signal degradation and regenerate the transmitted waveform.
- Accurate end-to-end link analysis requires the transistor-level circuit modeling of both the RX and TX within the re-driver.
- However, transistor-level simulations exhibit extremely long initial transients due to AC coupling capacitors and DC biasing networks.
- These long settling times make simulations prohibitively slow and hinder IR extraction, limiting fast convolution-based system-level simulations.

Research Objectives

- **Propose** an IBIS-AMI model for the re-driver circuit using deconvolution-based IR extraction.
- **Verify** the extracted IR by reconstructing the output voltage through convolution with the input voltage.
- **Validate** the proposed IBIS-AMI model by comparing eye diagrams with transistor-level simulation results.

Contents

Proposed IBIS-AMI Modeling via Deconvolution-based IR Extraction



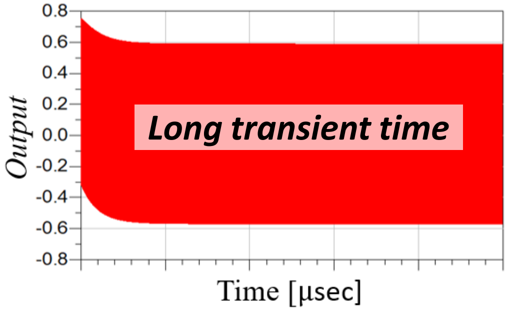
<Proposed IBIS-AMI framwork>

- The IR of re-driver is extracted from its input and output waveforms using deconvolution theory.
- The extracted IR is then imported into the TX2 AMI model and convolved with the RX1 output to reproduce the re-driver behavior.

Advantages of the Proposed IBIS-AMI Modeling Method

Advantage 1: Fast Simulation with Transistor-level Accuracy

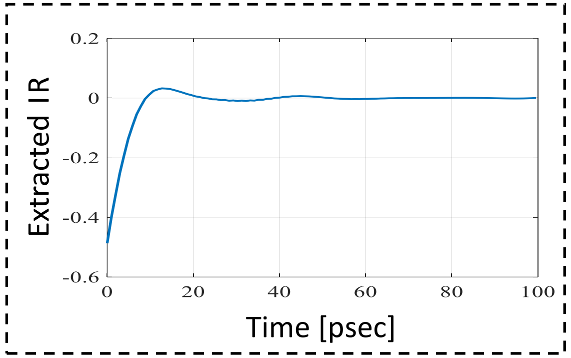
Transistor-level sim



Sim. time: Several hours

IR Extraction

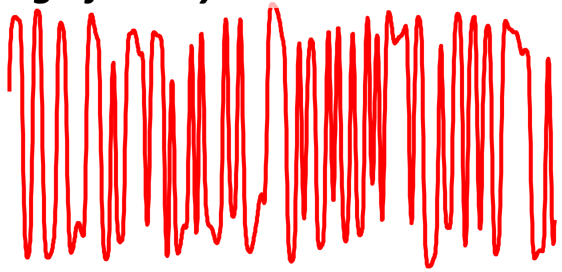
(One-time process)



Proposed IBIS-AMI

(Convolution)

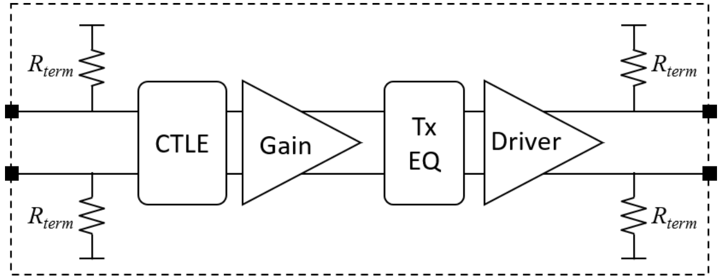
Significantly Reduced Sim. Time



Sim. time: Several minutes

Advantage 2: Black-Box Modeling without Internal Circuit Information

Transistor-level sim

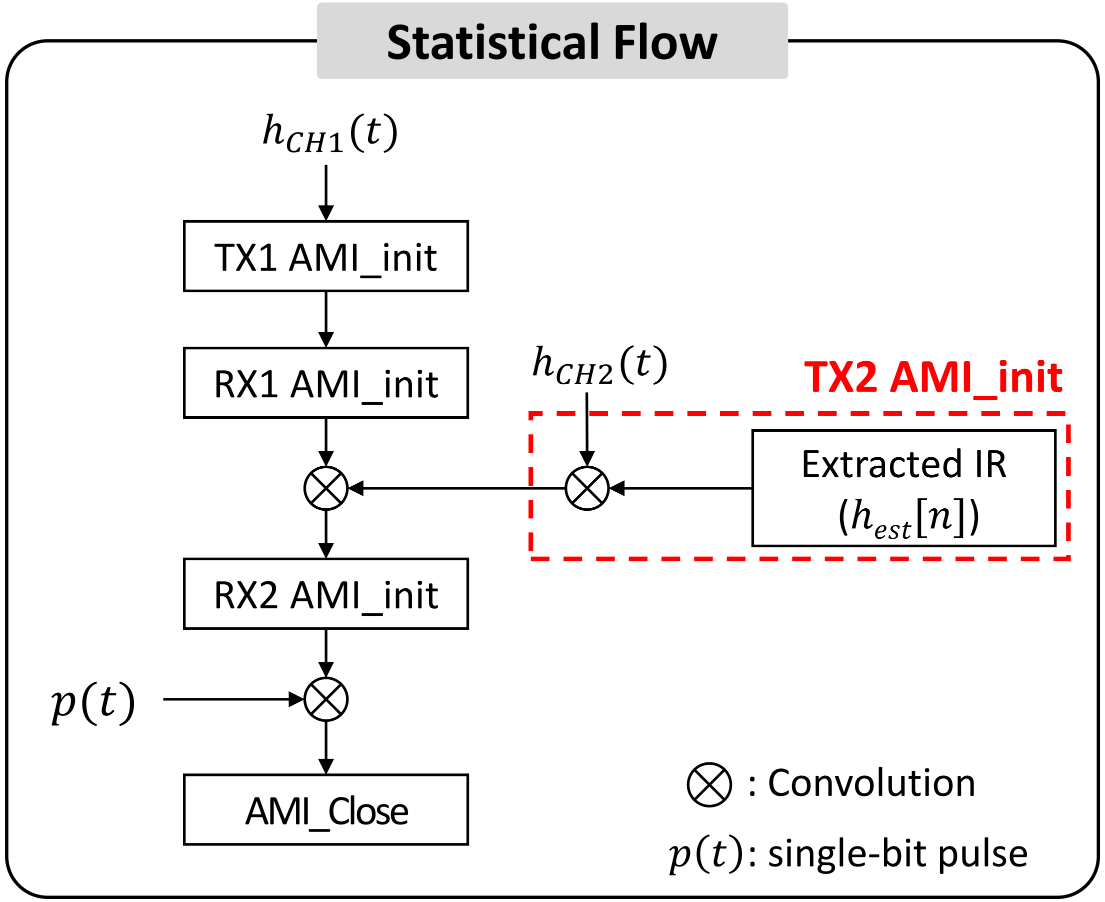


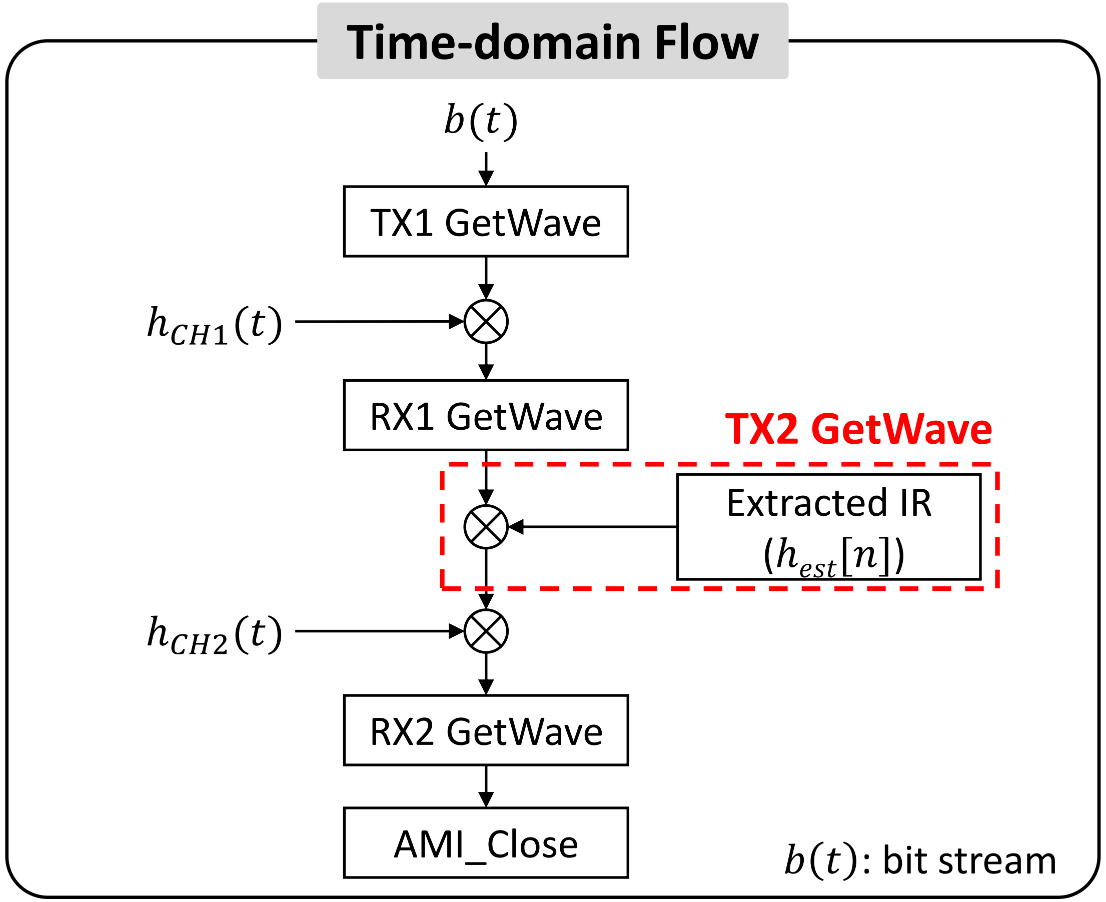
Circuit topology and device parameters required

Proposed IBIS-AMI

Only Input/Output Waveforms Required

Flow Chart of Proposed IBIS-AMI Model





- The proposed method is applicable to both statistical and time-domain modes, as shown in the flowchart above.

Least-squares Deconvolution (1/2)

Convolution

$x[n] \longrightarrow \boxed{h[n]} \longrightarrow y[n]$

$$y[n] = x[n] * h[n]$$

- $x[n]$: Input voltage
- $y[n]$: Output voltage
- $h[n]$: Impulse response

Matrix Form

$$\mathbf{y} = \mathbf{X} \cdot \mathbf{h}$$

$$\mathbf{y} = [y[0], y[1], \cdots, y[L_x + L_h - 2]]^T$$

$$\mathbf{h} = [h[0], h[1], \cdots, h[L_h - 1]]^T$$

$$\mathbf{X} = \begin{bmatrix} x[0] & 0 & \cdots & 0 \\ x[1] & x[0] & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ x[L_x - 1] & x[L_x - 2] & \cdots & x[L_x - L_h] \\ 0 & x[L_x - 1] & \cdots & x[L_x - L_h - 1] \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & x[L_x - 1] \end{bmatrix}$$

IR Extraction

$$\mathbf{X}^T\mathbf{X} \cdot \mathbf{h}_{est} = \mathbf{X}^T \mathbf{y}$$

$$\Downarrow$$

$$\mathbf{h}_{est} = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T \mathbf{y}$$

- $\mathbf{h}_{est}$: Extracted IR

- Deconvolution refers to the inverse problem of determining the IR ($h[n]$) from known input signal ($x[n]$) and output signal ($y[n]$) for a linear time-invariant (LTI) system [Ref].

[Ref] I. Selesnick, "Least squares with examples in signal processing," *Connexions*, vol. 4, pp. 1-25, 2013.

Least-squares Deconvolution (2/2)

Regularization

$$\mathbf{h}_{est} = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T \mathbf{y}$$

$\mathbf{X}^T\mathbf{X}$ is ill-conditioned ⇒ Noise amplification

$$\mathbf{h}_{est} = (\mathbf{X}^T \mathbf{X} + \lambda \mathbf{I})^{-1} \mathbf{X}^T \mathbf{y}$$

- λ is too small → Insufficient noise suppression
- λ is too large → IR distortion in peak value

Selection of Estimated IR Length

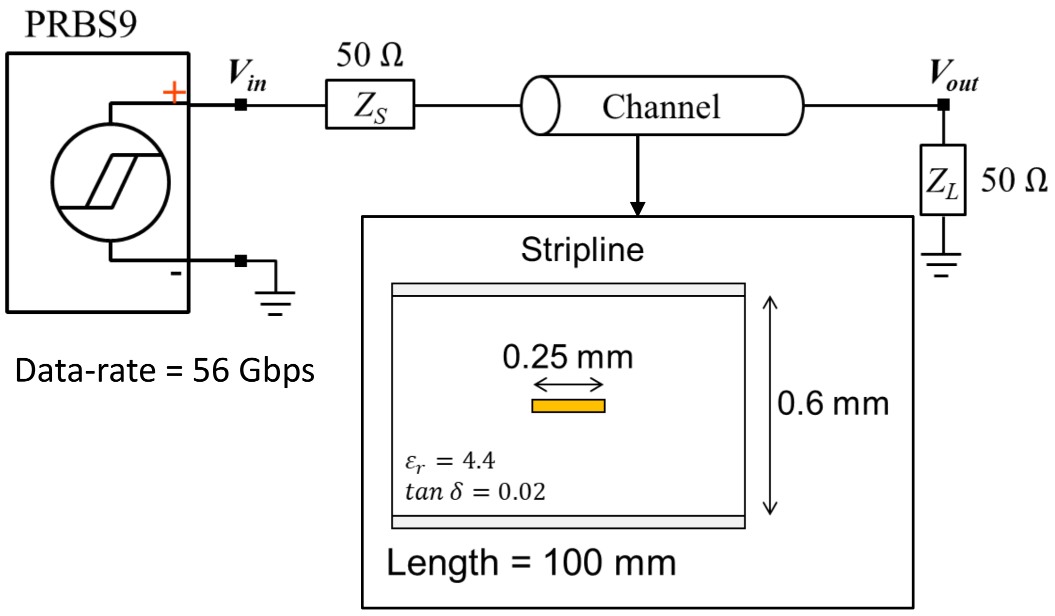
$$\sum_{k=0}^{L_{h,trunc}} |h_{est}[k]|^2 \geq 0.999 \sum_{k=0}^{L_{h,est}-1} |h_{est}[k]|^2$$

✓ $L_{h,trunc}$ is selected to retain at least 99.9% of the total energy of the estimated IR.

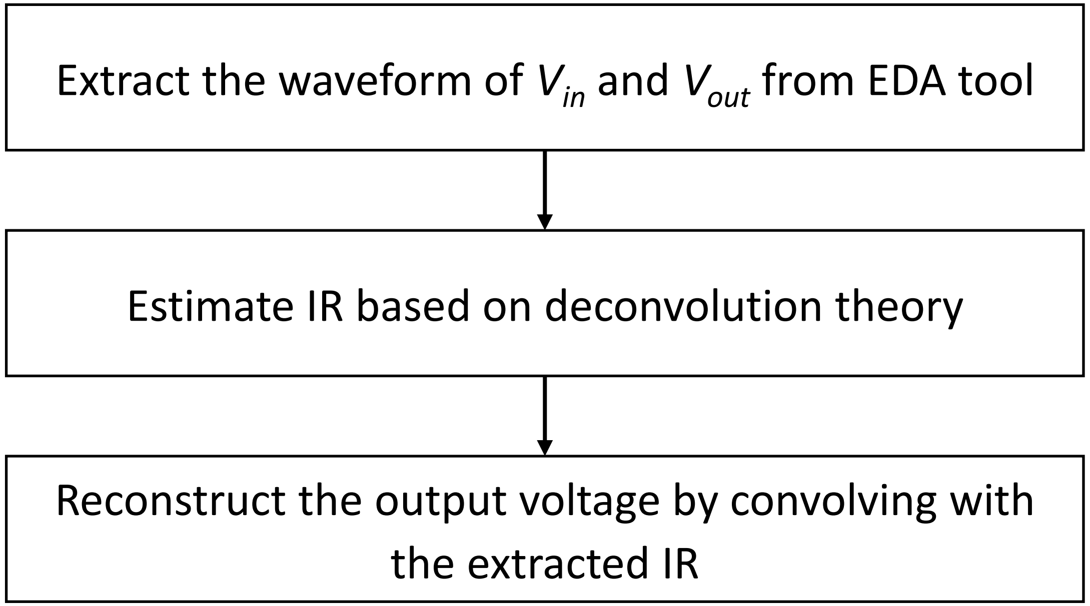
- $L_{h,est}$ is too short → Fail to capture the overall system response
- $L_{h,est}$ is too long → Overfitted to the specific intput-output

- To extract the IR stably and accurately, regularization is employed to suppress noise amplification caused by the ill-conditioned matrix.
- The estimated IR length is then selected to retain at least 99.9% of its total energy.

Validation of Deconvolution Theory



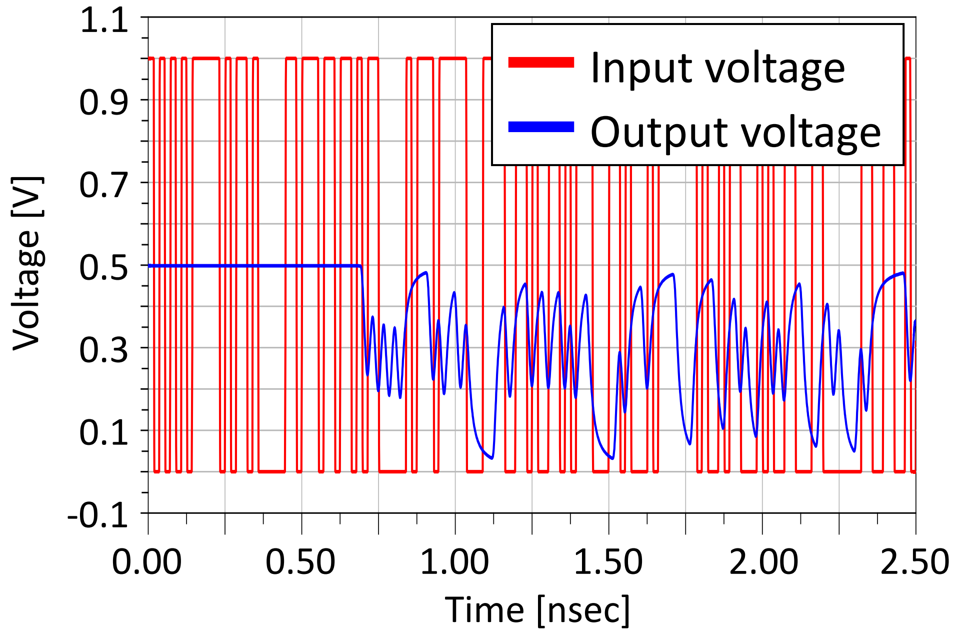
<Simulation setup for validation>



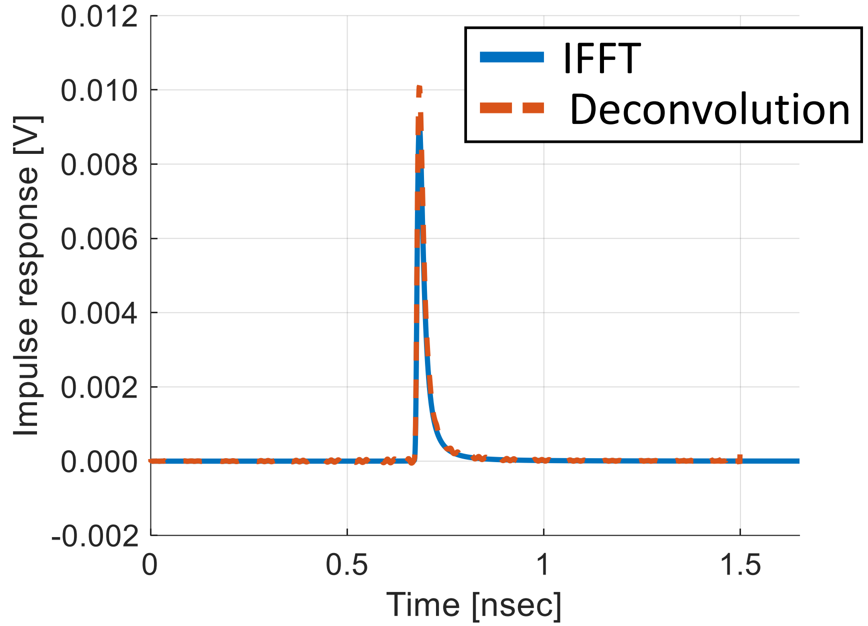
<Validation process>

- To validate the deconvolution theory, the IR is estimated from the simulated input and output waveforms and then used to reconstruct the output voltage through convolution.

Validation Results – Comparison of IR



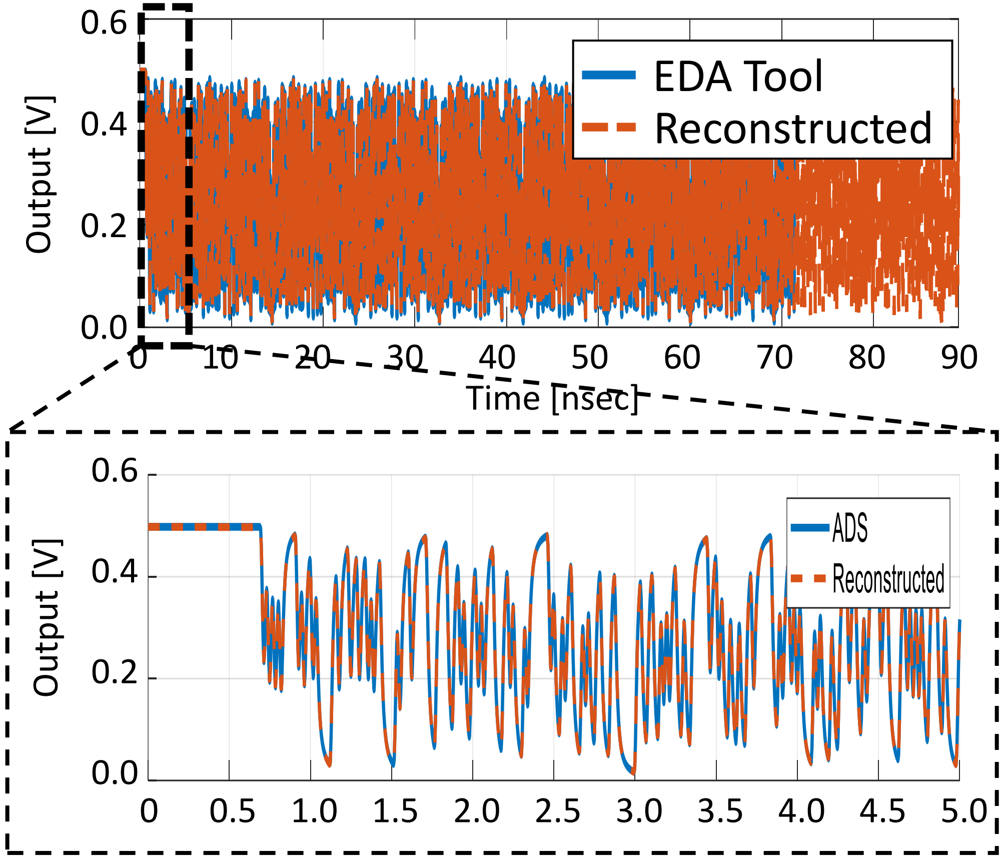
<Intput/output voltage for deconvolution>

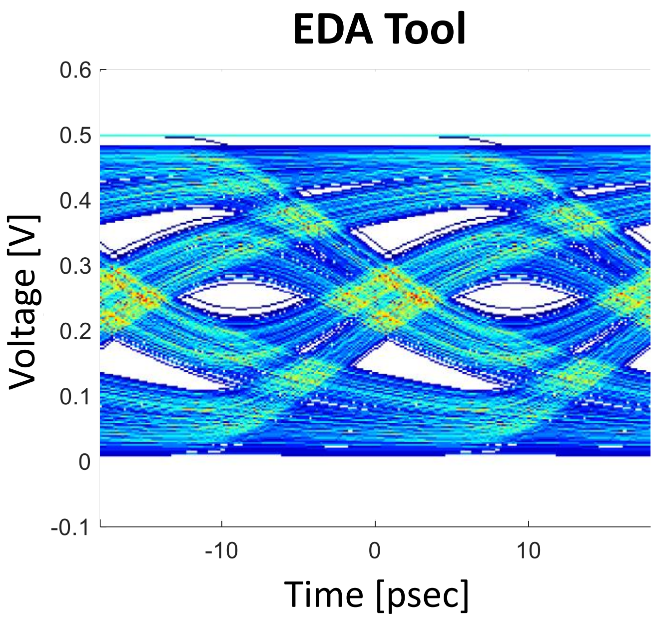


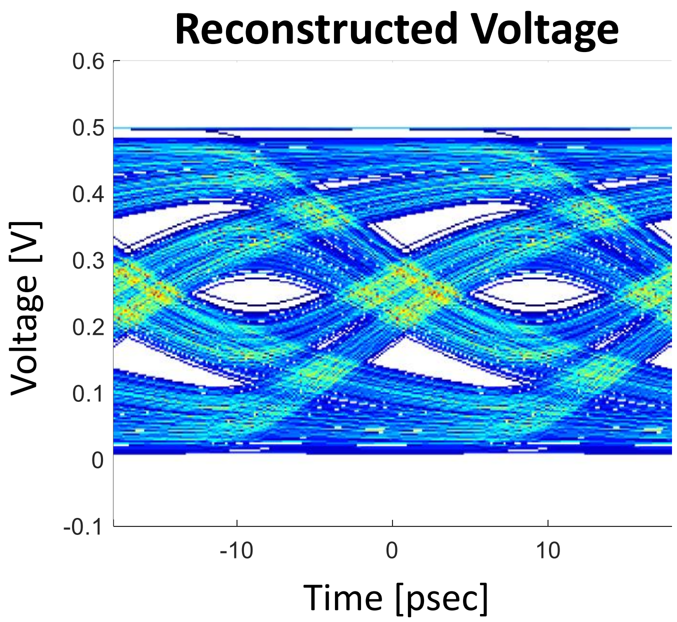
<IR extraction based on deconvolution>

- The IR is extracted by deconvolving the simulated input and output voltages and compared with the reference IR obtained by applying the IFFT to the channel S-parameters.
- The close agreement between the two results validates the proposed deconvolution-based IR extraction method.

Validation Results – Reconstructed Output Voltage



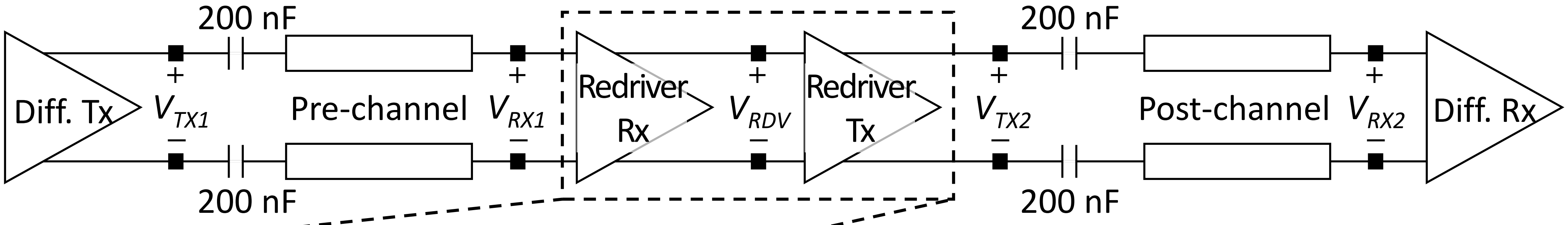


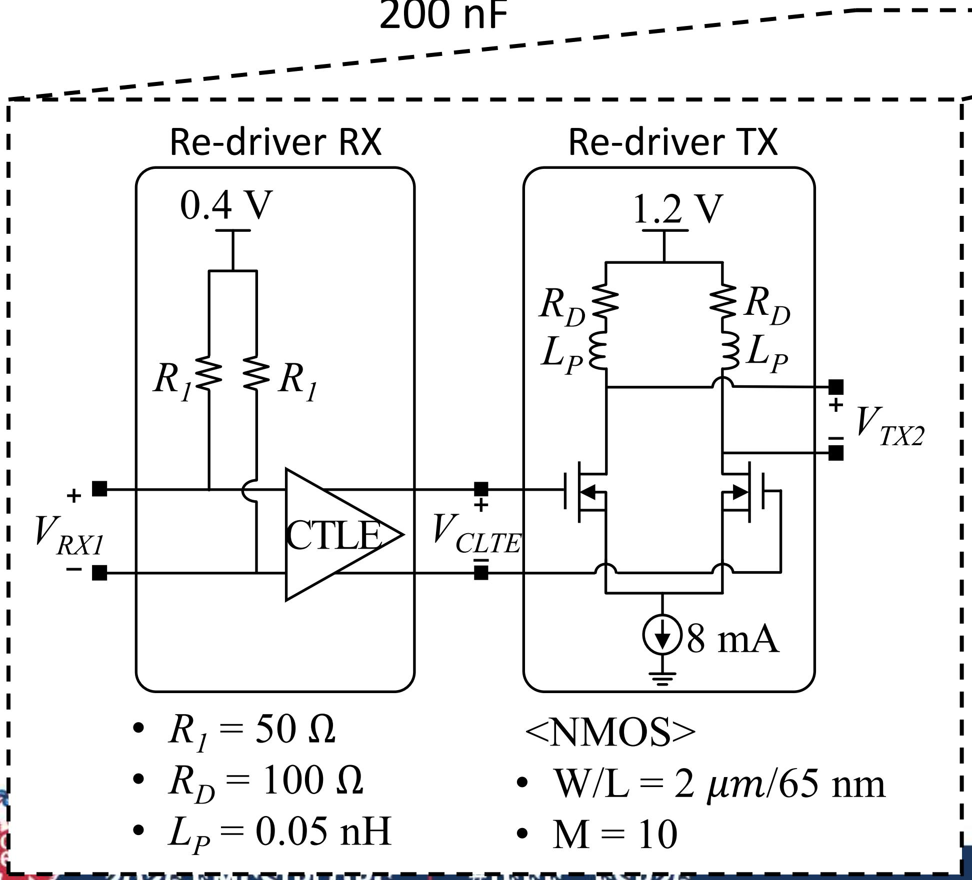


- The reconstructed output voltage, obtained by convolving the input voltage with the extracted IR, closely agrees with the EDA tool result in both the time-domain waveform and eye diagram.

Contents

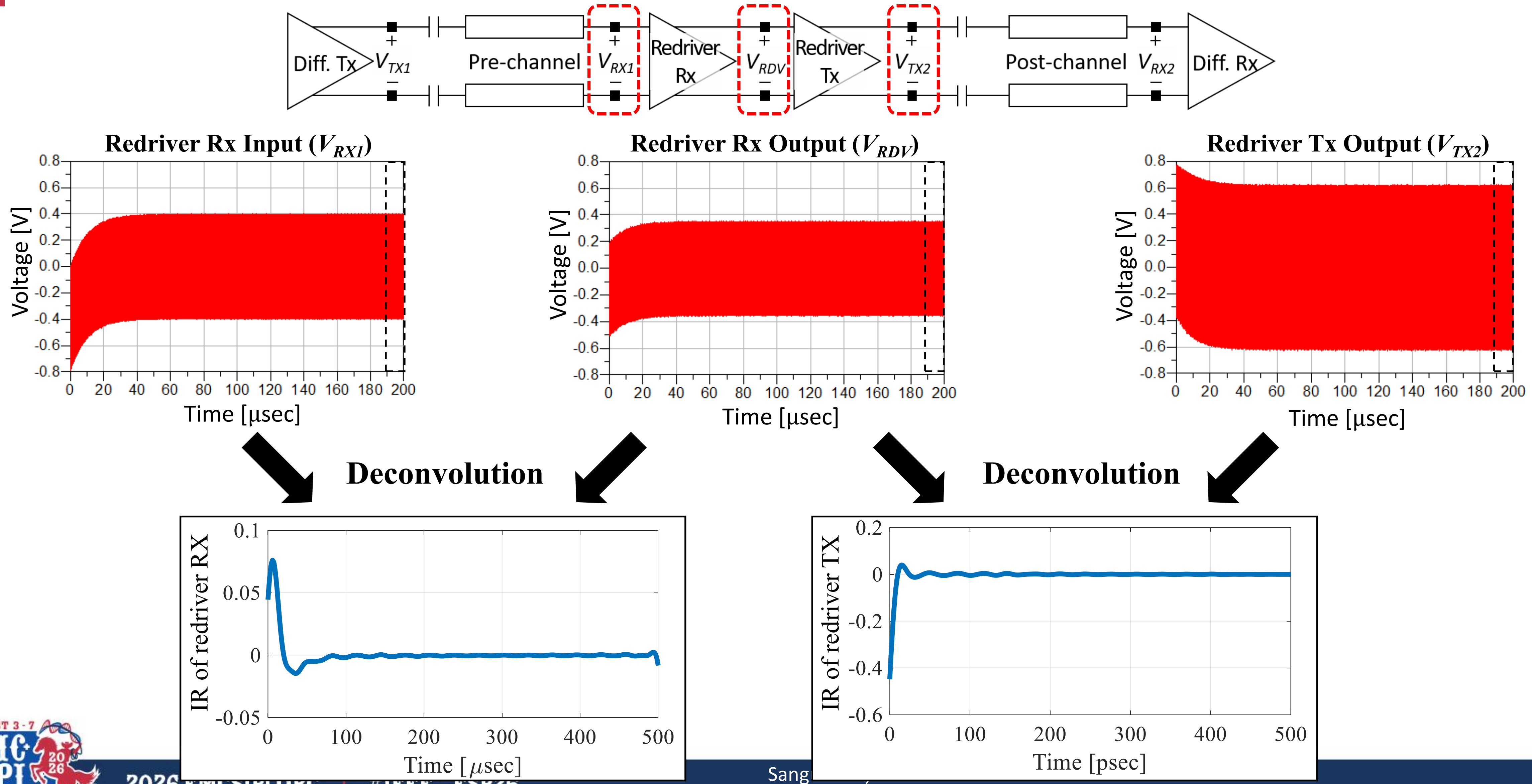
Mock-up Circuit Configuration for Verification





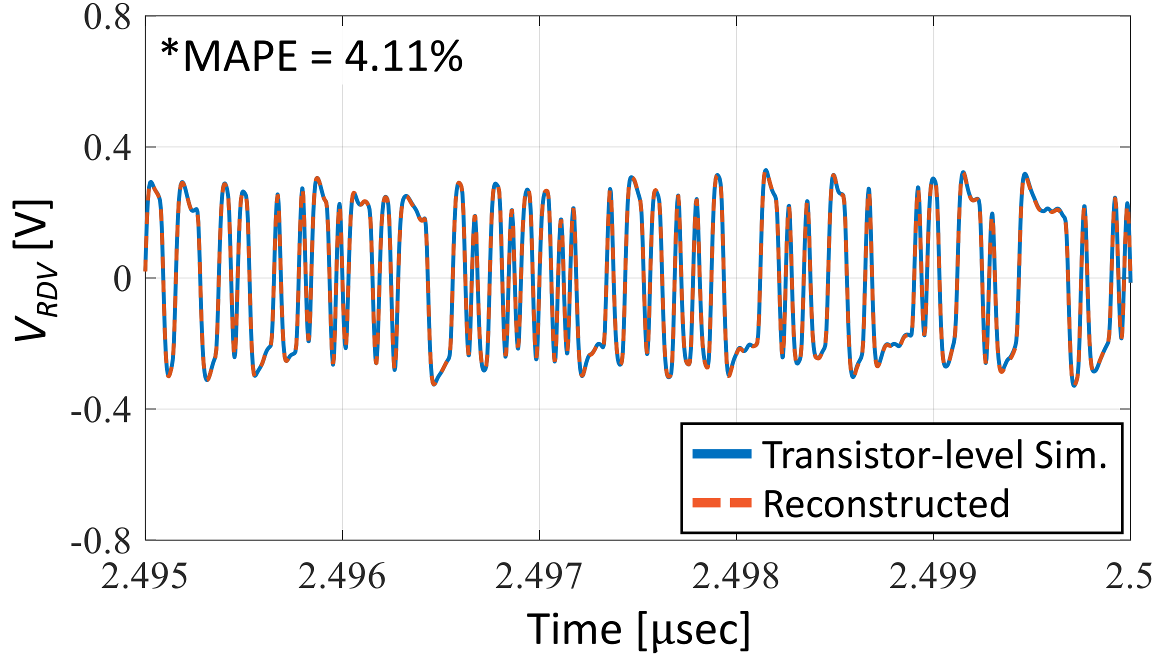
- The mock-up circuit is constructed, comprising a differential TX, pre-channel, redriver circuit, post-channel, and differential RX.
- The pre- and post-channels are configured with insertion losses of -8.4 dB and -8.2 dB at the Nyquist frequency of 16 GHz, respectively.
- Differential Tx
  - 800 mV, PRBS-8 pattern
  - Datarate: 32 Gbps (Rise/fall time = 10% of 1UI)

Transistor-level Simulation Result and IR Extraction

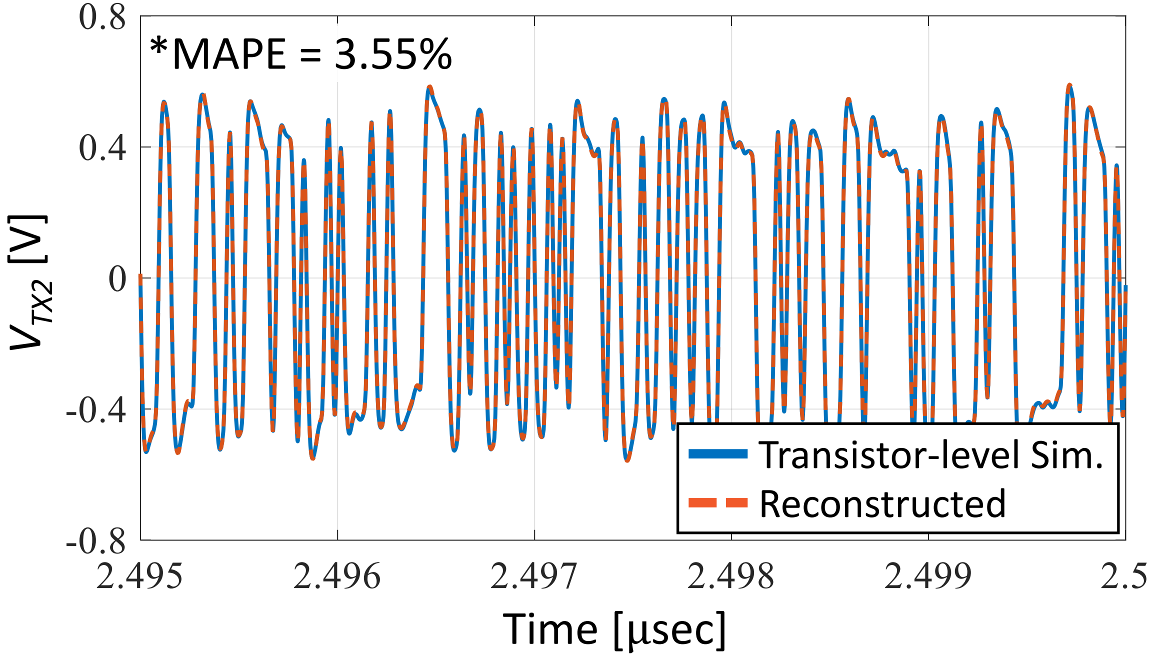


Reconstructed Output Voltage Using the Extracted IR

Redriver Rx Output (V_{RDV})



Redriver Tx Output (V_{TX2})

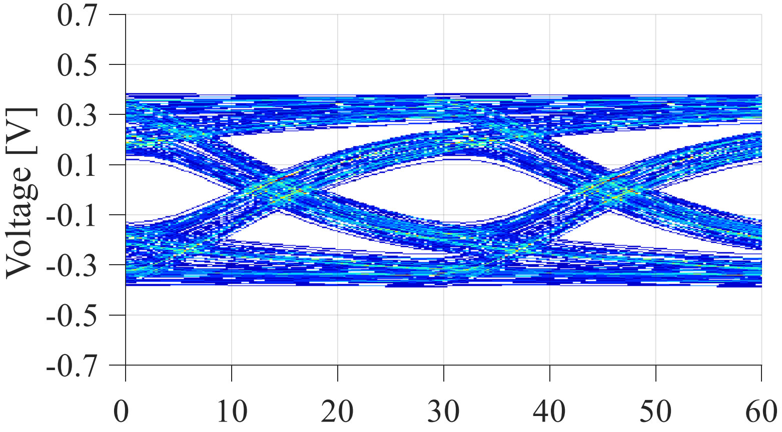
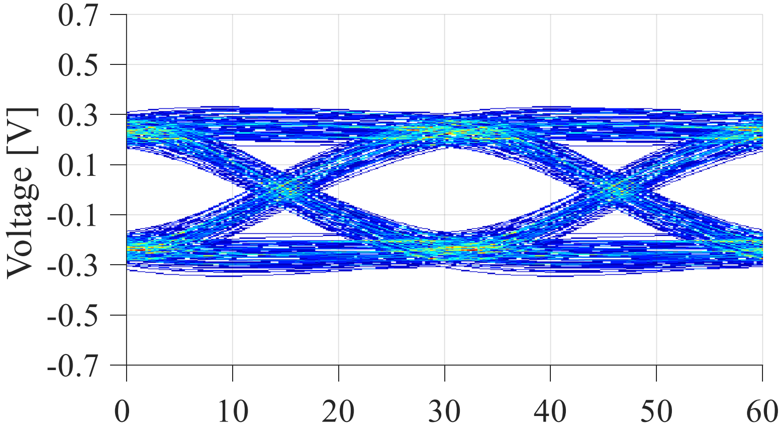
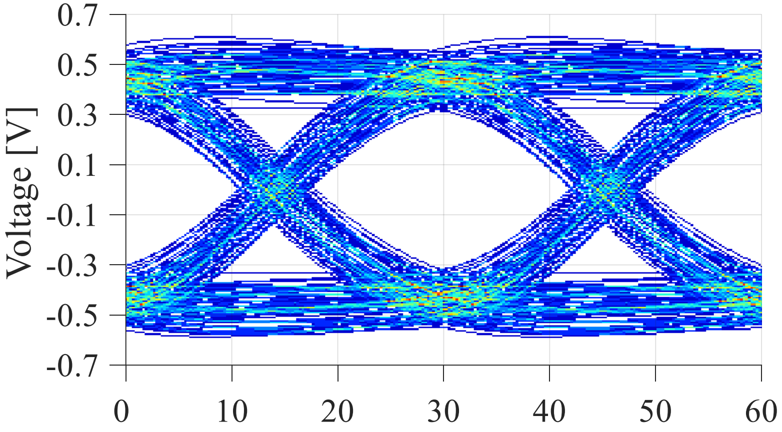
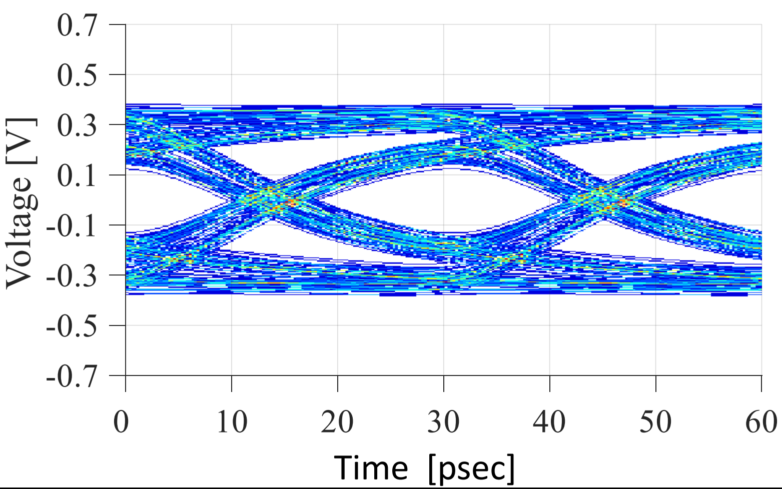
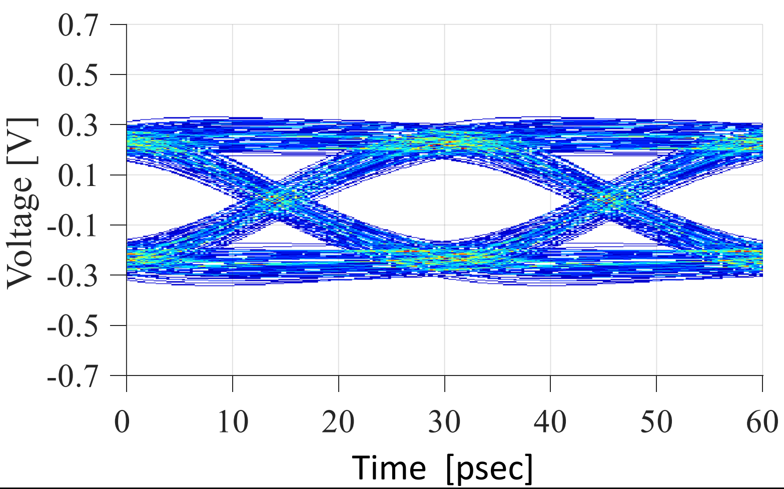
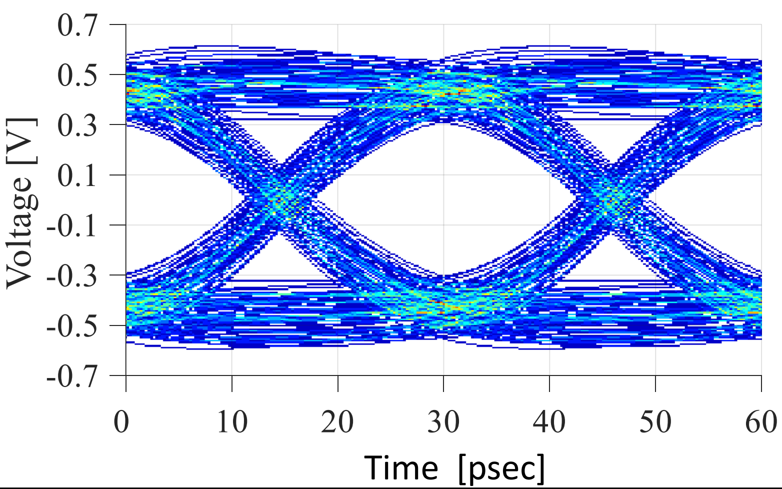


<Reconstructed output voltages obtained by convolving the extracted IR with PRBS-8 and PRBS-16 input waveforms>

- The reconstructed output voltages, obtained by convolving the extracted IR with PRBS-8 input waveforms, closely agree with the transistor-level simulation results, with MAPEs of 4.11% and 3.55%, respectively.

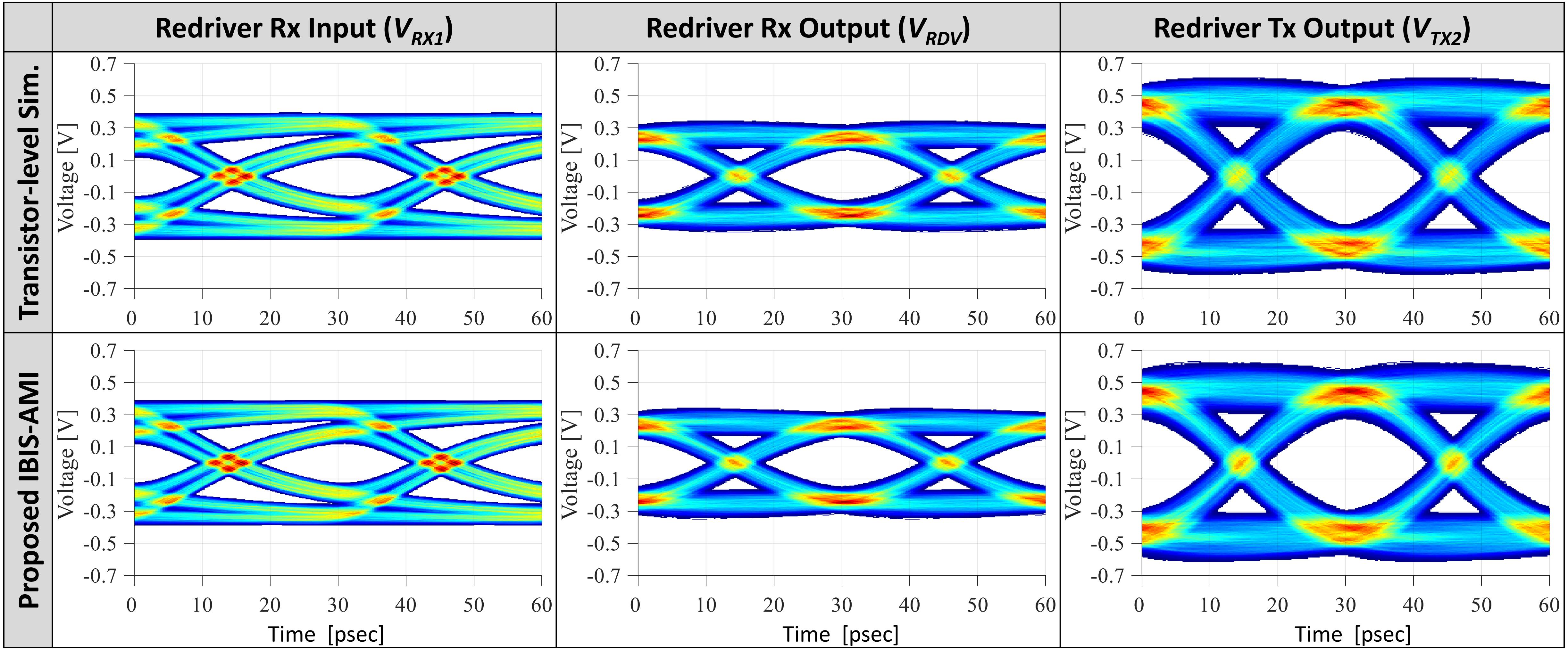
*MAPE: Mean absolute percentage error

IBIS-AMI Simulation Results – Case 1: PRBS8

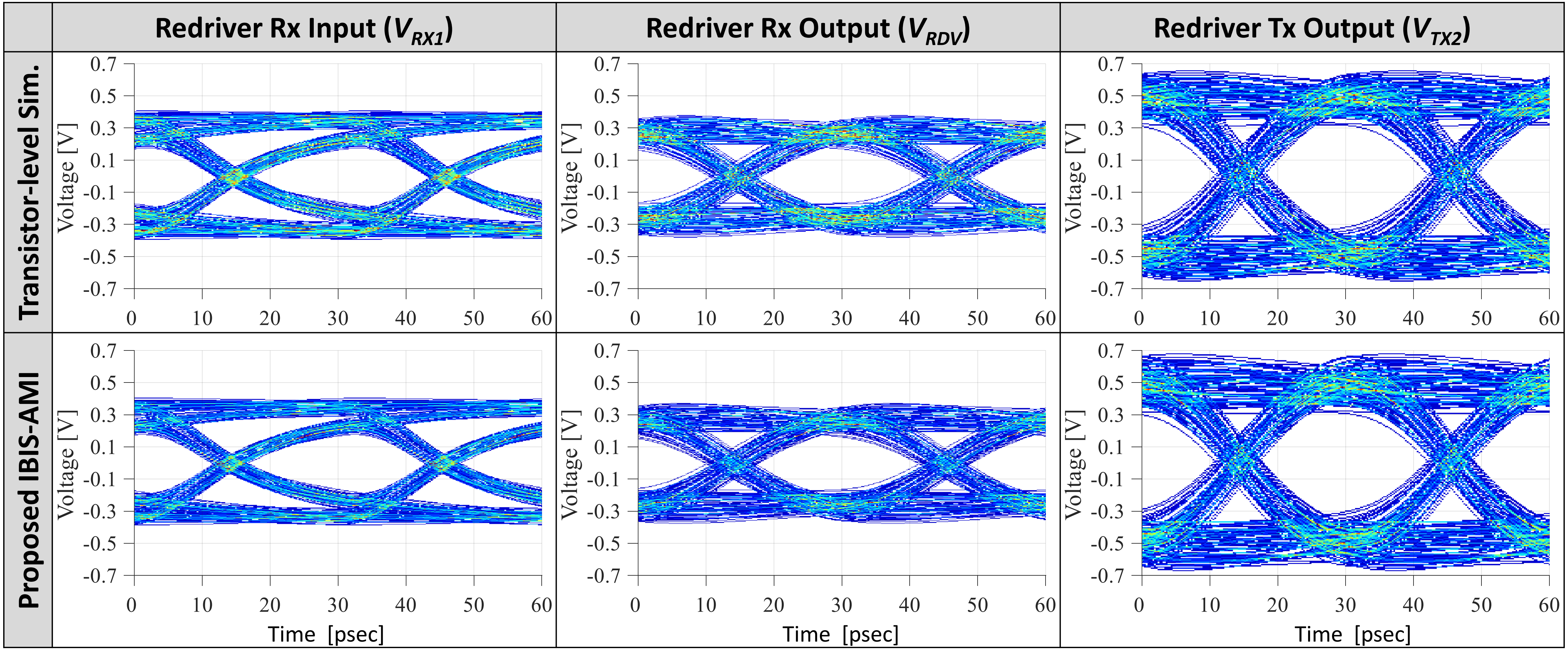
	Redriver Rx Input (V_{RX1})	Redriver Rx Output (V_{RDV})	Redriver Tx Output (V_{TX2})
Transistor-level Sim.			
Proposed IBIS-AMI			

- The proposed IBIS-AMI model closely matches the transistor-level eye diagrams at V_{RX1}, V_{RDV} and V_{TX2}.

IBIS-AMI Simulation Results – Case 2: PRBS16



IBIS-AMI Simulation Results – Case 3: PRBS8 + Different Channel



Comparison between Transistor-level and IBIS-AMI Simulation Results

(*): Relative error

Case	Voltage	Eye-height [mV]		Eye-width [psec]		Simulation time	
		Transistor-level	Proposed.	Transistor-level	Proposed.	Transistor-level	Proposed.
1 (PRBS8)	V_{RX1}	245.40	246.79 (0.6%)	21.90	22.39 (2.2%)	5 h 28 m 59 s	1 m 34 s (210.0x faster)
	V_{RDV}	333.80	324.28 (**2.9%**)	23.62	23.65 (0.1%)		
	V_{TX2}	617.99	602.96 (2.4%)	23.62	24.11 (2.1%)		
2 (PRBS16)	V_{RX1}	224.90	228.85 (1.8%)	20.91	21.16 (1.2%)	5 h 37 m 43 s	1 m 43 s (196.7x faster)
	V_{RDV}	289.23	282.07 (2.5%)	21.41	21.65 (1.1%)		
	V_{TX2}	541.77	536.70 (0.9%)	21.41	22.15 (**3.5%**)		
3 (PRBS8+ Diff. Ch)	V_{RX1}	355.51	354.83 (0.2%)	25.34	25.59 (1.0%)	5 h 38 m 21 s	1 m 14 s (274.3x faster)
	V_{RDV}	341.21	337.83 (1.0%)	23.38	23.13 (1.1%)		
	V_{TX2}	639.18	621.48 (2.8%)	23.13	23.87 (3.2%)		

- The proposed IBIS-AMI model achieves good agreement with the transistor-level results while reducing the simulation time by more than 196×, demonstrating high accuracy and computational efficiency.

Contents

Conclusion

- **Propose**d an IBIS-AMI model for the re-driver circuit using deconvolution-based IR extraction.

- **Verified** the extracted impulse responses by reconstructing the re-driver Rx and Tx output voltages, achieving MAPEs of 4.1% and 3.6%, respectively.

- **Validated** the proposed IBIS-AMI model through eye-diagram comparisons, with eye-height and eye-width errors below 2.9% and 3.5%, respectively, while achieving a simulation speedup of more than 197× over transistor-level simulation.

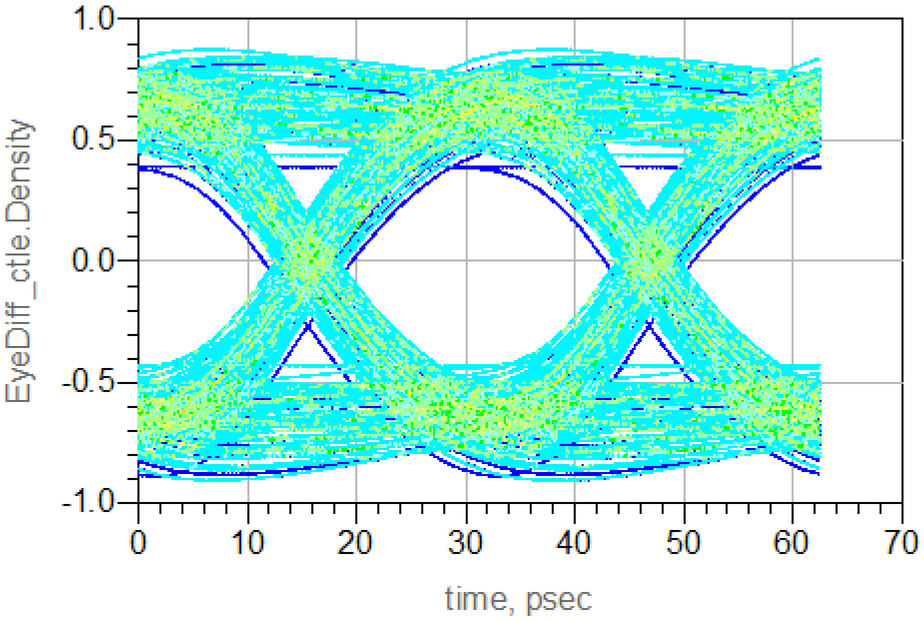
Thank you

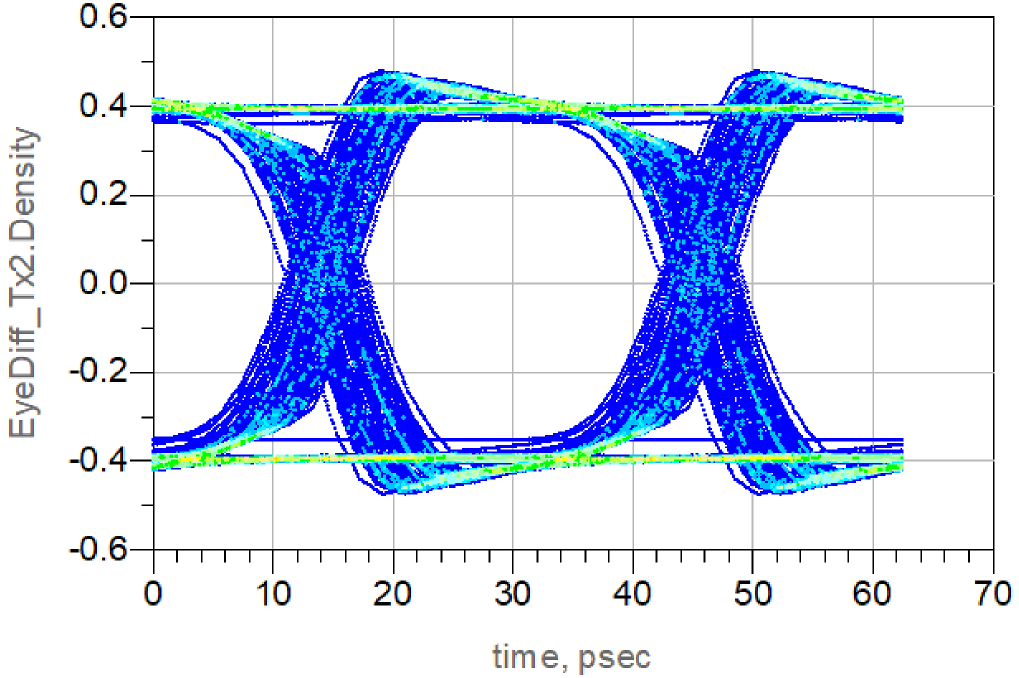
Sanguk Lee

Korea Advanced Institute of Science and Technology

sang960326@kaist.ac.kr

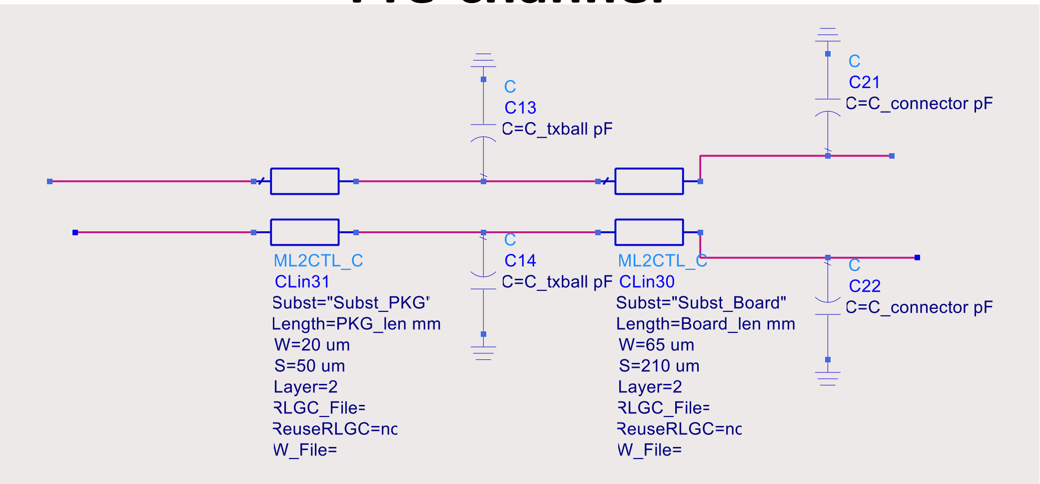
Transistor level simulation – w/o AC coupling capacitor

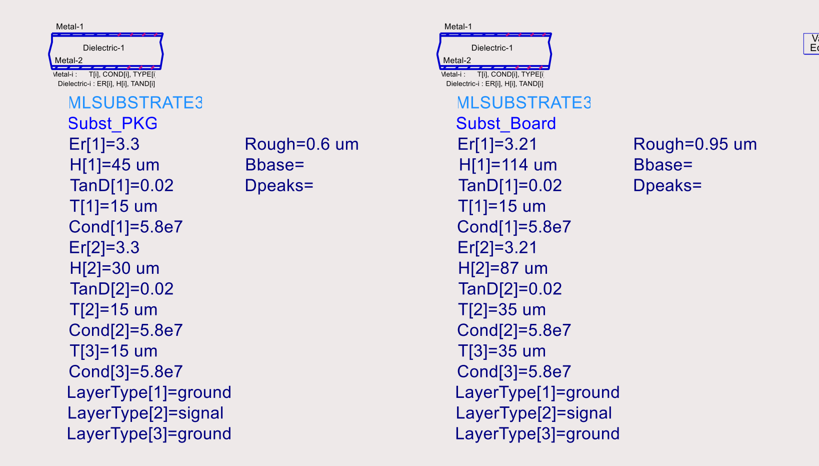




Pre- and Post-channel configuration

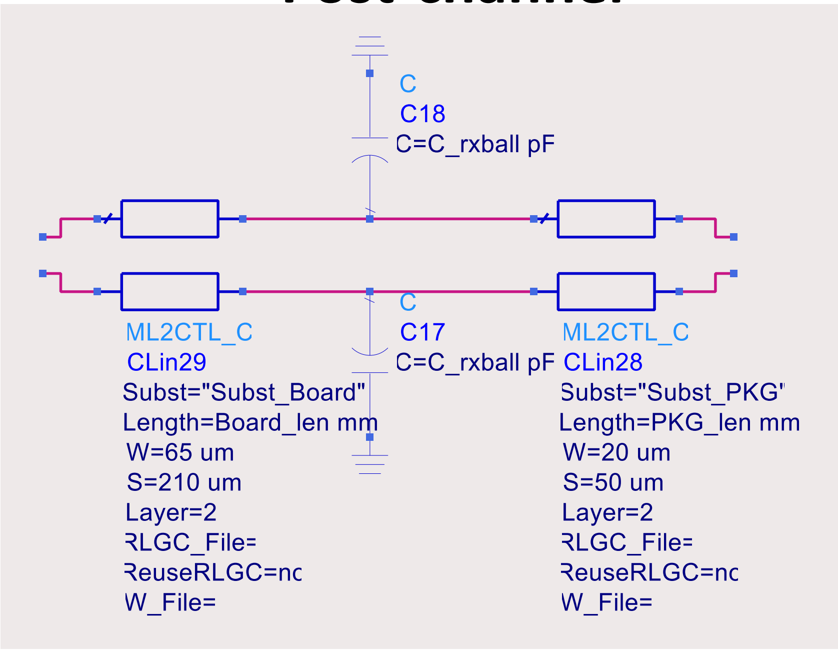
Pre-channel





3layer
(G-S-G)

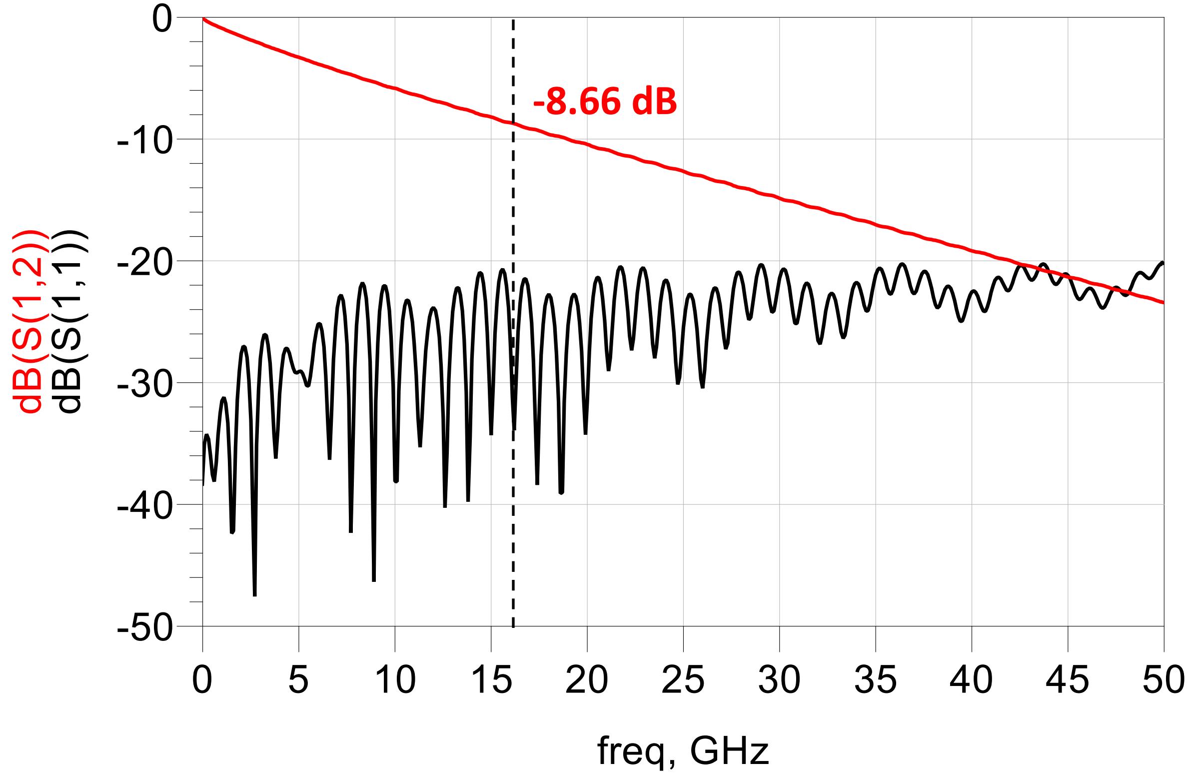
Post-channel



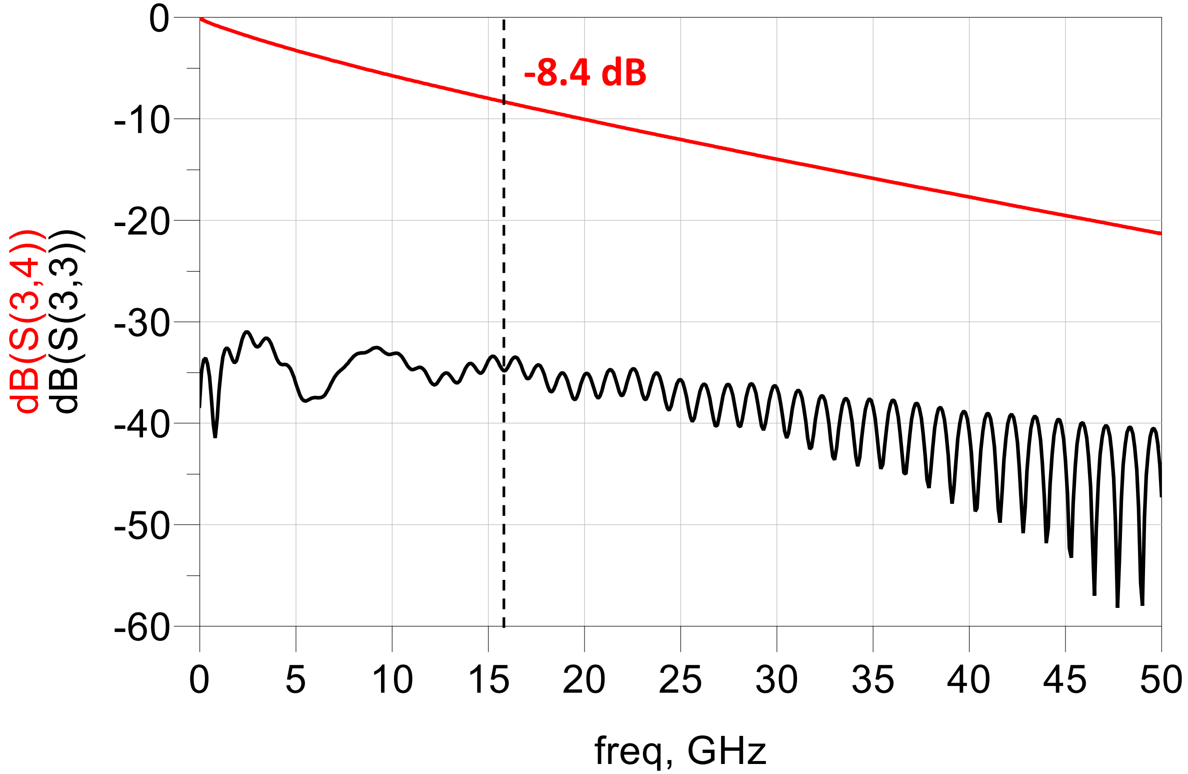
(default length)
brd = 70 mm
pkg = 12 mm

Sparameter of Pre- and Post-Channel

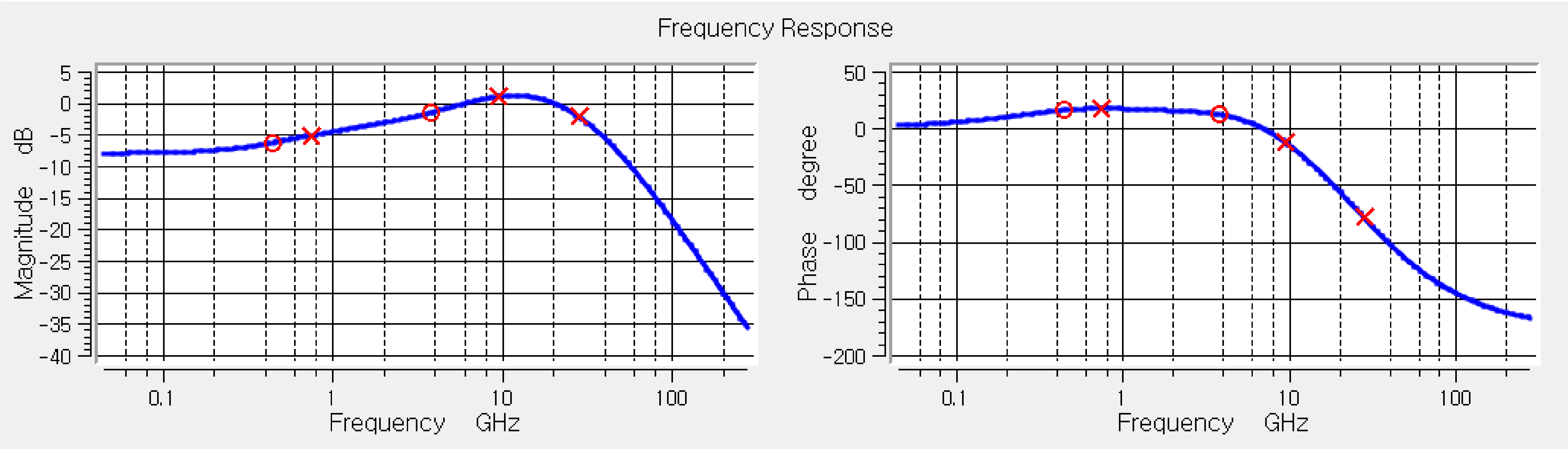
Pre-channel



Post-channel



Frequency Response of CTLE



$$H(s) = \frac{\omega_{p1}\omega_{p3}\omega_{p4}}{\omega_z} \cdot \frac{(s+\omega_z)(s+A_{dc}\omega_{p2})}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})(s+\omega_{p4})}$$

Transfer Function Type	4 Pole, 1 Zero							
DC Gain	0.39811		DC Gain 2					
Zero 1 Frequency	0.45	GHz	Zero 2 Frequency		GHz			
Pole 1 Frequency	0.7425	GHz	Pole 2 Frequency	9.5	GHz	Pole 3 Frequency	28	GHz
Pole 4 Frequency	28	GHz	Pole 5 Frequency		GHz	Pole 6 Frequency		GHz