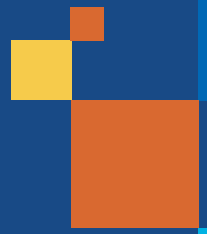
IBIS Interconnect Task Group Update

Touchstone 3.0 Features & Progress

Michael Mirmak (michael.mirmak@intel.com)

Presented at the Hybrid IEEE EMC+SIPI 2026 IBIS Summit
Dallas, Texas
August 6, 2026

Some material originally presented at the Hybrid Asian IBIS Summit 2025, Tokyo and the Asian IBIS Summit 2024, Shanghai



intel®

Legal Disclaimer

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at Intel.com, or from the OEM or retailer.

No computer system can be absolutely secure. Intel does not assume any liability for lost or stolen data or systems or any damages resulting from such losses.

You may not use or facilitate the use of this document in connection with any infringement or other legal analysis concerning Intel products described herein. You agree to grant Intel a non-exclusive, royalty-free license to any patent claim thereafter drafted which includes subject matter disclosed herein.

No license (express or implied, by estoppel or otherwise) to any intellectual property rights is granted by this document.

The products described may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest Intel product specifications and roadmaps.

Intel disclaims all express and implied warranties, including without limitation, the implied warranties of merchantability, fitness for a particular purpose, and non-infringement, as well as any warranty arising from course of performance, course of dealing, or usage in trade.

Warning: Altering PC clock or memory frequency and/or voltage may (i) reduce system stability and use life of the system, memory and processor; (ii) cause the processor and other system components to fail; (iii) cause reductions in system performance; (iv) cause additional heat or other damage; and (v) affect system data integrity. Intel assumes no responsibility that the memory, included if used with altered clock frequencies and/or voltages, will be fit for any particular purpose. Check with memory manufacturer for warranty and additional details.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit http://www.intel.com/performance.

Cost reduction scenarios described are intended as examples of how a given Intel- based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction.

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether referenced data are accurate.

Copies of documents which have an order number and are referenced in this document may be obtained by calling 1-800-548-4725 or by visiting www.intel.com/design/literature.htm

Intel, the Intel logo, and Xeon are trademarks of Intel Corporation or its subsidiaries.

*Other names and brands may be claimed as the property of others.

Touchstone History… and Gaps

*More detailed history in "**Touchstone Immediate and Long-Term Future**" from 2023*

- Touchstone format maintained by the IBIS Open Forum since 2007
  - Touchstone 1.1 (2002) – documented format from mid-1980s RF software
  - Touchstone 2.0 (2009) – added optional IBIS-like keywords for cross-checking
  - Touchstone 2.1 (2024) –corrections plus clarifications on per-port referencing

- Touchstone gaps identified by industry in the interconnect context
  - File compression not supported: large, fast networks cause unwieldy files
  - Connecting ports requires documentation: automation not supported

Touchstone 3.0 is being prepared to address these issues

Proposed Changes for Touchstone 3.0

- Touchstone Issue Resolution Documents
  - 7.2 Standardized Pole-Residue Representation
  - 8 Option line changes
  - (9) Standardized Port Mapping (WIP): Draft 29

The goal: balance usability by the wider industry (e.g., for RF and circuit purposes) with IBIS-specific features to help with package and system interconnect modeling

Pole-Residue for File Compression

Not shown…
[Begin Pole-Residue Data Source] /
[End Pole-Residue Data Source]

- A coefficients example, where data corresponds to [α_m ω_m A_m B_m] complex pole and normalized residue pairs, respectively

```
[Number of Pole-Residue Indices] 10

[Begin Pole-Residue Data] (1,1) (2,2) (3,3) (4,4)
Delay = 1.26351e-09
Constant_at_infinity = 0.321123423421
Number_of_data_lines = 35
1.60981891e+08 6.038300e+09 -2.15363238e-06 1.96534688e-05
2.93321810e+09 1.917708e+09 -1.05426912e+01 -8.82630433e+00
1.23990373e+08 4.399943e+09 1.257286128e-05 2.13669372e-05
...
5.23409852e+06 1.345345e+07 3.073147044e-06 5.16091015e-06
[End Pole-Residue Data]

| Additional data pairs follow…
```

Alternately, a pair of keywords may be used:

Common Poles Data
- All matrix elements share the same poles
- Just one per set model file

Residues Data
- Defines data for individual pairs
- Also includes the same subparameters

The data is meant for use in a single equation shown here for one (row, column) element…

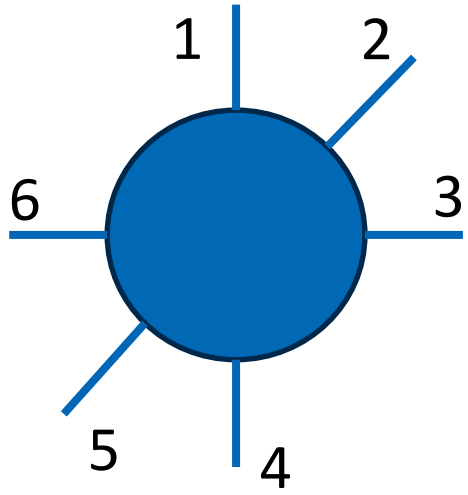
$$H(if) = \mathrm{e}^{-i2\pi fD}\left\{H_0 + \frac{1}{2}\sum_{m=1}^{M}\left[\frac{A_m - iB_m}{1+if/(\alpha_m + i\omega_m)} + \frac{A_m + iB_m}{1+if/(\alpha_m - i\omega_m)}\right]\right\} + ifG$$

This format is understood and used, with variations, by several existing industry tools.

This change to Touchstone has already been approved – 10-100x compression!

The Port-Mapping Problem

- In current Touchstone, what can we say about this component?
  - Interconnect or device?
  - If interconnect, what is the relationship between terminals?
  - Can I make inferences from the data?
  - What is the referencing scheme (how do terminals become ports?
- For interconnects, we need to know the terminal arrangement to focus properly on losses, crosstalk and the like
  - Is S21 insertion loss? Or is S21 crosstalk?



 # MHz Y RI R 50

5.00 8.0 9.0 2.0 -1.0 3.0 -2.0 1.0 3.0 1.0 0.1 0.2 -0.2

2.0 -1.0 7.0 7.0 1.8 -2.0 -1.0 -1.0 -0.5 0.5 0.2 -0.1

3.0 -2.0 1.8 -2.0 5.8 6.0 1.2 0.8 0.9 0.7 0.3 -0.5

1.0 3.0 -1.0 -1.0 1.2 0.8 6.3 8.0 2.0 -0.5 1.5 0.6

1.0 0.1 -0.5 0.5 0.9 0.7 2.0 -0.5 4.7 -6.0 -1.0 2.0

0.2 -0.2 0.2 -0.1 0.3 -0.5 1.5 0.6 -1.0 2.0 5.5 -7.0

For interconnects, need a structure that establishes expectations for terminal behavior automatically and in advance of detailed data analysis

Port-Mapping WIP Syntax for Touchstone 3.0

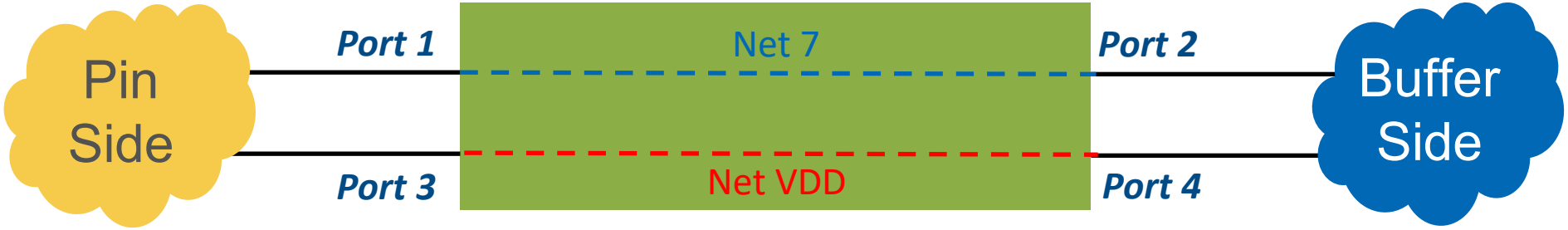
```
[Begin Port Map]
|
Data_usage "IBIS_Interconnect"
Port 1 (Physical pin.7)              (Type S)(Side Pin)     (Net 7)   (Logical DQ3pin)
Port 2 (Physical buf.7)              (Type S)(Side Buffer)  (Net 7)   (Logical DQ3buffer)
Port 3 (Physical Pin.Bus_label:VDD)  (Type P)(Side Pin)     (Net VDD)(Logical VDDpin)
Port 4 (Physical Pullup_ref.7)       (Type P)(Side Buffer)  (Net VDD)(Logical VDDbuffer)
Symbol_leftside 1 3
Symbol_rightside 2 4
|
[End Port Map]
```

Data_usage is optional, and supports IBIS structures EMD, C_comp_model and Ts4file as well

Reference and Diff_Port identifiers are also available

A port is a pair of terminals. The reference terminal is A_gnd for all ports in this example.

DQ3 and VDD from pin to buffer



Physical and Net provide connectivity guidance;
all other identifiers are informative (e.g., for schematic symbols)

NEW: Limitations of IBIS Interconnect and EMD

- A challenge of linking IBIS structures to Touchstone…

For File_TS, the Terminal_number entry shall match the Touchstone file port number or reference terminal line, as shown below. The Terminal_number entries may be listed in any order as long as there are no duplicate entries. The terminal line for Terminal_number N+1 is required as a reference terminal for each port and shall be connected to a rail terminal or A_gnd in the EMD Model. At least one other terminal line entry is required.

Terminal_number	Port
1	1
2	2
…	
N	N
N+1	Reference terminal for the Touchstone file

EMD only supports Touchstone structures with a single reference terminal

All other "ports" are terminals using this reference

- The initial release of Touchstone 3.0 Port Mapping will support multiple references in ways that IBIS Interconnect and EMD cannot
  - Updates to IBIS will be needed (BIRDs); Touchstone 3.x updates to follow

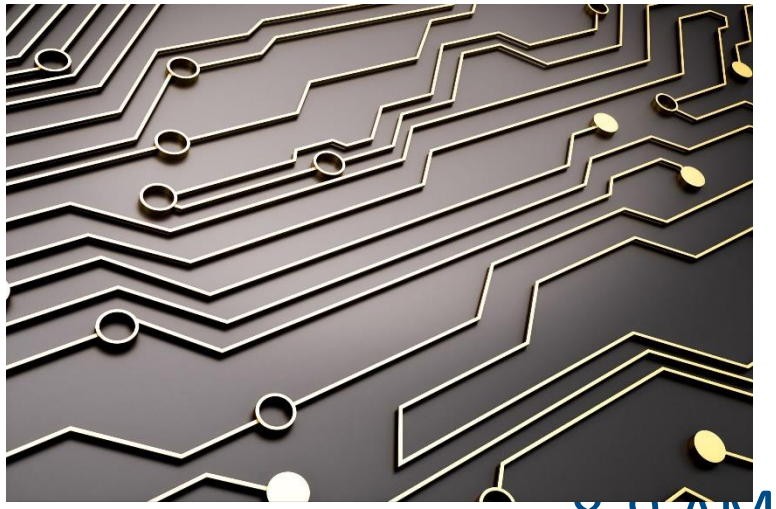
Our Request to the Community

- Touchstone 3.0 is targeting the two major
  - Reduce file sizes
  - Support port-mapping for automated connections
- Do these changes address your needs?
  - If not, what features are missing?
- What test cases would you need to evaluate Touchstone 3.0?
  - What examples should be part of the standard?

Please review the documents and provide comments!

Backup

Who Is The IBIS Interconnect Task Group?



- Designs and writes technical changes support passive interconnect formats
  - Supports IBIS, Touchstone and IBIS-ISS
  - Live teleconferences are held Wednesdays 8-9 AM US Pacific Time
  - Web site: https://ibis.org/interconnect_wip/
  - Freelists is the most up-to-date source for documents and discussion:
  - https://freelists.org/archive/ibis-interconn/


intel