IBIS and Behavioral Modeling

Michael Mirmak
Intel Corporation
Chair, EIA IBIS Open Forum

IBIS Summit
Shenzhen, China
December 6, 2005
Legal Disclaimers

- THIS DOCUMENT AND RELATED MATERIALS AND INFORMATION ARE PROVIDED "AS IS" WITH NO WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE. INTEL ASSUMES NO RESPONSIBILITY FOR ANY ERRORS CONTAINED IN THIS DOCUMENT AND HAS NO LIABILITIES OR OBLIGATIONS FOR ANY DAMAGES ARISING FROM OR IN CONNECTION WITH THE USE OF THIS DOCUMENT.

- Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

- Intel may make changes to specifications, product descriptions, dates and plans at any time, without notice.

- Copyright © 2005, Intel Corporation. All rights reserved.
What is IBIS?

- **IBIS** (I/O Buffer Information Specification)
  - A standard format for expressing I/O buffer electrical behavior plus component pin and package information
  - ANSI/EIA* 656-A, IEC* 62014

Most buffers expressed through
- Current vs. Voltage (I-V tables)
- Voltage vs. Time (V-T tables)
- Buffer capacitance (C_comp)

Components include
- Pin assignments and names
- Package information
Behavioral Modeling

- IBIS is only one type of behavioral model
  - Others include:
    - ICM* (IBIS Interconnect Modeling Specification)
    - IMIC* (I/O Model for Integrated Circuits, JEITA* ED-5302)
    - ICEM* (Integrated Circuit Electrical Model, IEC 62014-3)
    - VHDL-AMS* (IEEE* 1076.1)
    - Verilog-AMS* (Accelera*)
  - Behavioral models replace internal design information with **observations of electrical ports or terminals**
An Example

- IBIS, as a behavioral modeling standard, offers
  - Protection of internal design information
  - Availability under multiple software tools
  - Increases in simulation speed over transistor-based models
- **IBIS behavioral vs. transistor-based models**
  - For a serial-differential design, IBIS can be 100 times faster!
  - Careful model creation preserves accuracy

**IBIS vs. SPICE**
(time-shifted to show correlation)

Image from SiSoft*:
IBIS Models at 2.5 GHz and Beyond; used with permission

Speed quotation from
Multi-Gigabit SerDes System Level Analysis...
by Huq/Dodd; used with permission
The Future of Modeling

Why behavioral instead of transistor-based models?

Processor MIPS per Year: 1982-2004
(smoothed plot; source: Intel Corp.)

Processor MIPS

Year


12/06/05
*Other brands and names are the property of their respective owners
The Future of Modeling

- Buffer complexity is keeping pace with processor power!

I/O Buffer Size and Processor MIPS per Year: 1995-2004
(sourced: Intel Corp.)

- Serial ATA 1.5 & 3.0 Gb/s (TX only)
- PCI Express® (one lane)
- PCI 33 (one data line)
Supporting Future Designs

- Buffers becoming more complex
  - Size is *tracking processing power*
- New designs need more analysis
  - Power delivery and switching noise
  - Pre-emphasis, active feedback and compensation
- IBIS expanding to address needs
  - New links to VHDL-AMS, Verilog-AMS, Berkeley SPICE*
  - Enable equations within IBIS
  - Links to ICM are in development

The industry needs behavioral modeling for today and tomorrow

IBIS provides a standard, unified solution for behavioral buffer modeling
You Are Invited!

- IBIS Welcomes Worldwide Participation!

**Specifications**
- ICM: [http://www.eda.org/ibis/icm_ver1.1/](http://www.eda.org/ibis/icm_ver1.1/)

**Training**
- Including IBIS history and tutorials
  - [http://www.eda.org/ibis/training/](http://www.eda.org/ibis/training/)

**IBIS Cookbook**
- Features explained plainly
  - [http://www.eda.org/ibis/cookbook/](http://www.eda.org/ibis/cookbook/)

**Task Groups**
- Futures, Macromodel Library, Quality
- Free Model Review service!

IBIS appreciates your input and support!
BACKUP
A Related Specification: ICM

ICM = IBIS Interconnect Modeling Specification
- Standard text format for interconnect modeling data
- “Interconnect” can be connector, cable, PCB traces or even an IC package
  - Defines structure as path between “sections”
  - Defines the electrical data for each section

Described by
[Begin ICM Model]
... (path description)
... [End ICM Model]

Described by
[Begin ICM Section]
... (RLGC or S-params)
... [End ICM Section]