IBIS在信号完整性分析中的应用
Using IBIS for SI Analysis

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Outline

• What happened on IBIS （IBIS历史）
• Why IBIS （IBIS的好处）
  – Speed and Accuracy （速度和精度）
  – Industrial Examples （工业化例子）
• Advanced IBIS Technologies （加强型IBIS技术）
  – Complex-IO Devices （复杂I/O器件）
  – Macromodeling is a solution （宏模型解决方案）
  – Experiences and Industrial Examples （经验和工业化例子）
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What happened on IBIS
- Spice Transistor Level Models

- Very Complicated
- A lots of unusable stuff
- Too slow in the simulations
What happened on IBIS

- Behavioral Models

Behavioral Extractions
What happened on IBIS
- IBIS is behavioral Model

IBIS model

Block diagram of CMOS buffer

A basic IBIS model consists of:
- four I-V curves: pullup & POWER clamp, pulldown & GND clamp
- two ramps: dV/dt_rise, dV/dt_fall
- die capacitance: C_comp
- packaging: RLC values

for each buffer on a chip
What happened on IBIS
- The Original “Box”

- 1st PCI Chipset (33 MHz)
- 1st Pentium uP (66 MHz)
...and the “Box” did grow

- 1st PCI Chipset (33 MHz)
- 1st Pentium uP (66 MHz)

An increasing amount of Complex IO models are missing the box
What happened on IBIS
- IBIS Model Vendors

![Graph showing Top10 IBIS Model Vendors on Web](image)
What happened on IBIS
- IBIS in EDA Tools（IBIS在EDA工具中的应用）

• Major EDA Simulators are supporting IBIS now
  – Cadence
  – Mentor

**SPICE Simulators are taking IBIS now !!!**
  – Agilent

And many, many more ……
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Why IBIS（IBIS的好处）

-Speed and Accuracy（速度和精度）

- Behavioral data in Spice simulators

\[ I_{\text{pad}} = I_{pd}(V_{\text{pad}} - V_{\text{gnd}}) \cdot W_d(t) + I_{cd}(V_{\text{pad}} - V_{\text{gnd}_c}) \]
\[ + I_{pu}(V_{\text{pad}} - V_{\text{pwr}}) \cdot W_u(t) + I_{cu}(V_{\text{pad}} - V_{\text{pwr}_c}) \]

- Results are accurate
- Much, much faster simulation time
- 20-1000 times faster
- IP Protected
Why IBIS（IBIS的好处）
- Industrial Examples（工业化例子） (133MHz)

Driver: IDT 79RC32438
Receiver: Micron MT46V16M8TG
Why IBIS （IBIS的好处）
- Industrial Examples（工业化例子）(622Mbps)
Why IBIS (IBIS的好处) - Industrial Examples (工业化例子) (622Mbps)

Eye Height: 210mv
Eye Width: 1.1ns

Eye Height: about 240mv
Eye Width: about 1.15ns
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  – Speed and Accuracy
  – Industrial Examples

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  – Complex-IO Devices  （复杂I/O器件）
  – Macromodeling is a solution  （宏模型解决方案）
  – Experiences and Industrial Examples  （经验和工业化例子）
Pre-emphasis \( \text{预加重} / \text{De-emphasis} \text{去加} \)

**Emphasis (t) = Input (t-1)**

- **Input stimulus pattern**
  - \( \text{X011 1011} \)
  - \( \text{in concert} \)
  - \( \text{0111 0111} \)
  - \( \text{X100 0100} \)

- **Emphasis stimulus pattern**
  - \( \text{X011 1011} \)
  - \( \text{in opposition} \)

- **Main (+ & -)**
  - Non-Inverting
  - Inverting

- **Boost (+ & -)**
  - Non-Inverting
  - Inverting

- **TX+ Pad**
  - \( \text{1000 1000} \)

- **TX- Pad**
  - \( \text{0111 0111} \)

Picture from Michael Mirmak's presentation in DesignCon East IBIS Summit 2004
Complex-IO Devices

Self calibrating driver
(Charging Output Impedance only)
(For DDR2, when controller in a read cycle, the receiver is terminate)
(50 ohms. The resistor also requires to calibrate at run-time)

Driver with Slew Rate Control

Note:
1) PMOS side is not being shown here.
2) For simplicity, NMOS and PMOS are used interchangeable.
Independent slew control for Rise and Fall.
What is MacroModeling and Why?

Macromodeling is a Methodology

- Equation-based macromodeling of LVDS drivers
- Accurate and efficient macromodel (5-10x speed-up)
- Methodology only
- Flexible methodology
- No specific assumption on device internal structure (preserve IP)
- Handle drivers with enhanced features (e.g., control cKts)
- Multi-lingual extension

KEY
Conclusions
Macromodel from architecture templates

- Most modern devices are based on known DSP circuit architectures

Match template parameters to Layout model to get an accurate macromodel
“Altera successfully adapted the MacroModel templates to produce fast and accurate models of our multi-gigabit transceivers. Not only did the resulting model correlate well, it also simulates between 20 to 400 times faster than its transistor-level counterpart. And the model can be easily adjusted to match the behaviors of actual silicon measured in the lab.”

Correlation: MacroModel vs TransistorModel

“Overall, the templates were simple to work with and very valuable amidst the challenges of multi-gigahertz design.”
Correlation - Altera Stratix GX

- Transistor Level Model (HSpice)
- Spice Macromodel (Cadence DML)

Transmitter output at factor=5
Case Study: Agere Systems 4 Gbps SerDes

Given transistor simulation output and macromodel template, how many iterations and how much time required to make an accurate model?

Final Correlation
- 17th Iteration
- 54 minutes
- ~400x faster sim

Adjusted
1. rt
2. scale
3. cf1
4. padcap
5. dt
6. c_comp

Transistor 1st Try 9th Try (15 mins) 12th Try (30 mins)
Cadence IBIS 4.1 Kit

IBIS 4.1 Kit
- README

IBIS 4.1 MODELS
For Simulators
- SPICE
- HSpice
- Spectre

IBIS 4.1 SIMULATIONS
Templates
- SerDes
- Gate Modulation
- PCI Express IO
- Non-ideal Power
- Pass-thru Rx
- Self-calibrating Tx
- DFE

IBIS 4.1 TOOLS
- Ibis2signoise
- Ibischk4
- SPICE manual
Thank You