Splitting $C_{comp}$ for Power Integrity Simulations

Zhiping Yang, Ph.D.
Cisco Systems, Inc.
(Now with Apple Computer, Inc.)

Asian IBIS Summit in ShenZhen, China
12/6/2005
Acknowledgment

- The author would like to thank Cisco Systems, Inc. for the support and approval of this presentation material.
- The author would like to thank Apple Computer, Inc. for providing travel arrangements to make this presentation happen.
- The author would like to thank Randy Wolf from Micron for his support and help on HSPICE buffer model.
Why C_comp and its split ratio are important for power integrity simulations?

The procedures to extract the C_comp and C_decap values from HSPICE simulations

Simulation results for Micron U27_a_dq buffer
Why C_comp and its split ratio are important for power integrity simulations?

C_comp could impact the power integrity simulations in following ways:

- C_comp at non-switching I/O could act as effective local decoupling caps. The ratio has a big impact.
- C_comp split ratio heavily impacts the noise level coupled from power supply to quite I/O pins, especially at high frequency.
- C_comp split ratio will have direct impact on dynamic current distribution for switching I/O buffers.

Note: C_comp split ratio has no impact on SI simulations when voltage supply is ideal.
Simplified I/O model for IBIS specification
Zvddq_open

\[
Z_{vddq\_open} = Z_{\text{decap}} \parallel (Z_{\text{up}} + Z_{\text{down}}) \quad (1-1)
\]

\[
Y_{vddq\_open} = Y_{\text{decap}} + \frac{Y_{\text{up}} \times Y_{\text{down}}}{Y_{\text{up}} + Y_{\text{down}}} \quad (1-2)
\]
Z_{vddq\_short\_to\_gnd}

\[ Z_{vddq\_0} = Z_{decap} // Z_{up} \quad (2-1) \]

\[ Y_{vddq\_0} = Y_{decap} + Y_{up} \quad (2-2) \]
Z_vddq_short_to_pwr

Z_{vddq_1} = Z_{decap} // Z_{down} \quad (3-1)

Y_{vddq_1} = Y_{decap} + Y_{down} \quad (3-2)
\[ Z_{io} = Z_{down}/Z_{up} \quad (4-1) \]

\[ Y_{io} = Y_{down} + Y_{up} \quad (4-2) \]
Extraction of Yup, Ydown and Ydecap

- \( Y_{vddq_0} = Y_{decap} + Y_{up} \) (2-2)
- \( Y_{vddq_1} = Y_{decap} + Y_{down} \) (3-2)
- \( Y_{io} = Y_{up} + Y_{down} \) (4-2)

- \( Y_{up} = (Y_{vddq_0} + Y_{vddq_1} + Y_{io})/2 - Y_{vddq_1} \) (5-1)
- \( Y_{down} = (Y_{vddq_0} + Y_{vddq_1} + Y_{io})/2 - Y_{vddq_0} \) (5-2)
- \( Y_{decap} = (Y_{vddq_0} + Y_{vddq_1} + Y_{io})/2 - Y_{io} \) (5-3)
I/O pin impedance

I/O pin impedance

Imaginary part of I/O pin impedance
Power/ground impedance when I/O pin is open
I/O pin capacitance
Vccq parasitic resistance

- Real part of total on-die Vccq decoupling
  - Input low
  - Input high

- Real part of total on-die Vccq decoupling (excluding C_comp effects)
  - Input low
  - Input high

- Real part of on-die Vccq parasitics (excluding C_comp and lumped decap cell effects)
  - Input low
  - Input high

Everything included

C_comp effect excluded

C_comp and lumped decap cell effect excluded
Vccq parasitic capacitance

- Everything included
- C_comp effect excluded
- C_comp and lumped decap cell effect excluded
Pull_up and Pull_down resistance
Pull_up and Pull_down capacitance
Conclusions

- \( C\_\text{comp} \) is frequency and state dependent
- \( C\_\text{comp} \) split ratio is also frequency and state dependent
- \( C\_\text{comp} \) and its split ratio are very important factors for correct power integrity simulations
- Existing \( C\_\text{comp} \) and I/V table may not completely model the frequency dependent property of I/O buffer, even at steady state.