Macromodeling and Multi-GHz Interconnection Simulation

Asian IBIS Summit

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December 2005

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Agenda

- Transistor-Level Model versus Behavior-level Model
- Macromodeling of Complex IOs
- Lab Correlation for Macromodels
- Multi-GHz System Interconnect Simulation
- Conclusions

Transistor-level model and Behavior-level model

- SPICE Model
  - Good accuracy
  - models are derived from transistor-level netlist and layout
  - Relatively long simulation time and sometimes convergence problems
  - Intellectual property protection concerns

- IBIS Model
  - Models are derived from measurements and/or full SPICE model simulations
  - Fast simulation run time
  - Model must be verified, sometimes be converted and modified before usage
  - Difficult in Modeling complex transceiver buffers

- MacroModel
  - Fast simulation run time
  - A simply modeling solution for complex IOs ,such as pre-emphasis buffers
  - Macromodel is based on IBIS model

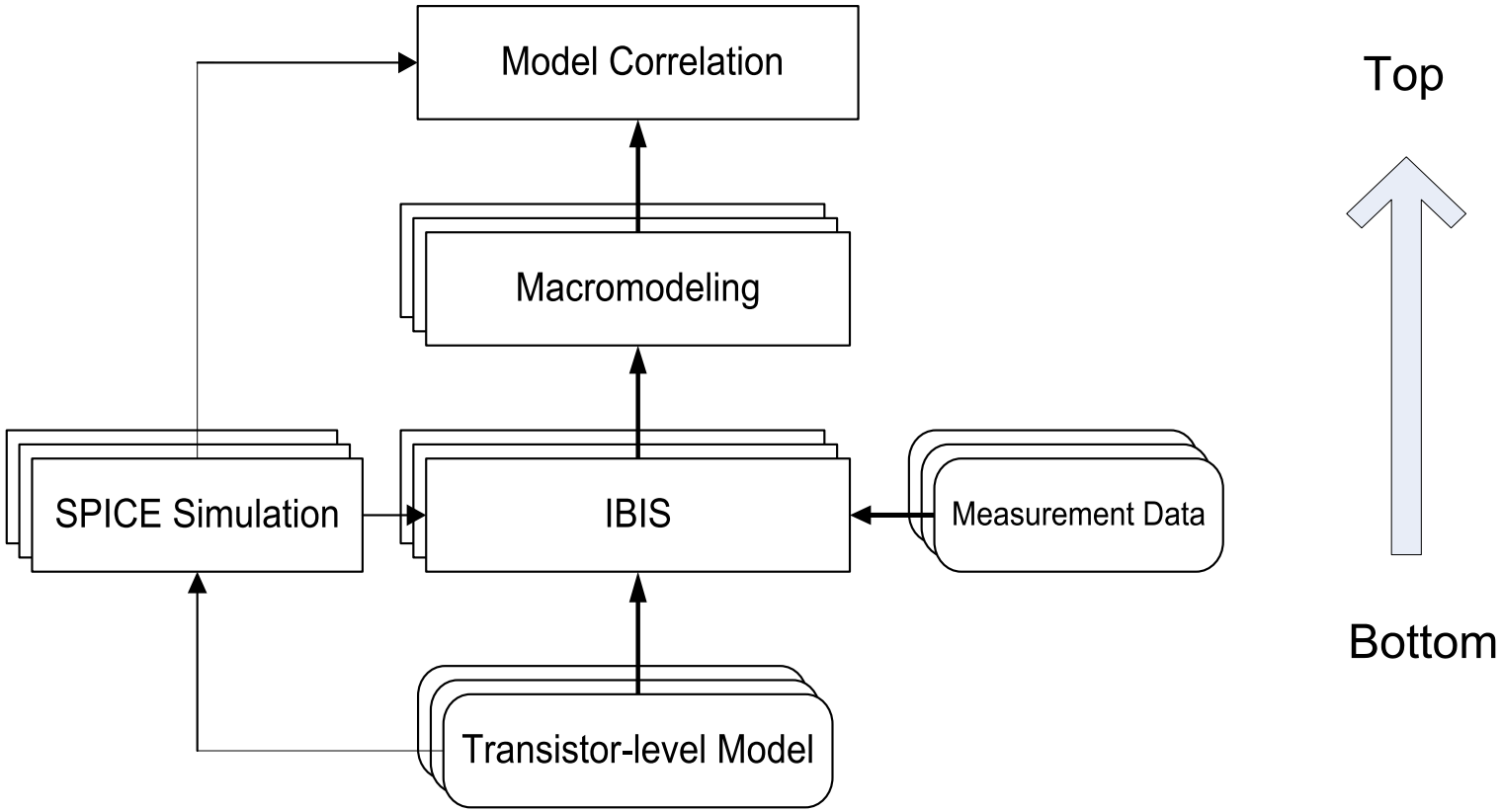
Modeling methodology

- Modeling is quite involved, it covers active devices as well as passive devices, such as package, transmission line, connector, via, and plane etc..
- Not all modeling methods are the same. They have tradeoffs and are suitable for different applications.
- There are behavioral IBIS and structural Spice modeling for active devices. Spice model is appropriate for demanding situations, while IBIS model is often used in system and board level simulation.
- Circuit simulators can run both IBIS and Spice. Different simulators have different characteristics.

Modeling of complex IOs

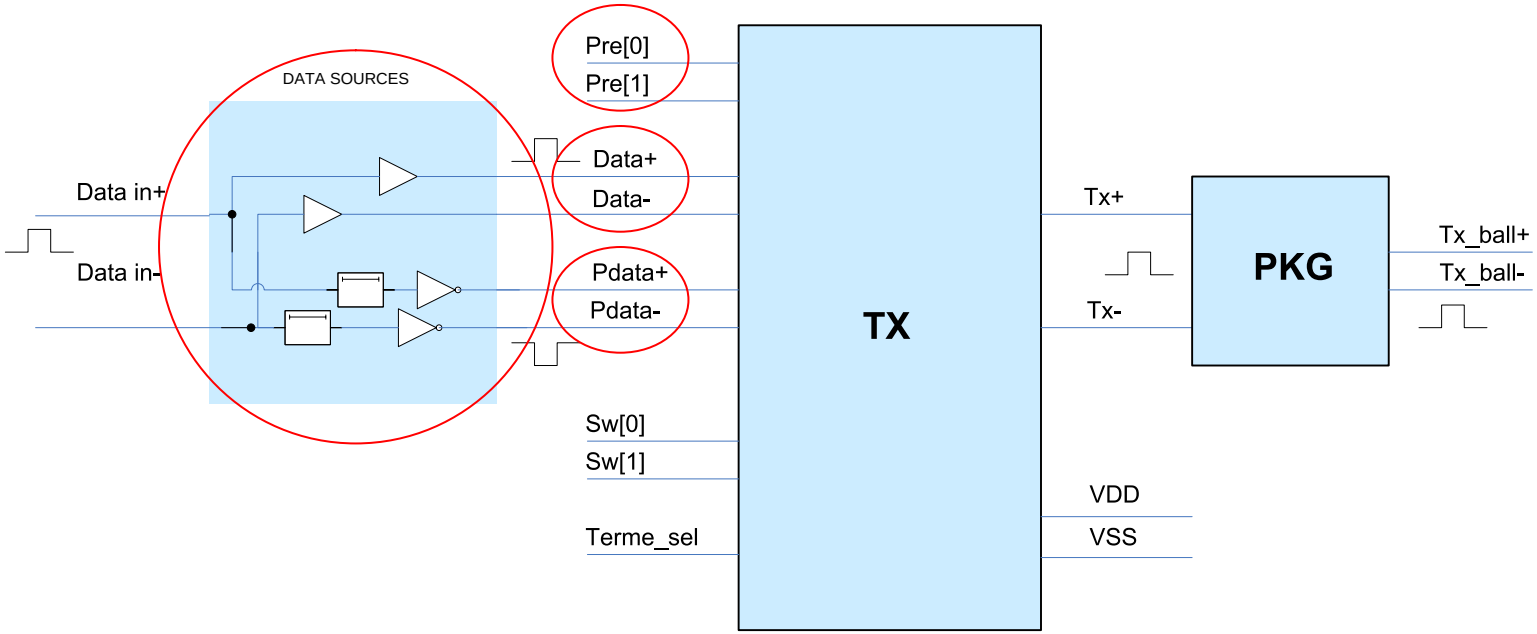
- IBIS Multi-lingual Modeling
  - VHDL-AMS
  - Verilog-AMS
  - Incorporating SPICE Subcircuits
  - Incorporating External Model
  - Incorporating S-Parameter Model
- Macromodeling based on IBIS
  - A simply solution for complex buffers
  - Combining spice subcircuits and behavioral models

Macromodeling and its correlation flow



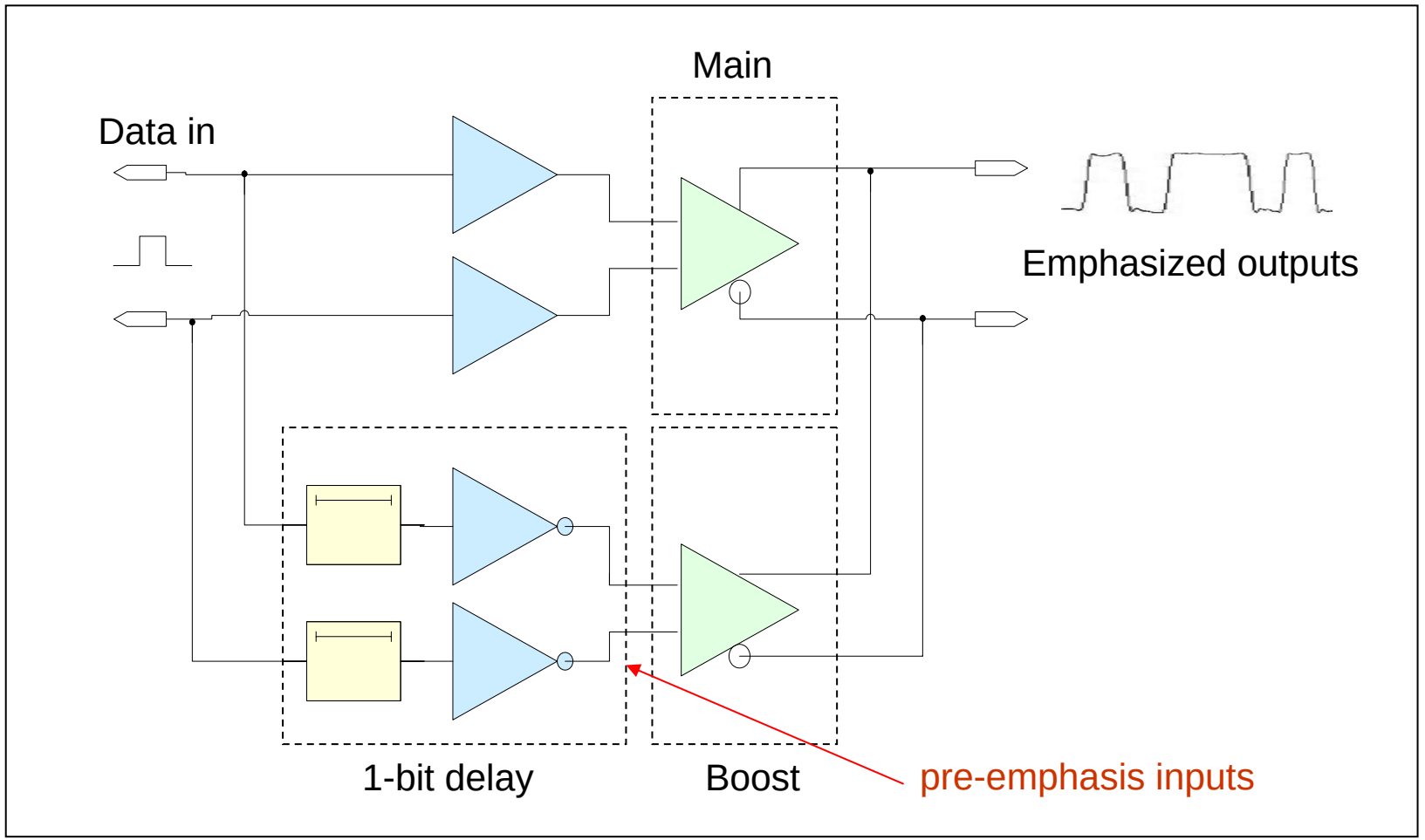
For behavior-level modeling , correlation is necessary.

Macromodeling of SERDES



The structure of transmitter device

Pre-emphasis



Example Macromodel for Pre-emphasis

- Normal IBIS data

```
[Model]        TX_sample
Model_type     Output

C_comp                    0.26pF   0.18pF   0.30pF
[Voltage Range]           1.2V     1.14V    1.26V
|
[Pulldown]
| Voltage      I(typ)       I(min)       I(max)
|
[Pullup]
| Voltage      I(typ)       I(min)       I(max)
|
[Ramp]
|              typ          min          max
dV/dt_r     0.36/0.10n    0.35/0.11n    0.37/98.79p
dV/dt_f     0.33/99.12p   0.33/96.04p   0.33/0.10n
R_load = 5k
```

- Place in macromodel template
  - (Pullup (ReferenceVoltage
  - rt
  - (Pulldown (VICurve
  - (Ramp (dt
  - (C_comp and/or padcap
- Additional data
  - Bitp ----- Unit interval
  - eqdb ----- Pre-emphasis db
  - Scale ----- Vp-p

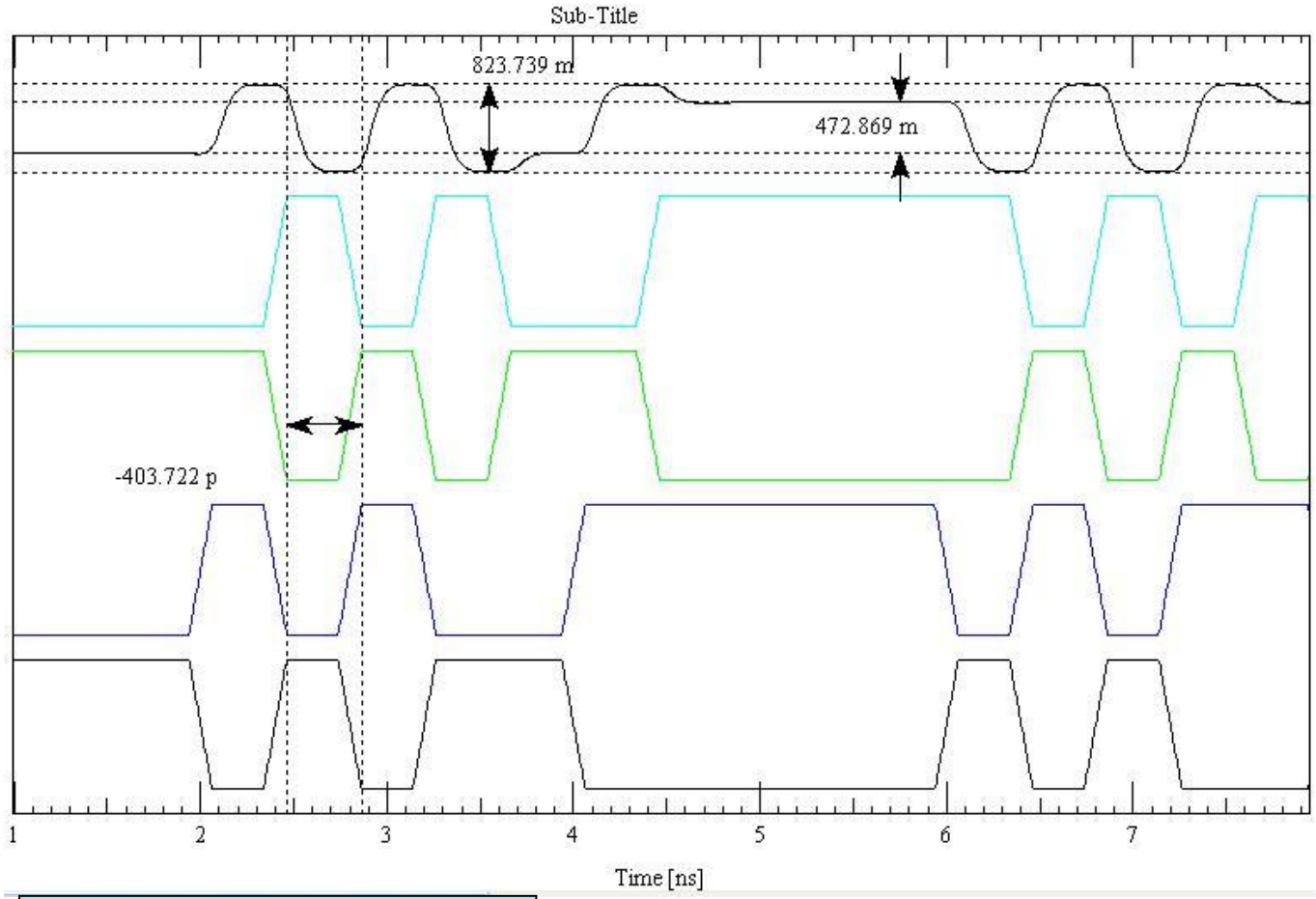
MGH MacroModel templates can be downloaded from

http://www.allegrosi.com

http://www.specctraquest.com

http://register.cadence.com/register.nsf/macromodeling?openform

Simulation of Pre-emphasis using marcormodel



Pre-emphasis output

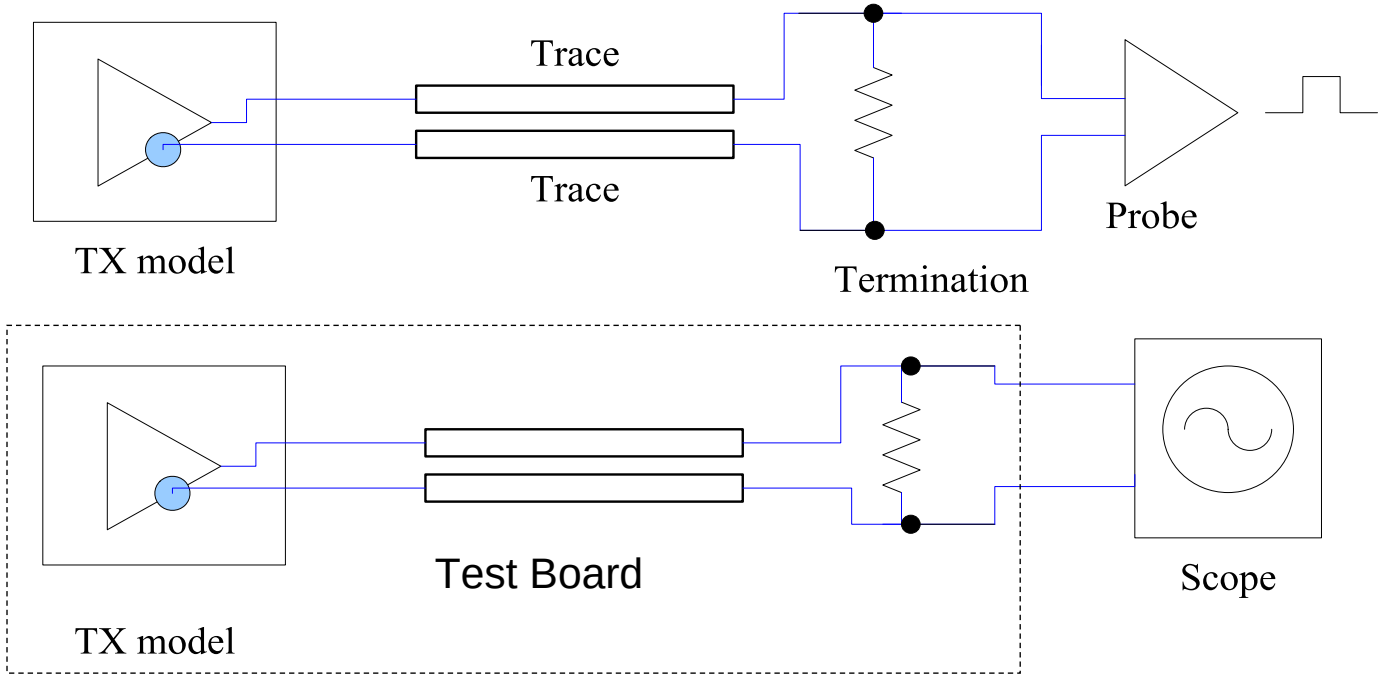
delay_1bit

data in-

data in+

UI=400ps PRBS K28.5

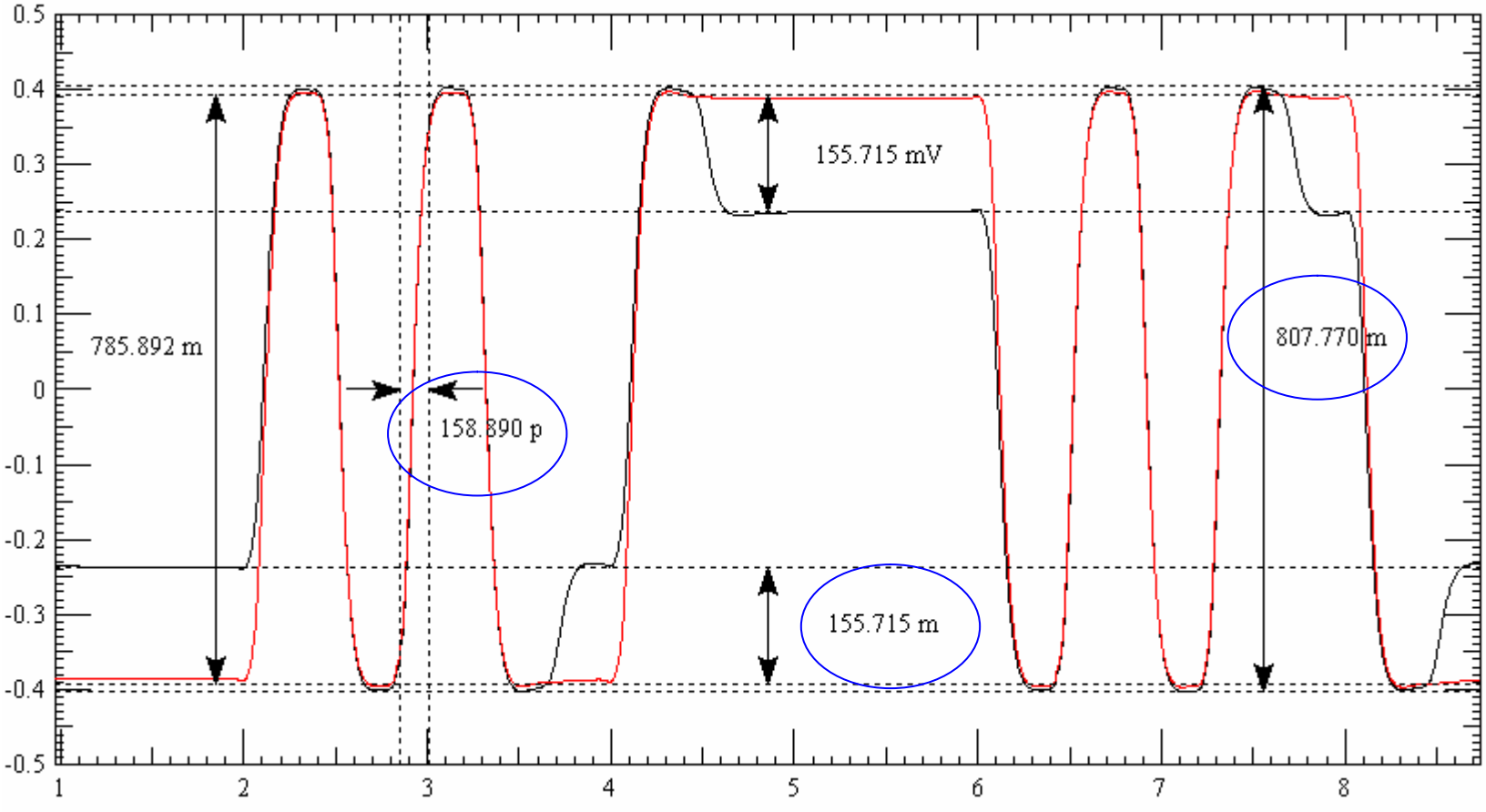
Macromodel Validation setup



Correlations with lab measurements and HSPICE simulations

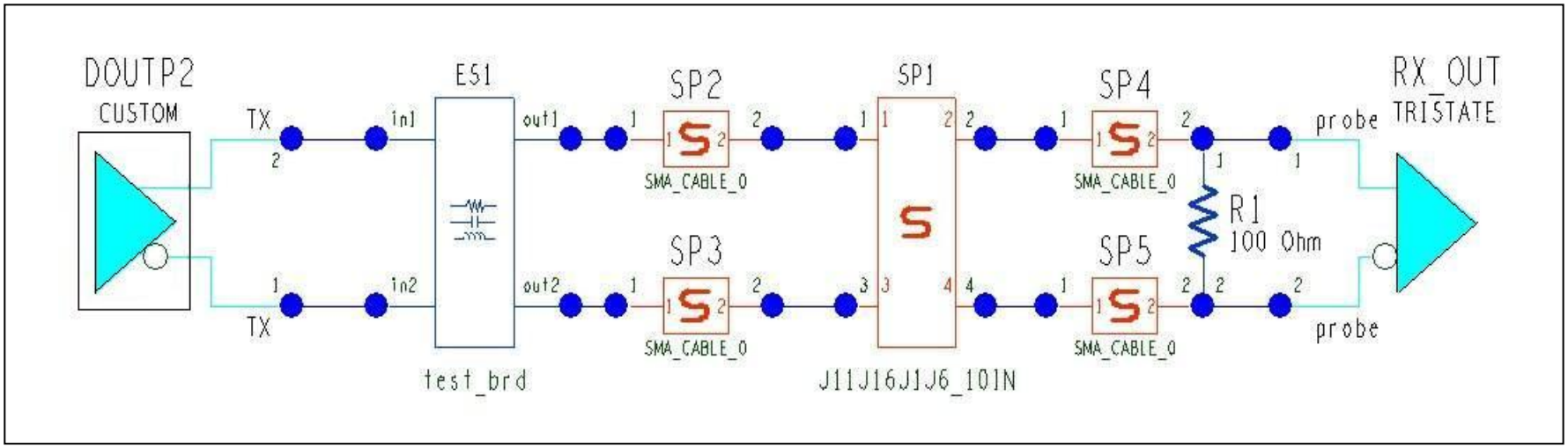
Macromdeling simulation w./wo. pre-emphasis

Red Curve: No Pre-emphasis Black Curve: 40% Pre-emphasis



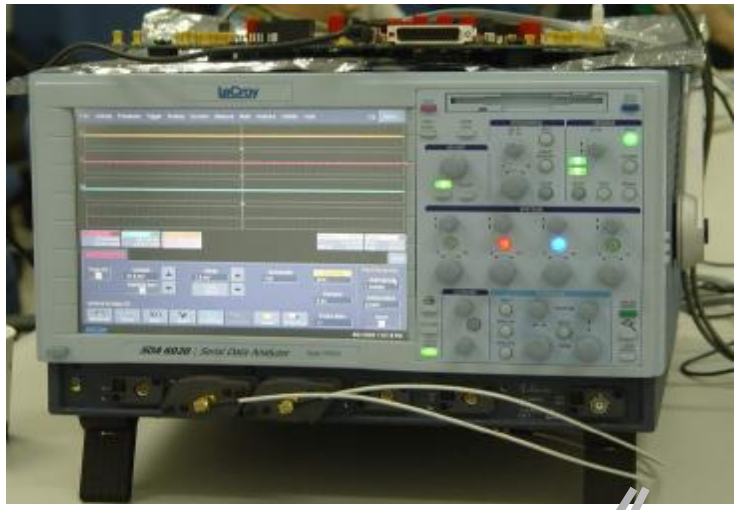
Lab Correlation for Macromodels

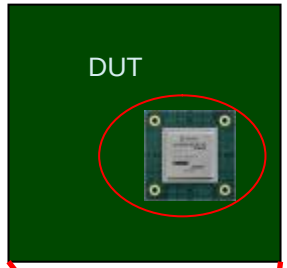
1 Simulation using HSPICE models
2 Simulation using macrmodels
3 Correlate with laboratory measurement

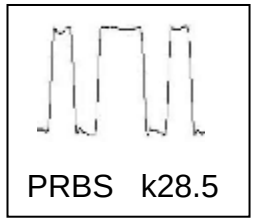


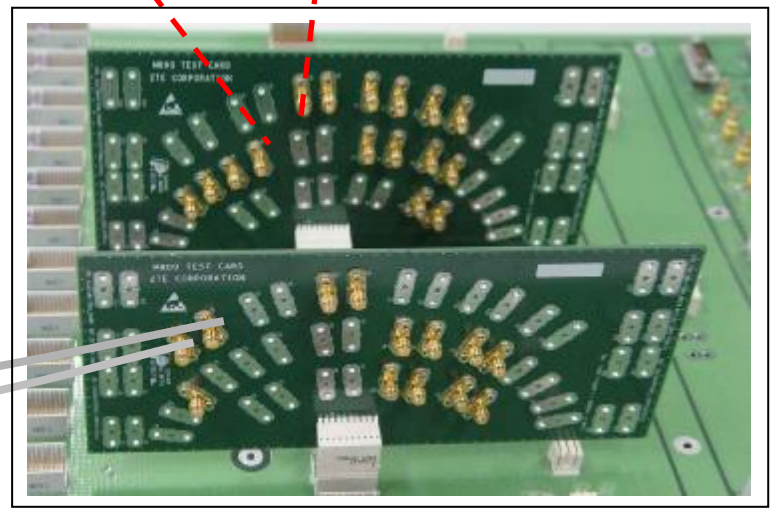
Measurement versus Simulation

Laboratory and measurement setup







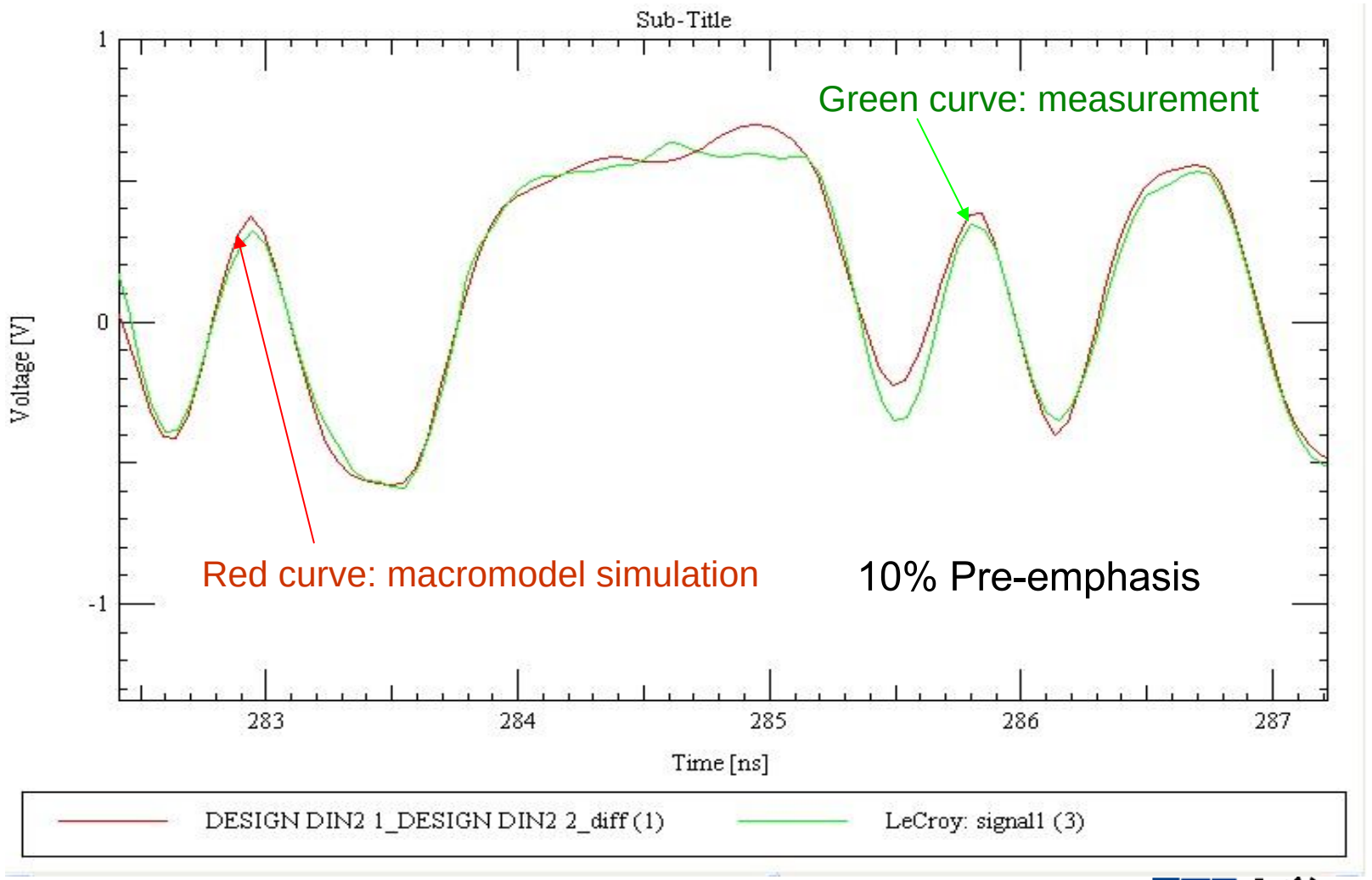


The backplane has 10’’ of stripline

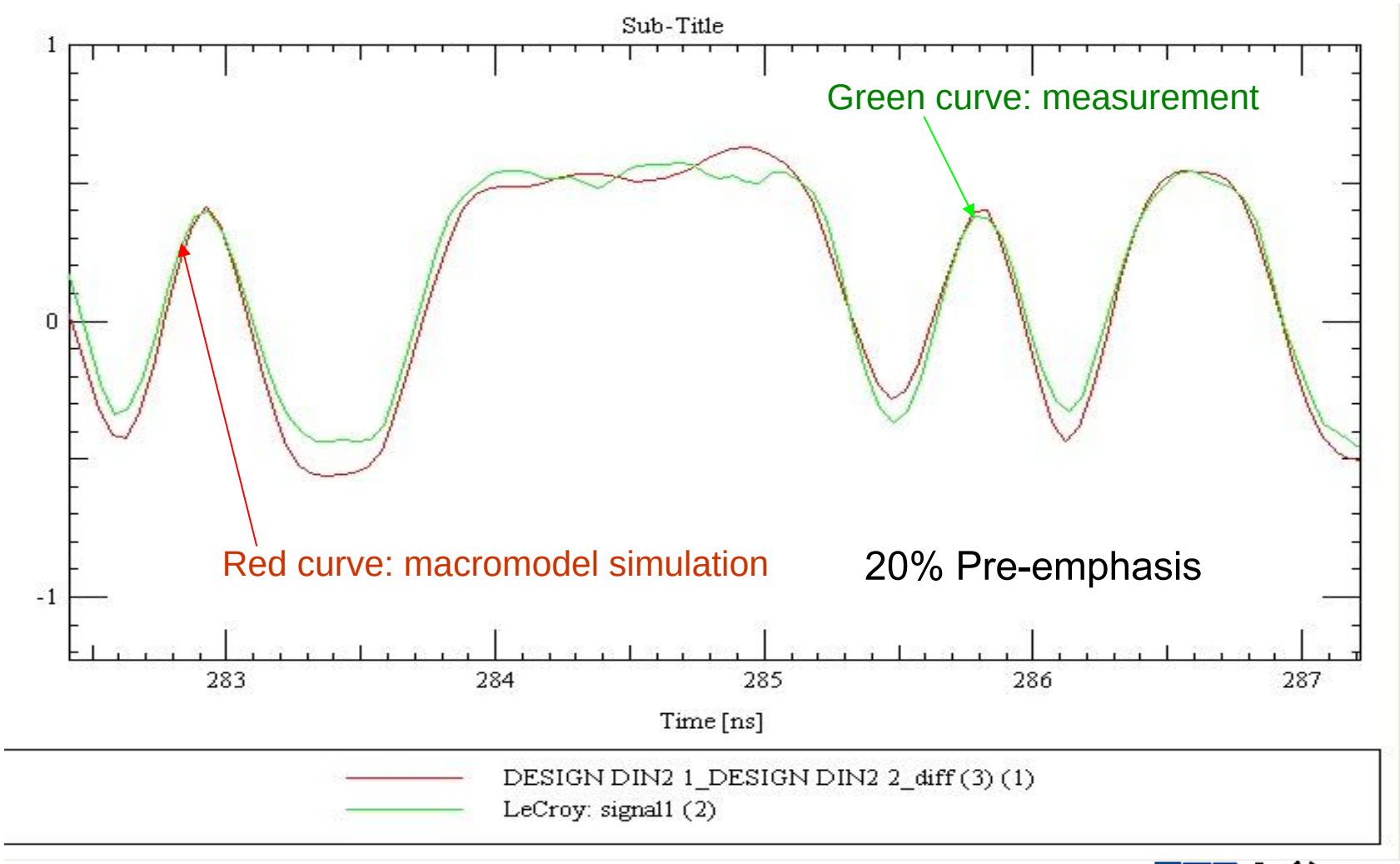
The daughter card has 3” of stripline

Data rate is 3.125Gb/s

Lab Correlation for Macromodels

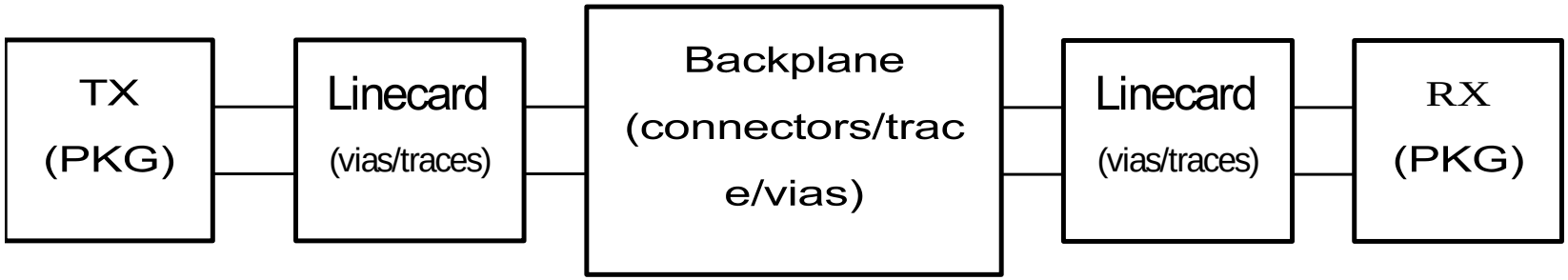


Lab Correlation for Macromodels



Multi-GHz System Interconnect Simulation

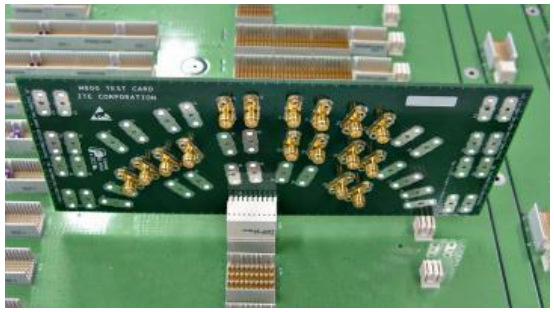
- Multi-GHz System Interconnect Simulation includes:
  - Transceiver Modeling
  - Transceiver Package Modeling
  - Interconnection (Traces, Vias, Connectors) Modeling



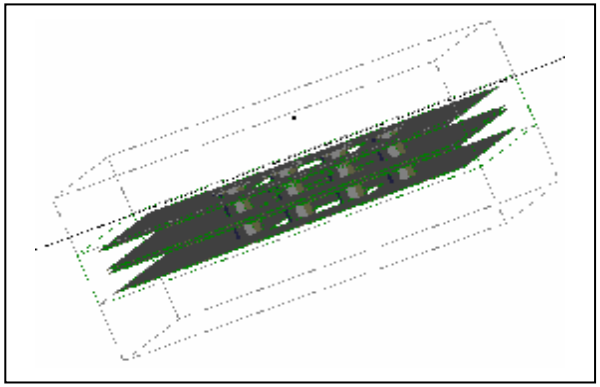
Multi-GHz System Interconnect Simulation

- Extracting models using 2D/3D EM solver
- Correlation based on VNA and TDR/TDT measurements
- SI/PI/EMC Simulations
- Eye diagram analysis and design margin budget
- Optimization

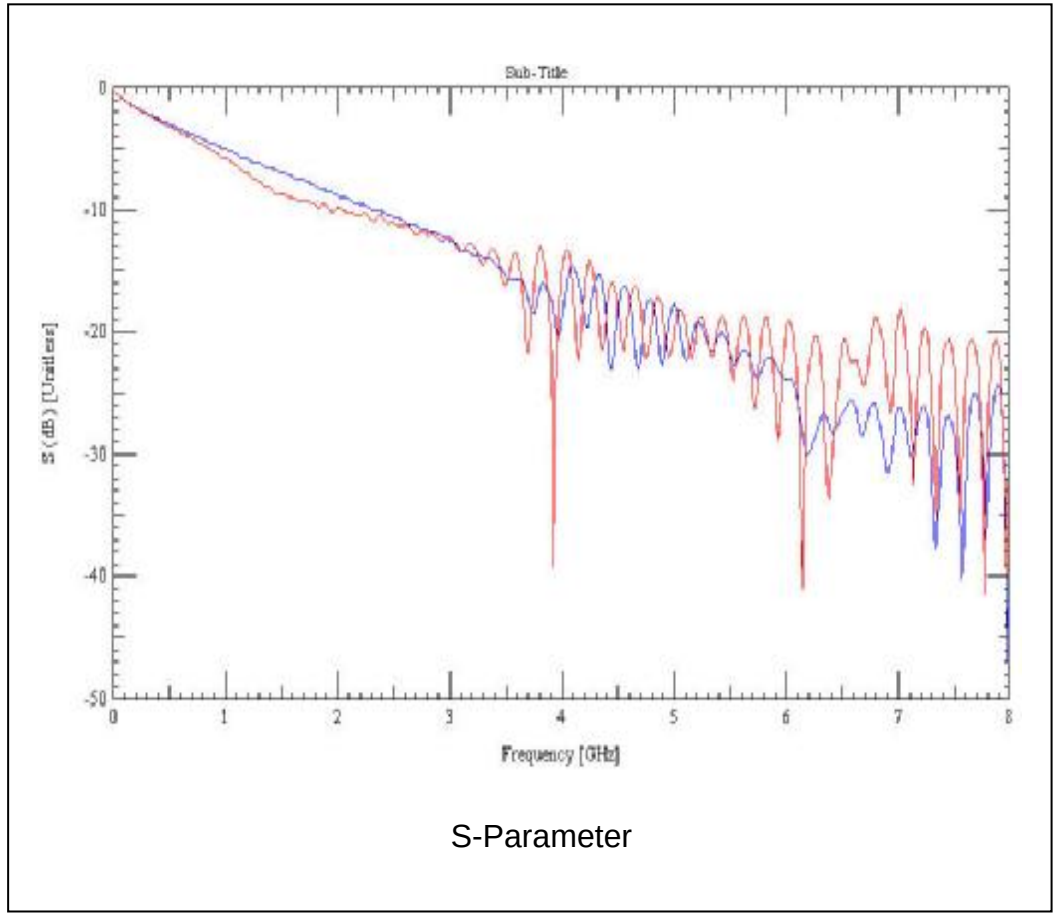
Measurement modeling



Measurement setup



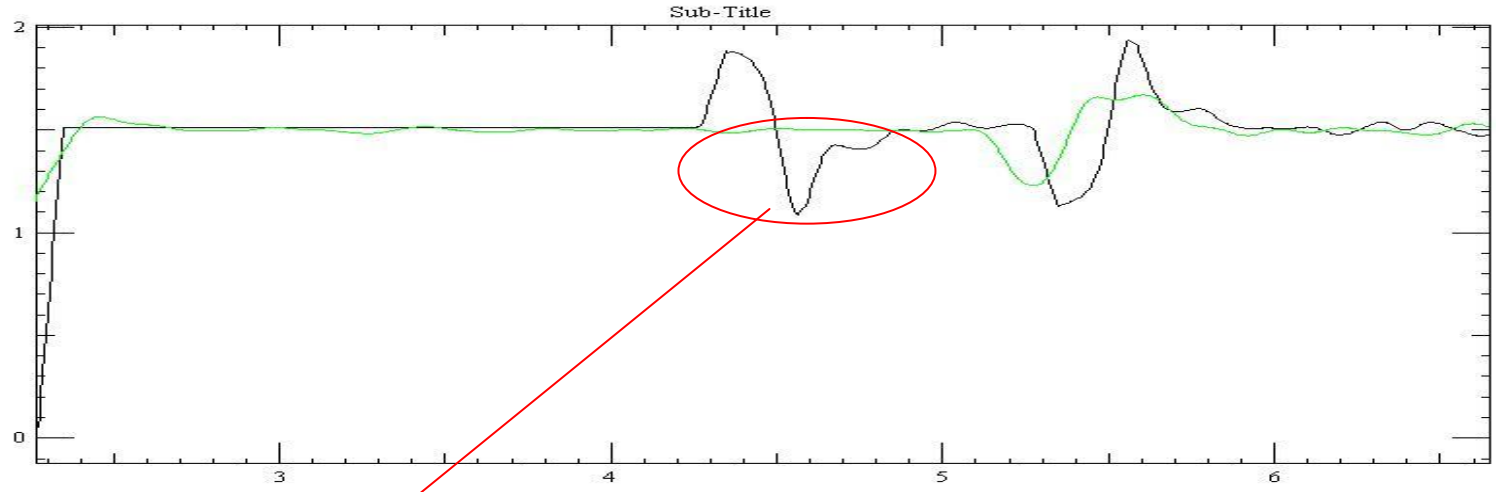
3D EM Solver Modeling

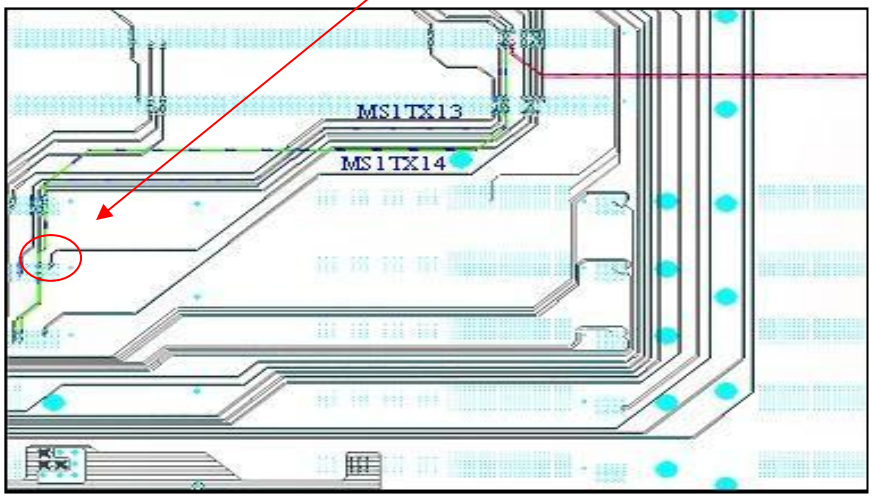


S-Parameter

S21 data comparison between VNA measurement and Simulation

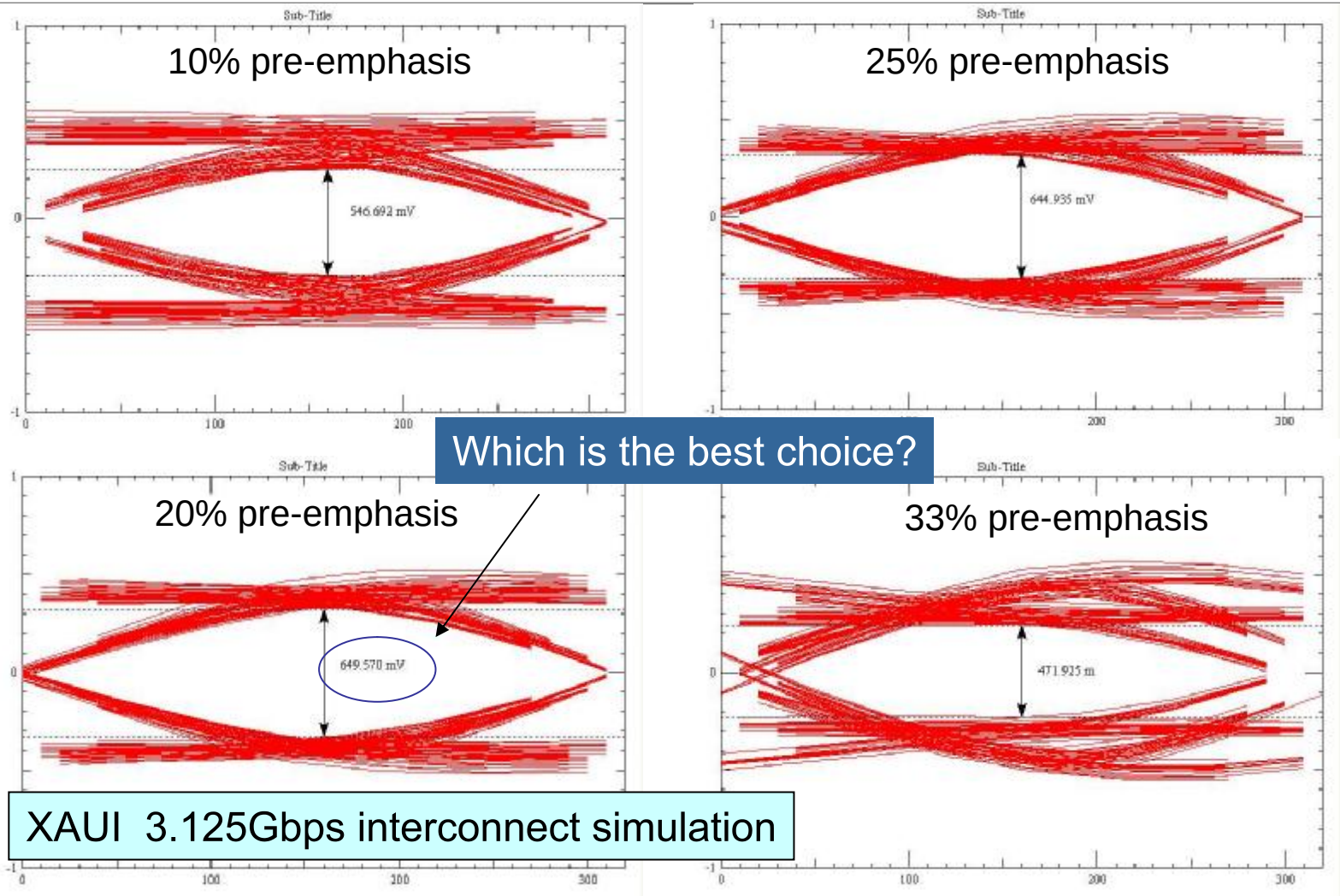
TDR optimization





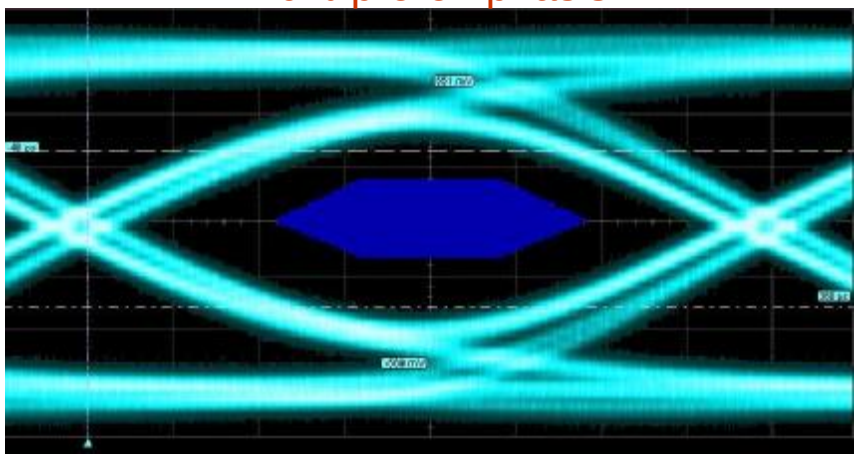
Impedance analysis of multi-GHz Interconnection is very important.

Macromodel application

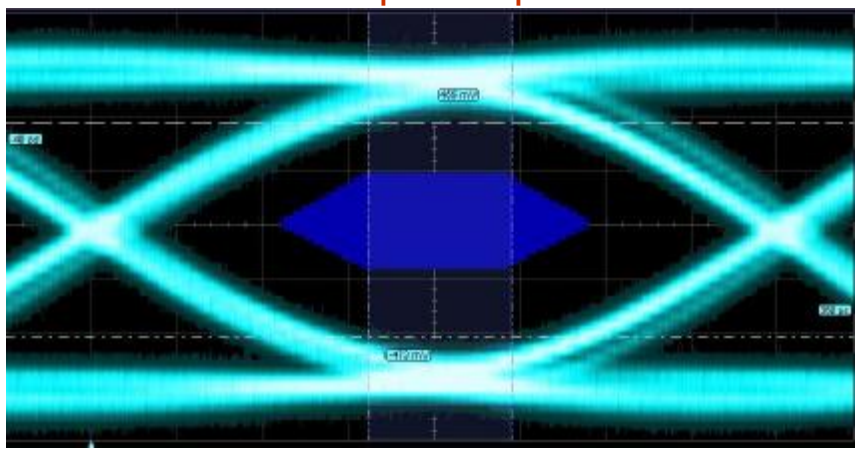


Correlation

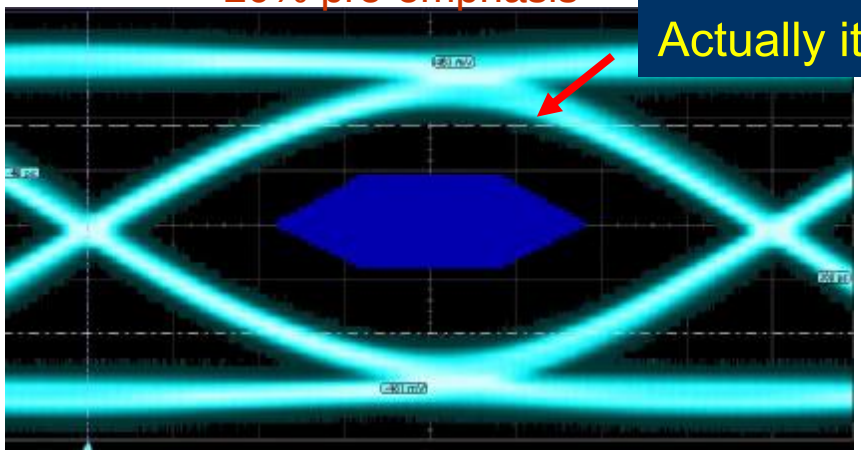
10% pre-emphasis



25% pre-emphasis

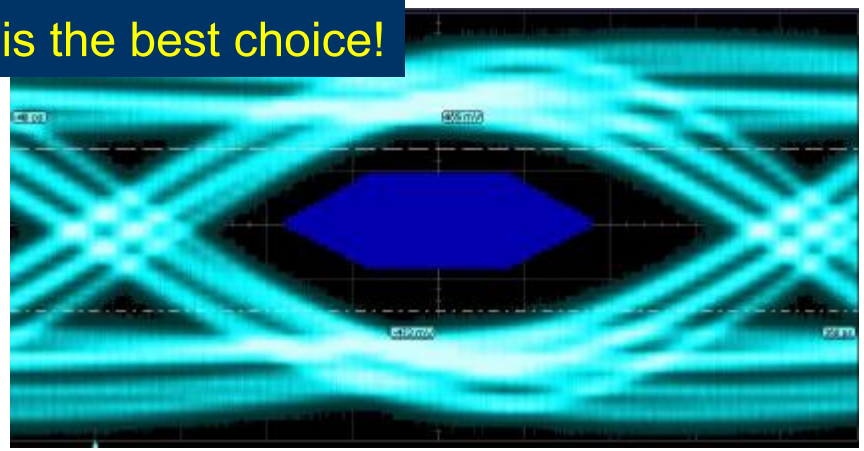


20% pre-emphasis



Actually it is the best choice!

33% pre-emphasis



Conclusions

- Choose an appropriate modeling method is critical for simulation. Otherwise simulation may not be accurate enough or too complex and time consuming.
- Macromodel is an efficient solution for complex IO modeling, provided it be validated before usage.
- MacroModel enables much shorter simulation time than transistor-Level spice model. They can be used for system design and post-layout analysis.
- MacroModeling is appropriate for what-if analysis due to its relative short run time and sufficient accuracy.
- For multi-GHz Interconnection optimization, active device modeling using marcomodels, PCB modeling using EM solver, and correlation based on lab measurements have been proved to be very effective.