Creating IBIS Models for Stacked-Die Packages

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Problem Statement

- Intel sells memory with several devices stacked inside a single package
- We receive bare die from several vendors
  - We receive IBIS models but no schematics
- Customers require IBIS models for new stacked-die package
Solution

• Use internal schematics plus vendor IBIS models to create a new netlist
• Simulate to generate IV and VT curves for new IBIS model
Methodology

• Generate two sets of IV and VT curves
  – Device A is active while device B is tri-stated
  – Repeat with device B active and A tri-stated
• Build new IBIS model using both curves
  – Assign D[0] to A active (with B tri-stated)
  – Assign D[7:1] to B active (with A tri-stated)
• Edit IBIS model to add model_selector
  – Change D[7:0] to use model_selector
  – Requires IBIS version 3.2 or higher
Data Bus Example

● BEFORE

[IBIS Ver] 2.1

... [Pin] signal_name model_name
B1   DQ0   Ab_output
B2   DQ1   Ba_output
B3   DQ2   Ba_output
B4   DQ3   Ba_output

At least one instance of each buffer
Manually add Model Selector

● AFTER

[IBIS Ver] 3.2

... [Pin] signal_name model_name
B1   DQ0   DQ
B2   DQ1   DQ
B3   DQ2   DQ
B4   DQ3   DQ

... [Model Selector] DQ
Ab_output Device A DQ
Ba_output Device B DQ
Ground Clamp Comparison

- New IBIS model reflects behavior of both die
- Device A ground clamp (-130mA)
- Device B ground clamp (-195mA)
- Combined ground clamp (-325mA)
AC Timing Comparison

- Original (single-die) pullup_on for device A
- Combined curve showing additional loading from device B
- Original device B
- Combined device B
Conclusion

• This document describes a methodology of generating a multi-die IBIS model from transistor netlists plus IBIS models

• Effects of multiple loads are accounted for
  – Power clamps for all devices are combined
  – Vt behavior accounts for additional loading

• Package parasitics can be handled using worst case loading or EBD format