



Verification of IBIS models

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Agenda

- Introduction
- Where to get IBIS models
- How to verify IBIS models
- Adding additional information
- Roadmap IBIS Development Studio



Where to get IBIS models

- Download from internet
 - Not always latest version on internet
- Contact component vendor(s)
- Create models from spice data
- Create models by measurement



How to verify IBIS models

- IBIS golden parser
- Visual verification
- Test IBIS model in simulator
- Compare IBIS model with measurement data



IBIS Golden parser

■ IBISCHK

- Is a program that parses the model file to verify that the file conforms to the IBIS specification. It is free, publically available executable code developed by contractors for the IBIS Open Forum.
- The official ibischk4 checks Version 1.1, 2.1, 3.2 and 4.0 level IBIS files. (Use -ebd and -pkg flags for .ebd and .pkg files.)

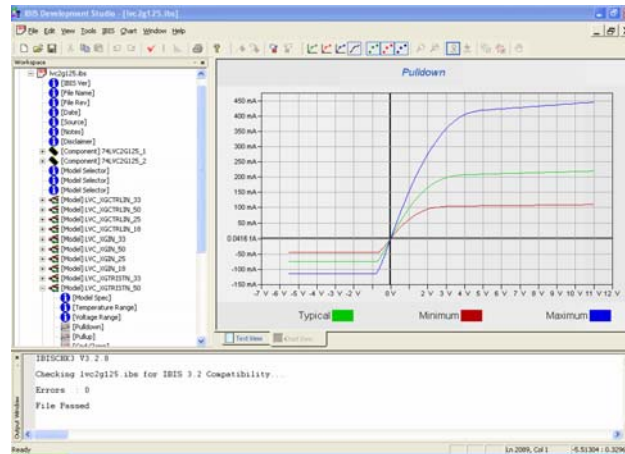


Visual verification

- To verify an IBIS model, a graphical view of the waveform(s) makes it easier
- In a graphical viewer of the IBIS models, the potential problems can be found easier.
- Free tools are available for visual verification of an IBIS model.
 - IBIS Development Studio
 - Visual IBIS editor



Graphical Viewer



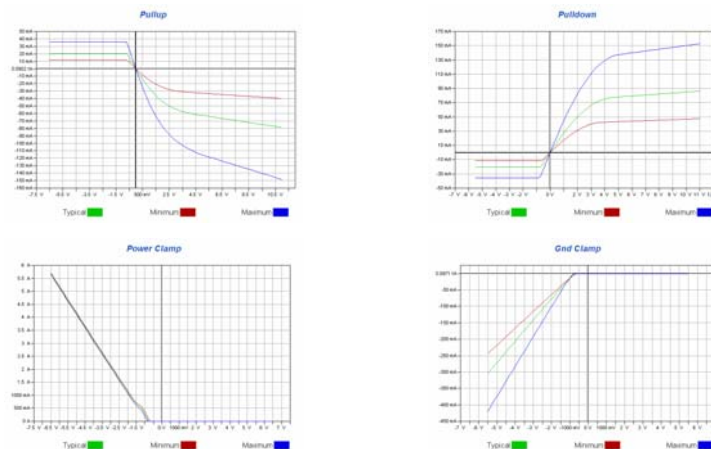
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Graphical view of I/V tables



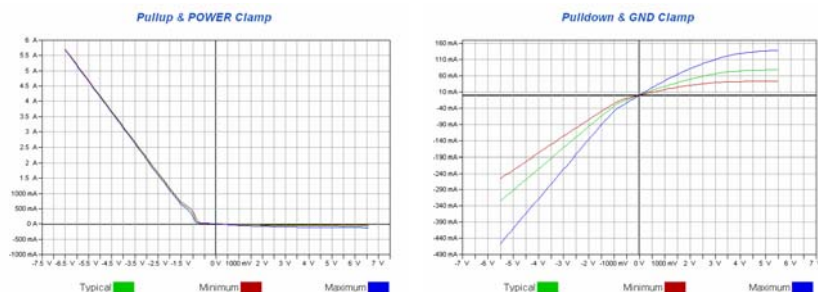
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Combine waveforms



Modify waveform

- Modify waveform in the ASCII file is difficult.
- It is easier to move points graphically
- Graphical editing functionality needed





Test IBIS model in simulator

- After graphical verification, the IBIS model must be tested in the simulator where you are going to use the IBIS model.
- Run the model with the standard test loads.
- Comparing the results against a transistor-level reference simulation using the same loads.



Compare IBIS model with measurement data

- The last step in the modeling process is to correlate the simulation results with actual silicon measurements.
- Correlation involves measuring the I-V curves and rise/fall times of an actual IC and verifying that they fall within the maximum and minimum values used in the IBIS model.
(In addition, for ICs in a motherboard or other test setup driving a known load, compare the oscilloscope waveforms with simulation waveforms using the same load.)



Adding additional info

- A IBIS model is the best place to define constraints needed for the SI simulator :

- | | |
|--------------------|--------------------------------|
| ■ S_overshoot_high | Static overshoot high voltage |
| ■ S_overshoot_low | Static overshoot low voltage |
| ■ D_overshoot_high | Dynamic overshoot high voltage |
| ■ D_overshoot_low | Dynamic overshoot low voltage |
| ■ D_overshoot_time | Dynamic overshoot time |
| ■ Vmeas | Measurement voltage for timing |



Constraints in IBIS

- Most SI simulators uses a constraint spreadsheet for defining constraints.
- Constraints for under-/over-shoot should come from the IBIS model.
- Most IBIS models does not contain this information.
- This information can be found in the datasheet, or contact the component vendor.



Roadmap IBIS Development Studio

- Test model in simulator (ICX / ePlanner / Hyperlynx / simulators) within IBISDS
- Enhanced features for model wizard
- XML output of IBIS model
- Other improvements suggested by IBISDS users (ibisds@edality.com)
- For more info, visit us at <http://www.edality.com>