



# Parametric Models in IBIS Multilingual Framework

F.G.Canavero<sup>1</sup>, I.A.Maio<sup>1</sup>, B. Ross <sup>2</sup>, **I.S.Stievano**<sup>1</sup>

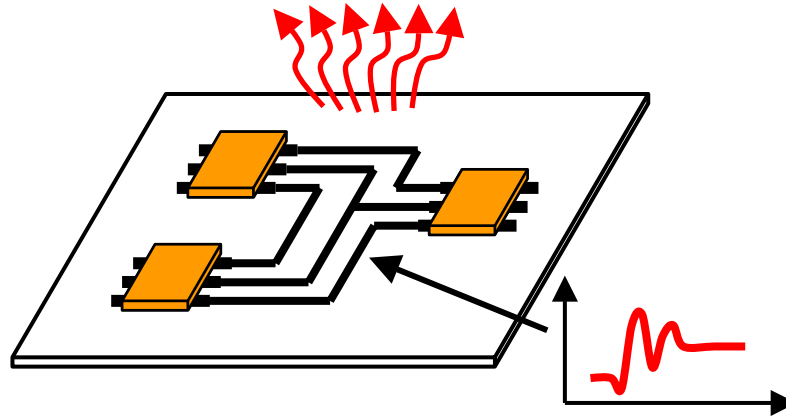
<sup>1</sup> Politecnico di Torino, Italy, <sup>2</sup> Teraspeed Consulting Group LLC (USA)

[igor.stievano@polito.it](mailto:igor.stievano@polito.it)

<http://www.eln.polito.it/research/emc>

# Introduction (i)

## IBIS Implementation of I/O buffer Parametric Models for High-Performance SI and EMC simulations



Improved modeling of latest technologies and high-order effects

- LVDS drivers with pre-emphasis,
- DDR memories,
- Power supply ports, etc ...

# Introduction (ii)

## **$M\pi log$ - Macromodeling via parametric identification ( $\pi$ ) of LOfic GAtes**

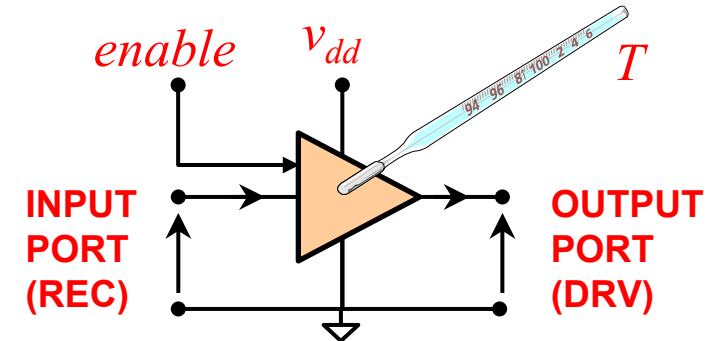
### Available applications:

- Single-ended CMOS
- **Macromodels** of I/O ports
  - Inclusion of slowly-varying **device parameters** (eg, temperature)
  - Inclusion of the **power-supply voltage** variation
  - Models of the **power supply port**
  - Models of **tristate drivers**

[I.S.Stievano, I.A.Maio, F.G.Canavero, " $M\pi log$ , Macromodeling via Parametric Identification of Logic Gates," Trans. Of Adv. Pack., 2003 (in press)]

- Models of **LVDS** devices

[I.S.Stievano, C.Siviero, I.A.Maio, F.G.Canavero, "Modeling of the Static and Dynamic Behavior of Differential Drivers," Proc. of EMC-Compo 2004]

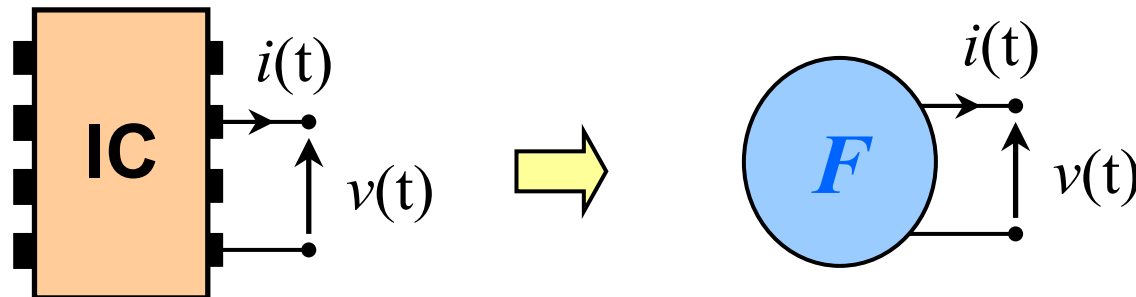


# $M\pi log$ review (i)

**$M\pi log$  - Macromodeling via parametric identification ( $\pi$ ) of **L**Ogic **G**ates**

## What is it ?

A **mathematical expression** reproducing the electrical behavior of the device



$$i = F(v, d/dt)$$

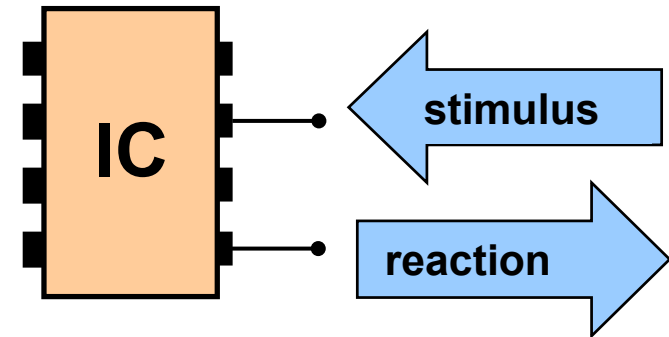
Nonlinear dynamic relationship



# M $\pi$ log review (ii)

## How does it work ?

- Real Device (or its physical model) is conveniently **stimulated**
- **Reaction** (port transient responses) is used to build the model



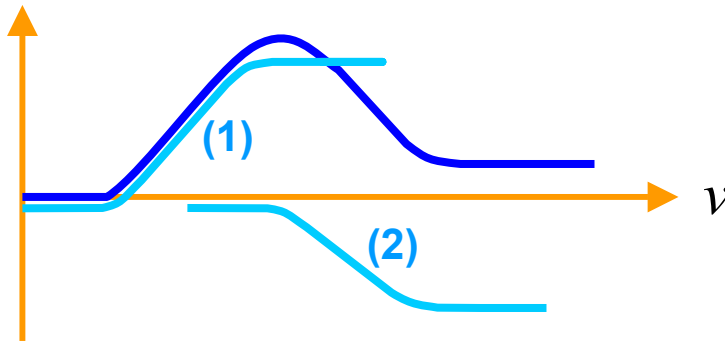


# $M\pi log$ : what is the output ?

**Model structure:**  $F$  is a  $\Sigma$  nonlinear **Basis Functions** (various types)

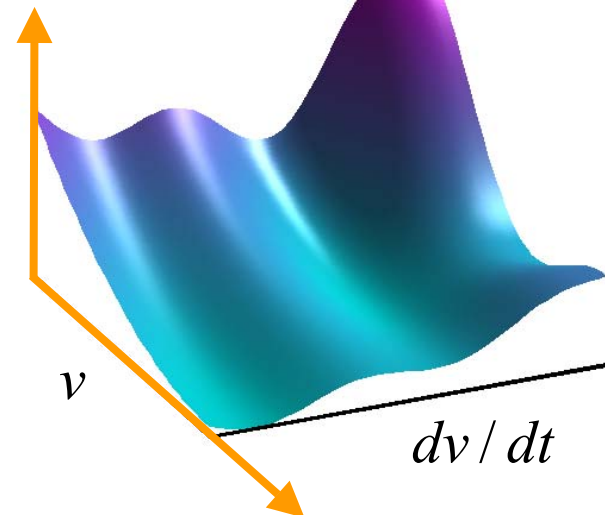
e.g., 
$$i = \underbrace{-a_1 \tanh\{c_1 v + b_1\}}_{(1)} + \underbrace{a_2 \tanh\{c_2 dv/dt + b_2\}}_{(2)}$$

$$i = F(v, dv/dt)$$



unknown parameters: **amplitude, position, spreading**

$$i = F(v, dv/dt)$$

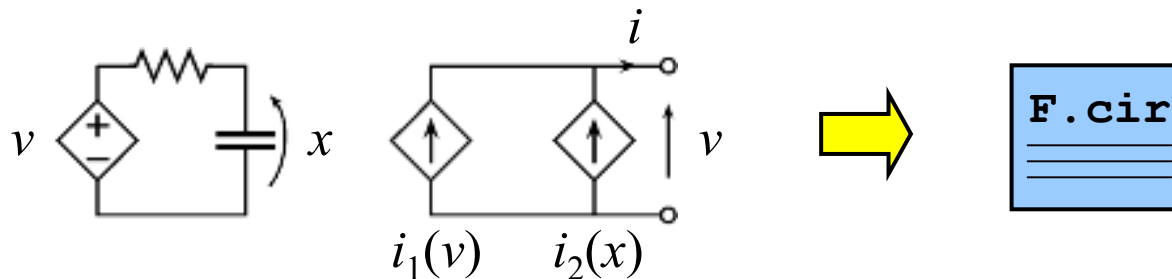




# $M\pi log$ : implementation

$$i = \underbrace{-a_1 \tanh\{c_1 v + b_1\}}_{i_1} + \underbrace{a_2 \tanh\{c_2 dv/dt + b_2\}}_{i_2}$$

## (a) CIRCUIT INTERPRETATION & SPICE IMPLEMENTATION



## (b) DIRECT EQUATION DESCRIPTION/IMPLEMENTATION: VHDL-AMS and IBIS Multilingual Extension

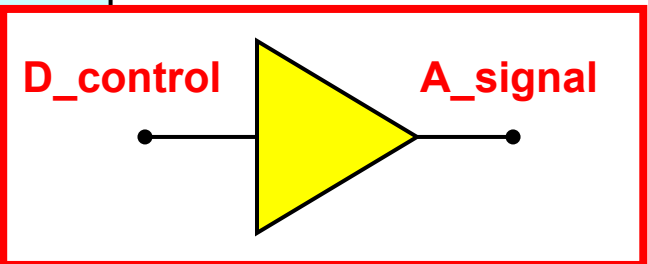
for  ICX Ver. 3.2 simulator



# IBIS Multilingual Extension

```
[IBIS Ver]    4.0
[File name]  driver_test.ibs
[File Rev]   0.0
[Date]       28/01/2004
|*****|
[Component]  DRIVER
[Manufacturer] Polito
[Package] ...
...
[Pin] signal_name model_name R_pin L_pin C_pin
1  vout      MODEL_PAR
|*****|
[Model] MODEL_PAR
Model_type  Output
Polarity    Non-Inverting
...
[External Model]
Language VHDL-AMS
|
| corner_name  file_name  circuit_name
Corner Typ    driverX.vhd  driverX(bufferbehav)
|
|   d_control a_signal
Ports D_control A_signal
|
[End External Model]
```

Driver\_test.ibs



**NOTE:** some example syntax details differ slightly from the approved IBIS Version 4.1 specification





# VHDL-AMS Model Implementation (i)

**Digital  
to analog  
conversion**

```
entity driverX is
  generic (
    Ts: real := ...
  )
  port(
    d_control : in std_logic;
    terminal a_signal : electrical);
end entity driverX;

architecture bufferbehav of driverX is
  quantity Vu_ref across i through a_signal
  to Electrical_ref;

  ...

  --- w1_01 low to high transition
  constant w1_01 : real_vector := ...

  InputBITSTR: process (d_control)
  begin
    if (d_control'event and d_control = '0') then
      flag <= 10;
      trans_inst <= now;
    elsif (d_control'event and d_control = '1') then
      flag <= 01;
      trans_inst <= now;
    end if;
  end process InputBITSTR;

  ...
```

driverX.vhd

1



# VHDL-AMS Model Implementation (ii)

**Analog  
parametric  
model**

```
...
...
...
driverX.vhd
...
if (d_control = '0' and flag = 10) use
  w1 == Lookup("Vt", now-trans_inst, w1_10, tw);
  w2 == Lookup("Vt", now-trans_inst, w2_01, tw);
elsif (d_control = '1' and flag = 01) use
  w1 == Lookup("Vt", now-trans_inst, w1_01, tw);
  w2 == Lookup("Vt", now-trans_inst, w2_10, tw);
end use;

f1 == -a1*(2/(1+exp(-2*c1*Vu_ref+...))-1) + ...
f2 == ...
i == w1*f1 + w2*f2

end architecture bufferbehav;
```

Example representation for  
CMOS single ended drivers

$$i = w_1(t)f_1(v, dv/dt) + w_2(t)f_2(v, dv/dt)$$

2



## Example 1 (i)

### DEVICE

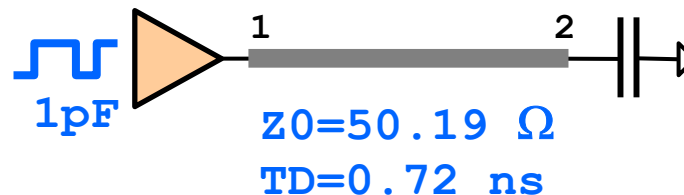
High-speed IBM CMOS Driver ( $V_{dd}=1.8V$ )

### PARAMETRIC MODEL

1 (2) basis functions for  $f_1$  ( $f_2$ ) and dynamic order 1

[I.S.Stievano et Al., "Parametric Macromodels of Drivers for SSN Simulations," Proc. of IEEE International Symposium on EMC, Boston, MA, USA, Aug. 18-22, 2003]

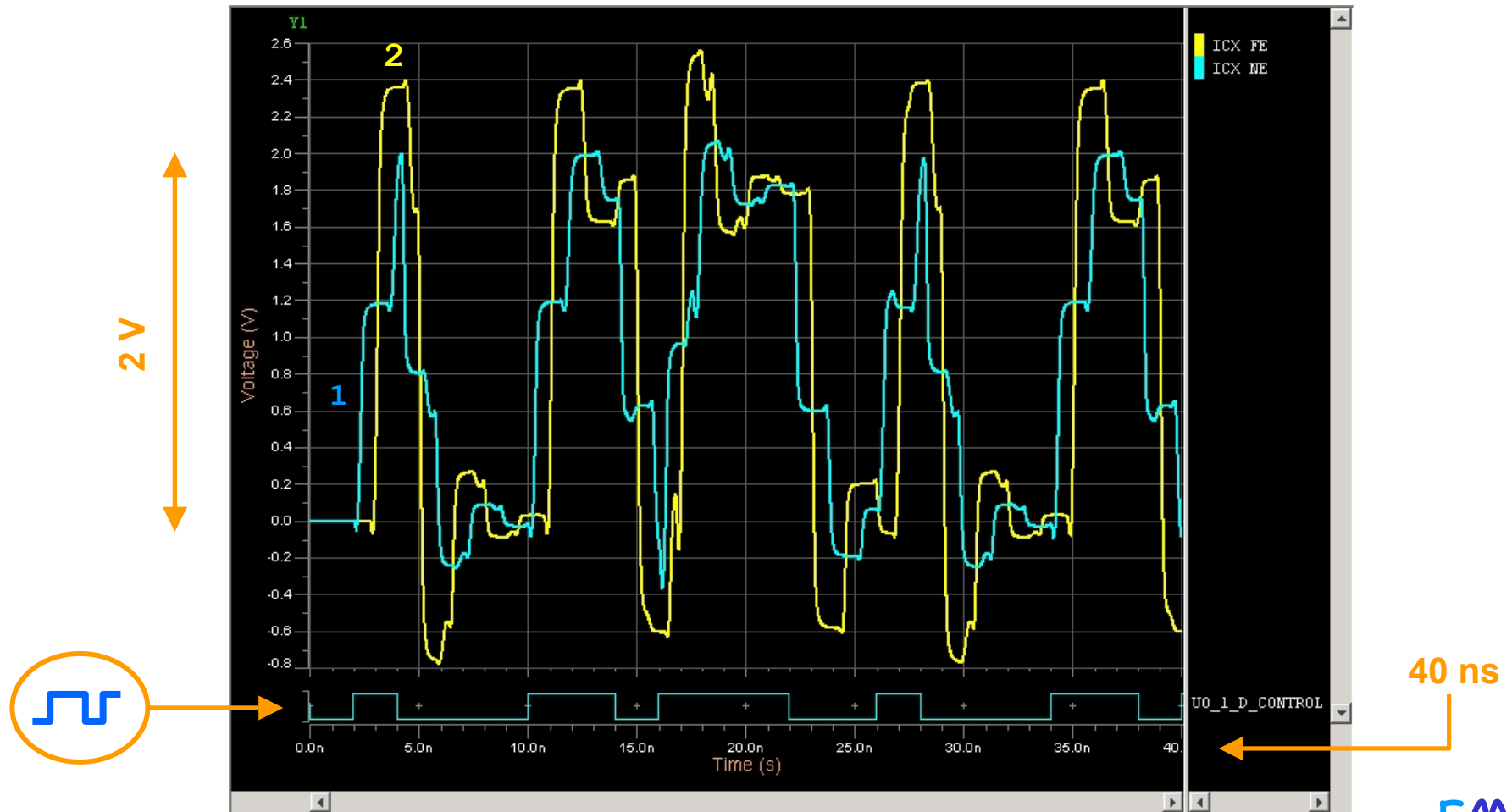
### TEST CIRCUIT





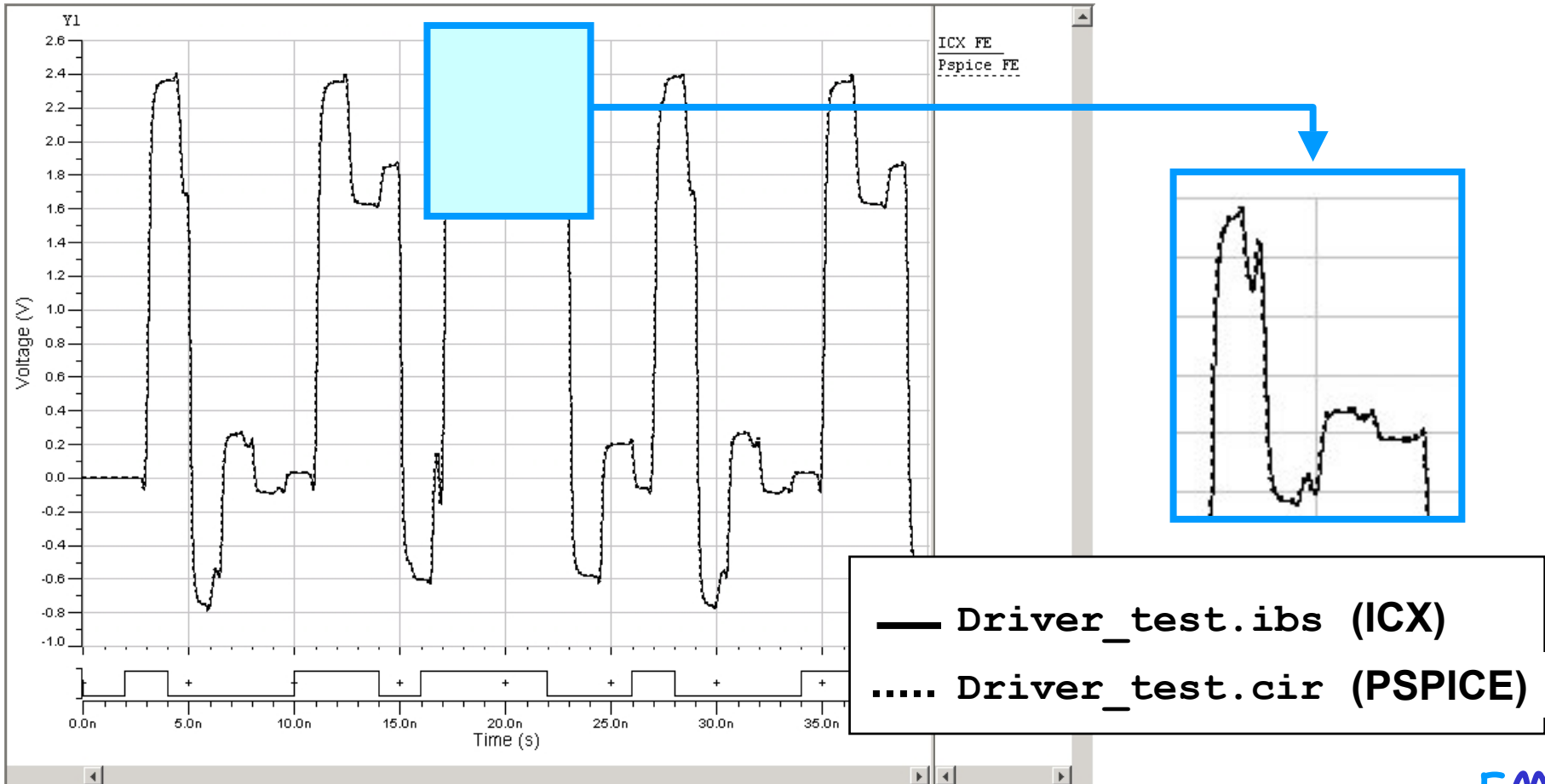
## Example 1 (ii)

Driver\_test.ibs simulation: ICX



## Example 1 (iii)

### Comparison of Driver\_test.ibs & Driver\_test.cir





## Example 2 (i)

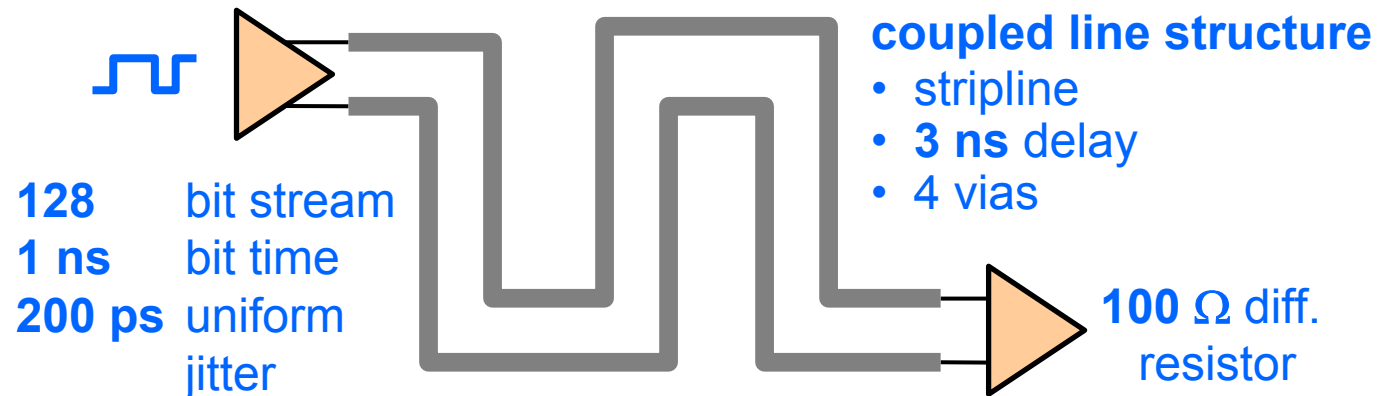
### DEVICE

Fairchild FIN1001 ( $V_{dd}=3.3V$ ) LVDS  
High Speed Differential Driver

### PARAMETRIC MODEL

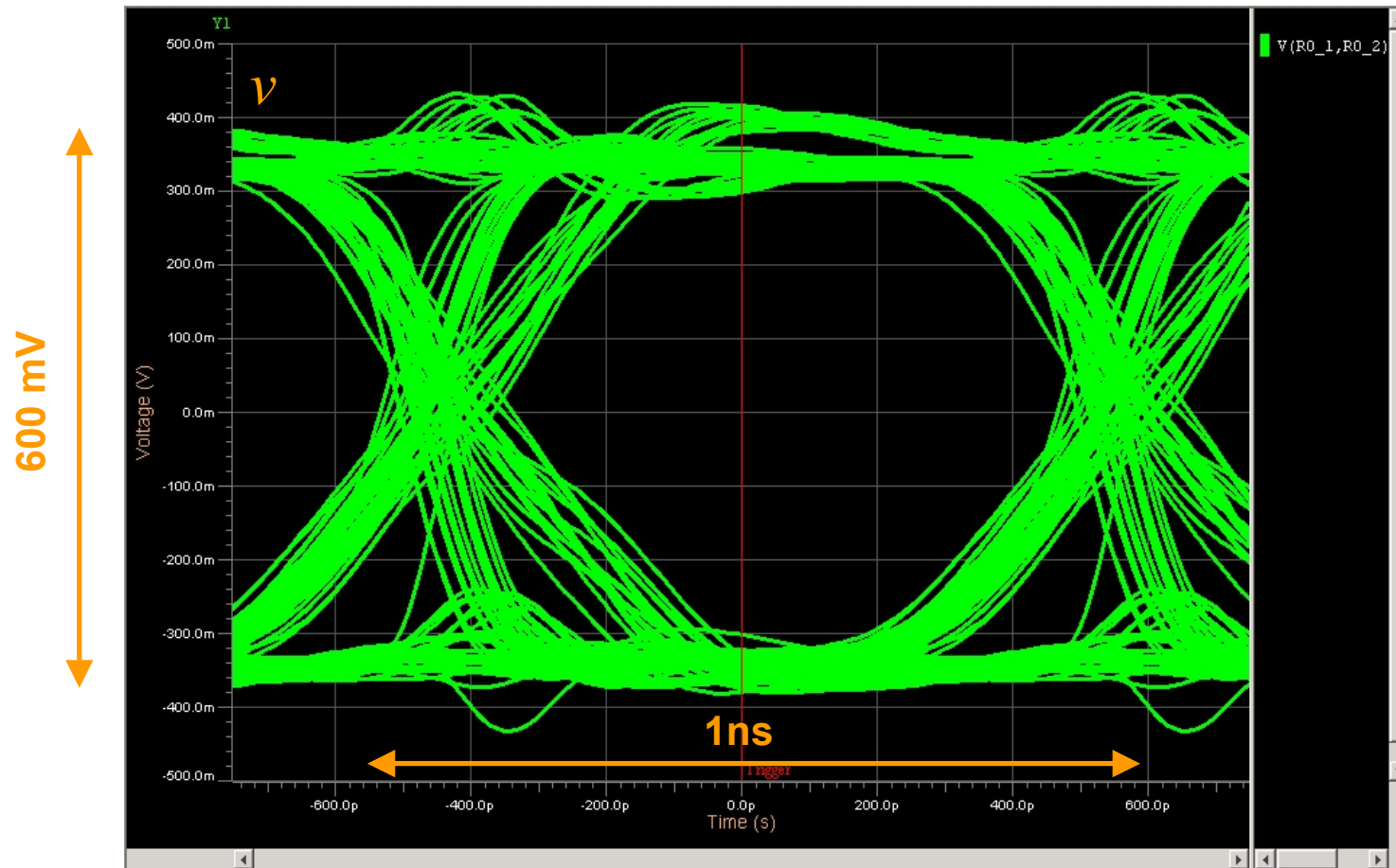
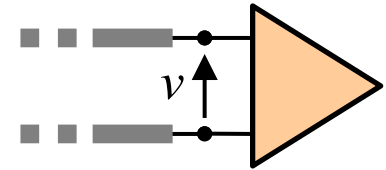
Macromodel **details** and **validation** in  
[I.S.Stievano, C.Siviero, I.A.Maio, F.G.Canavero, “Modeling  
of the Static and Dynamic Behavior of Differential Drivers,”  
Proc. of EMC-Compo 2004, Mar. 31 – Apr. 1, 2004]

### TEST CIRCUIT



## Example 2 (ii)

### ICX Application: Eye diagram





# Conclusions

**Parametric models are well suited to IBIS multilingual extension:** easy implementation and use in IBIS compliant simulators

- advantages {
- **Math Foundations and Generality**
  - **HIGH ACCURACY** at **LOW COMPLEXITY** (like classical IBIS models)
  - **Good EFFICIENCY**
  - **PROTECTION OF IP**

- advanced modeling techniques introduced via IBIS multilingual extension **not affect IBIS standard** and require **no upgrades of IBIS ver. 4.1 compliant simulators**





# Acknowledgements

Thanks to

- ❖  for providing the **ICX** simulation environment
- ❖ **Sergio Perazza** (Mentor, Italy) for the technical support on ICX and for the validation Example 2
- ❖ **Arpad Muranyi** (Intel) for VHDL templates and code posted on <http://www.eda.org/pub/ibis/summits/jun03a/> and <http://www.eda.org/pub/ibis/summits/feb04a/>