Introduction

- EDA Companies have established areas of excellence in their SI tools
  - E.g. AMS modeling, macro-modeling, (encrypted) SPICE modeling, design templates, flexible measurements, scripting.
  - Once these are established it is extremely unusual for a company to de-emphasis support for these features.

- All EDA Companies also maintain a “lowest common denominator” for SI device behavior and measurement
  - IBIS 3.2
  - Allows IC vendors and independent modeling companies to create a single model for use with all major SI tools.
  - Needs to accurately cover 99% of devices
What is the current state of the art?

- IBIS 3.2 still has lots of life in it for behavior, but there are examples where it is not adequate:
  - Drivers with pre-compensation
  - Equalizers
- IBIS 3.2 has bigger problems with measurement. It is not adequate for:
  - Receivers with slew rate sensitivity
  - Self clocked data streams
- IBIS 3.2 no longer meets the 99% criteria
  - Still should be the first choice where it is sufficiently accurate
- We need a new “lowest common denominator”

Synchronous Timing Analysis

- Static timing analysis: Clock edge to data out delay
- SI analysis: Driver, receiver, package, trace delays
- Static timing analysis: Input setup and hold time
- Spreadsheet: Constraints, results and violations
Analysis of Synchronous Nets

- Predominant technology when IBIS 2.1 was developed.
  - IBIS model describes behavior with IV and VT tables, Ccomp etc.
  - IBIS supports measurement with Vinh, Vinl, Vmeas etc.
- Typical Spreadsheet content (abbreviated):
  - Min/max/actual trace length, max/actual number of vias, max/actual stub length
  - Physical topology
  - Min/max/min actual/max actual driver to load delays
  - Max/actual overshoot voltage, max/actual ring-back voltage
  - Non-monotonic events

Source Synchronous Timing Analysis

Data book:
- Input setup and hold time

SI analysis (clock, data):
- Driver, receiver, package, trace delays

Spreadsheet:
- Constraints, results and violations
Analysis of Source Synchronous Nets

- Common technology when IBIS 3.2 was developed.
  - Additions to IBIS behavior include series passives, driver scheduling, bus hold ...
  - Additions to IBIS measurement include dynamic overshoot, strength dependant thresholds ...

- Additions to the Typical Spreadsheet
  - Max/actual trace length difference between data and clock net
  - Min/max/min actual/max actual driver to load delay difference match data and clock net
    (Derived from setup and hold requirement.)
  - Max/actual dynamic overshoot voltage and time

What Is New that Affects IBIS?

- Source synchronous devices with input slew rate sensitivity.
- Heavy inter-symbol interference
- New definitions for threshold voltages and overshoot
- Multi-gigabit, self clocked signaling
  - Pre-compensation
  - Equalizers
  - Phase locked loop data and clock recovery
  - Eye diagrams and masks
- Multi-level signaling
A look at one challenge: DDR2 (simplified)

- The clock and data receivers have very significant sensitivity to input slew rate.
- Dynamic overshoot is specified using a VT area.
- We want to be able to include DDR2 nets in an automated scan of the whole PCB
- We do not want to hard code DDR2 specific features into the waveform analysis or results spreadsheet.
  - This will be a never ending job and delivered later than the customer wants it!

Proposed General Approach

- Enhanced behavior and measurement information in IBIS
  - Create intelligent multi-lingual input models that delay their output signal based in slew rate
  - Enhance the IBIS measurement facilities to support the new dynamic overshoot constraint
    - Describe how to make the measurement
    - Inform the spreadsheet to add new columns for the data
Option 1: transistor level SPICE

- **Pros**
  - IC manufacturer can use the internal models that were developed from the Silicon.

- **Cons**
  - Encryption is required to hide the IP. Each EDA vendor has their own encryption package and proprietary foibles in their transistor primitives
  - Simulation will be slow compared to IBIS or AMS
  - Complicated models are prone to bugs.
  - Implementing flexible measurements in the model (e.g. the new dynamic overshoot) is too difficult. To solve the overall problem we would have to add a comprehensive measurement language to IBIS

Option 2: Macro-models

- **Pros**
  - Will work with any EDA vendor that has AMS, or is willing to add the (macro) building blocks into their SPICE like simulator.
  - Faster simulation than transistor level models

- **Cons**
  - The current building blocks only have been proven in their support of IBIS 3.2. It is likely that new building blocks will soon be needed.
  - Implementing flexible measurements in the model (e.g. the new dynamic overshoot) is too difficult. To solve the overall problem we would have to add a comprehensive measurement language to IBIS
Option 3: Analog Only AMS*

Pros
- Most EDA vendors have access to analog only AMS
- Stepping stone to full AMS.
- Relatively easy for the model to do its own measurements
  - Can be output as text messages ready for the spreadsheet
  - Augment in IBIS with a simple list of column headings to add to the spreadsheet.
- Fast simulation

Cons
- The languages are complex and no vendor (to my knowledge) has every feature supported
  - Could be alleviated by agreeing to a preferred language subset
- Implementing digital features e.g. extended history in an equalizer requires jumping through hoops.

* Analog “AMS” generally differs from “A” in its support for discontinuous functions

Option 4: AMS

Pros
- Most flexible and technically elegant solution
- Easy for the model to do its own measurements
  - Can be output as text messages ready for the spreadsheet
  - Augment in IBIS with a simple list of column headings to add to the spreadsheet.
- Fast simulation

Cons
- Few EDA vendors have currently offered AMS in their SI tools.
- The languages are complex and no vendor (to my knowledge) has every feature supported
  - Could be alleviated by agreeing to a preferred language subset
Conclusion

- We will not de-emphasize what we believe to the best long term solution i.e. multi-lingual IBIS with AMS.
- We believe that in addition to the ultimate solution a short term a “lowest common denominator” modeling language is needed
- IBIS 3.2, by itself, is no longer able to reliably meet this requirement
- The solution should address both behavior and measurement
- There are a number of competing methodologies that will meet many of the requirements
- By definition we will only have a “lowest common denominator” if all the major EDA vendors agree on a single solution and add it to their SI tools.