SSO Simulation with IBIS

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Motivation

SSN with IBIS in 2000
  - Simulation setup
  - BEHAVIOR – model with Voltage-Controlled Current Sources
  - very good concordance with transistor based models

Table driven kssn-multiplier
  - Multiplier extraction
  - Results HSPICE vs. VCCS-BEHAVIOR
  - Lacking concordance

Enhanced VCCS-BEHAVIOR
  - Additional RC – Timing coefficient
  - Improved results

Summary
Acknowledgements

Overview

- SSN 2000
- kssn - table
- Enhanced VCCS model
- Summary

- INFINEON TECHNOLOGIES
  - HYB18T512160AF
  - DDR2 - Memory

- TEXAS INSTRUMENTS
  - CDCE706
  - PROGRAMMABLE 3-PLL CLOCK SYNTHESIZER / MULTIPLIER / DIVIDER

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SSO Simulation Setup
( m+1 switching outputs )

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

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VCCS-Model enhancement

- A second multiplier for rising \((kssnr)\) and falling \((kssnf)\) edges
- Both multipliers are controlled by the \((Vdd-Vss)\) voltage drop
- Feedback on the gate source voltage of the output transistors
- Multiplier generation:
  - Pullup/down V/I-tables as a function of Vdd
  - SSO-V/t-table (Golden Waveform)
VCX16244 SSN analysis results (rising edge)
Enhanced two waveform behavioral model Number of SSO = 6

Overview
SSN 2000
kssn - table
Enhanced VCCS model
Summary

Node OUT: Transistor based Behavioral
Node END: Transistor based Behavioral

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kssnr/f Multiplier Generation Method

CMOS Driver Output High Characteristic

I(3.6V) = I(3.6V)/I(3.3V)

50 Ohm loading characteristic

I(3.3V)
I(3.6V)
kssn rising coefficient extraction
HYB18T512160AF (DDR2) INFINEON

Overview
SSN 2000
kssn - table
Enhanced VCCS model
Summary

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kssn falling coefficient extraction
HYB18T512160AF (DDR2) INFINEON

Overview
SSN 2000
Enhanced VCCS model
Summary

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HYB18T512160AF / INFINEON
kssn rising/falling @ Vdd = 0.5V to 3.6V (1.8V nom.)
Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

TI CDCE706 TEXAS INSTRUMENTS
kssn rising/falling @ Vdd = 0.5V to 5V (3.3V nom.)

Vdd_nom

slew rate max

slew rate min

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DDR2 buffer Infineon
Supply voltage drop (L=2x1nH) / Load Tline Zo=50 Ohm

Overview
SSN 2000
kssn - table
Enhanced VCCS model
Summary

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TI CDCE706 / Voltage drop / Rising edge
VCCS-model with kssn table (L=2x3nH)

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

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Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

TI CDCE706 Rising edge vs. Vdd drop
Transistor based model

Vdd=3.3V

Vdd drop
L=1nH … 9nH

Sig.@Vdd=3.3V

Sig.@Vdd drop
Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

TI CDCE706 Falling edge vs. Vdd drop
Transistor based model

Vdd drop
L = 1nH ... 9nH

Vdd = 3.3V

Sig. @ Vdd drop
Sig. @ Vdd = 3.3V

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## Differences VCCS 2000 vs. 2006

<table>
<thead>
<tr>
<th></th>
<th>VCCS 2000</th>
<th>VCCS 2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transition Time</td>
<td>ca. 5ns</td>
<td>&lt;500ps</td>
</tr>
<tr>
<td>Operation Point</td>
<td>saturation region</td>
<td>linear region</td>
</tr>
<tr>
<td>Vdd/GND drop</td>
<td></td>
<td></td>
</tr>
<tr>
<td>amplitude</td>
<td>ca. 15%Vdd</td>
<td>ca. 40% Vdd</td>
</tr>
<tr>
<td>width</td>
<td>ca. 7ns</td>
<td>ca. 1ns</td>
</tr>
<tr>
<td>Design of the OUTPUT stage</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time domains</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Slew rate control</td>
<td>NO/YES</td>
<td>YES</td>
</tr>
<tr>
<td>Vdd-drop Feed back</td>
<td>NO</td>
<td>YES</td>
</tr>
<tr>
<td>Prestage @Vdd_int</td>
<td>NO/YES</td>
<td>YES</td>
</tr>
<tr>
<td>On-die capacitance</td>
<td>NO</td>
<td>YES</td>
</tr>
</tbody>
</table>
Vdd drop improvement with C_pre=30pF
CDCE706 with PKG L=2x3nH 10 SSO

Overview
SSN 2000
kssn - table
Enhanced VCCS model
Summary

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Vdd drop improvement with $C_{pre}=30\text{pF}$

CDCE706 with PKG $L=2\times3\text{nH}$  10 SSO
Enhanced VCCS-Behavior Model with \textit{kssn} (static) and \textit{td\_RC} (dynamic) coefficients

**Overview**

- SSN 2000
- \textit{kssn - table}
- Enhanced VCCS model

**Summary**

Enhanced VCCS-Behavior Model with \textit{kssn} (static) and \textit{td\_RC} (dynamic) coefficients

\begin{align*}
\text{td\_RC} \text{ determination} \\
- \text{by optimisation through the } Vdd\_drop \text{ @ known } L \\
- \text{by adjustment from } I=I(t) \text{ table @ } L
\end{align*}

\begin{equation*}
td\_RCr(Vdd-Vss) * kssnr(Vdd-Vss) * kpu(t) * Ipu(Vout)
\end{equation*}

\begin{equation*}
td\_RCf(Vdd-Vss) * kssnf(Vdd-Vss) * kpd(t) * Ipd(Vout)
\end{equation*}

\begin{equation*}
Ipc(Vout) \quad C\_comp/2 \\
Igc(Vout) \quad C\_comp/2
\end{equation*}

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Vdd drop improvement
DDR2 with PKG L=2x3nH  5 SSO

Overview
SSN 2000
kssn - table
Enhanced VCCS model
Summary

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Vdd drop improvement
CDCE706 with PKG L=2x3nH 10 SSO

Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary

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Summary

- With improved IBIS models, SSO can be simulated in a better concordance with transistor based models, IF
  - kssn – table information (BIRD 97.x)
  - current vs. time tables @ known RLC environment (BIRD 95/98)

- Advantages
  - Signal integrity analysis
    - PDS – Voltage drop
    - Timing simulation

- More investigations have to be done, to evaluate for different technologies, the validity range and the accuracy of the proposed improvement
SSO Simulation with IBIS

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Thank you for your attention