Current Status - IBIS 4.1 Macro Library for Simulator Independent Modeling

presented by
Todd Westerhoff, Cisco Systems

<table>
<thead>
<tr>
<th>IBIS-Macro Working Group</th>
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<tbody>
<tr>
<td>Intel - Arpad Muranyi</td>
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<tr>
<td>Cisco - Mike LaBonte, Todd Westerhoff</td>
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<tr>
<td>NC State University - Paul Fernando</td>
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<td>SiSoft - Barry Katz, Walter Katz</td>
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<td>Cadence - Ken Willis</td>
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<td>Mentor Graphics - Ian Dodd</td>
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<td>Sigrity - Sam Chitwood</td>
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<td>Teraspeed - Scott McMorrow, Bob Ross</td>
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Agenda

- Origins of IBIS-Macro
- IBIS-Macro concept
- Status at last meeting
- Recent activities
- Current issues
- Next steps
Origins

- IBIS hasn’t kept up with new I/O technologies
  - SPICE use for SI is steadily increasing
- IBIS 4.1 supports AMS, but adoption has been slow
  - AMS is powerful, but also complex
- Macro modeling proposed as alternative to full AMS implementations
  - Proposed by Donald Telian of Cadence, Jan 2005
  - Original proposal used Berkeley SPICE extensions
- Study group formed in Mar 2005 to explore macro modeling concept in IBIS
Vendor / Tool / Language Survey

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<thead>
<tr>
<th>Tool #</th>
<th>Verilog-A</th>
<th>Verilog-AMS</th>
<th>VHDL-AMS</th>
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- Current status of 12 popular “SI” tools and their –AMS language support
- Goal: develop a strategy that supports advanced modeling across all these combinations
IBIS-Macro Goals

- Drive IBIS to support advanced technologies
- Multi-simulator support
  - Same as original IBIS, tool-independent models
- Speed EDA/semiconductor adoption of advanced behavioral modeling techniques
- Leverage existing skills
  - Most model developers are familiar with Spice-style macro modeling
Macro Models

- Instantiate blocks with pre-defined functions and behaviors
- Parameterize those blocks by passing values into the elements
- Interconnect blocks using a netlist-type syntax
- Define external ports to the model using the netlist syntax
IBIS-Macro Concept

- Library of AMS “elements” instantiated and interconnected to create complex buffer models
- AMS elements modeled after sources and elements found in popular SPICE tools
- Ensure elements can be implemented by substitution in SPICE-only engines
- Standardize AMS element library across semiconductor model providers
- Collection of reference “templates” instantiate AMS elements to address common modeling issues (e.g. pre-emphasis buffer)
IBIS-Macro Element Mapping

Verilog-AMS Simulator

```
`include "./Macro_lib\No_ODT_OUTPUT_data.dat"
IBIS_OUTPUT #("OUTPUT_data,
  .Max_dt(Max_dt_val),
  .Vth_R(Vth_R_val),
  .Vth_F(Vth_F_val)\"
B1 (Power, Ground, Pad, In_D, Power, Ground);
```

SPICE Simulator

```
b_io PUnref PDefB IOb InB En PCrefB GCrefB
+ file='mybuf.ibs' model='mybuf' +power=on buffer=2
```

VHDL-AMS Simulator

```
IBIS_OUTPUT1 : entity MacroLib.IBIS_OUTPUT(IBIS_2EQ2UK)
generic map ( DataFile => ".\Macro_lib\No_ODT_IO_data.txt" )
port map ( PU_ref => Power,
  PD_ref => Ground,
  Pad => Output,
  In_D => Input,
  PC_ref => Power,
  GC_ref => Ground );
```
Status at Last Meeting

- Preliminary library in place
- Recruiting semiconductor vendors to test library
- Looking for additional model templates
  - Initial set contributed by Cadence
- Looking for resources to help with automated model translation / reformatting
Recent Activities

- Ongoing weekly meetings
- Final coding / testing of element library
- Driving EDA tool compatibility
- BIRD100.2 accepted
- Recruited Paul Fernando (NCSU) to help with model translation issues
- Released library versions 1.0 (Verilog-A and VHDL-AMS)
  - www.eda.org/pub/ibis/macromodel_wip/
Tool Development

Documentation Tool

Model Data Extraction Tool
Current Issues

- Significant compatibility issues identified with AMS implementations in different EDA tools
  - Understandable, considering relative age of –AMS language and EDA implementations
- Discussions on best way to proceed
  - Discard macro modeling, rely on native AMS
  - Document needed AMS language subsets in Verilog and VHDL
  - Proceed as planned, using macro library as *de facto* subset documentation and test case
  - Proceed as planned, have macro library explicitly defined as compliance test suite
Next Steps

- Continue analog-only vs. full-AMS discussion
- Drive EDA tool improvements for language support
- Seek additional semiconductor and EDA vendor participation
- Create additional templates, determine if additional building blocks are needed
For More Information

- IBIS-Macro Website
  - www.eda.org/pub/ibis/macromodel_wip/
For More Information

- IBIS-Macro mail reflector
  - Mail to: ibis-macro-request@freelists.org
  - Subject: subscribe
- IBIS-Macro mail archives
  - www.freelists.org/archives/ibis-macro