



## Study of IBIS Waveform Time Offsets

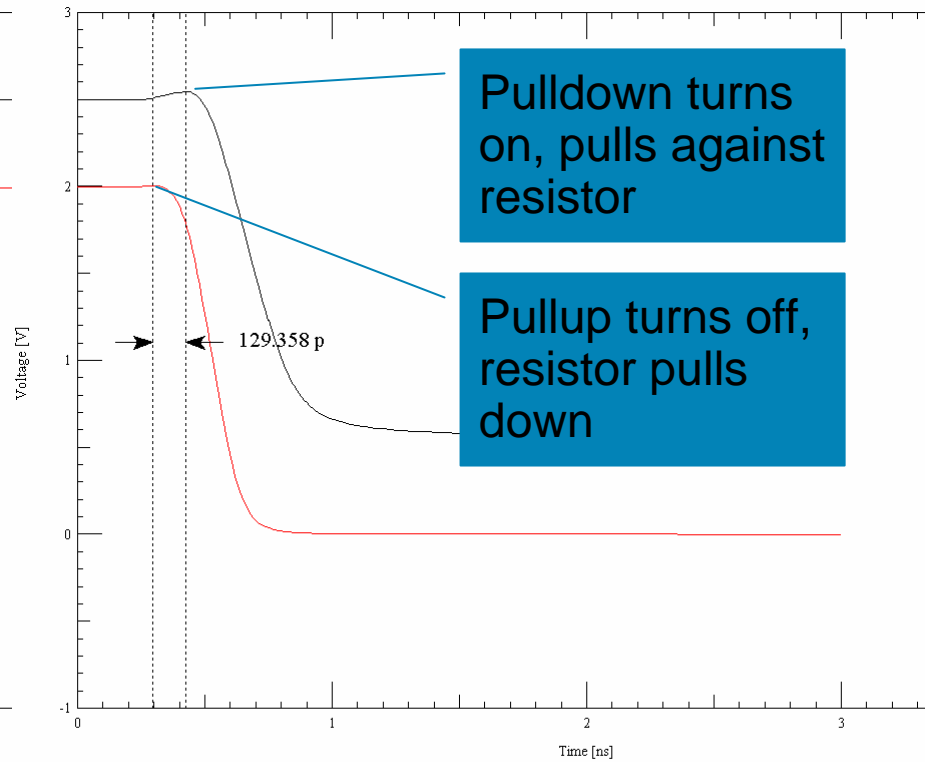
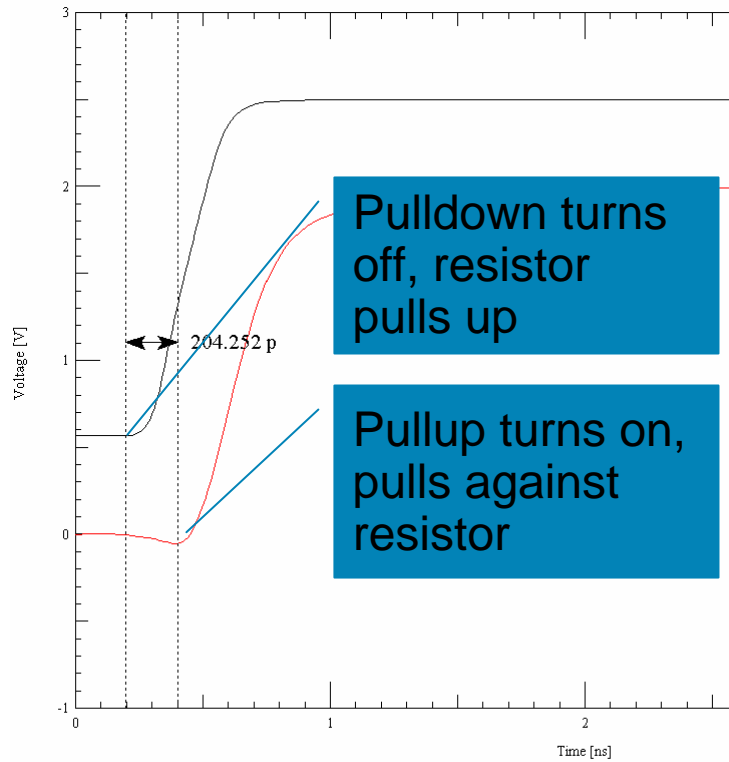


**How IBIS simulators handle offset and aligned IBIS waveform data**  
**Mike LaBonte, Cisco Systems**  
**IBIS Summit Meeting, 1 February 2007**

# Background

- To change states a buffer must turn off one transistor and turn on the other.
- The turn-off usually precedes the turn-on, to avoid excessive “through current” while both are partially on.
- Simulators must mimic this time offset controlling the pullup and pulldown I/V elements.
- IBIS models do not directly convey this timing.
- Simulators examine IBIS waveforms for 2 fixtures (pulled up and pulled down) to “guess” the turn-on/turn-off timing.
- When waveforms have no offset, simulators must revert to some fallback mode, which is proprietary and likely to vary.

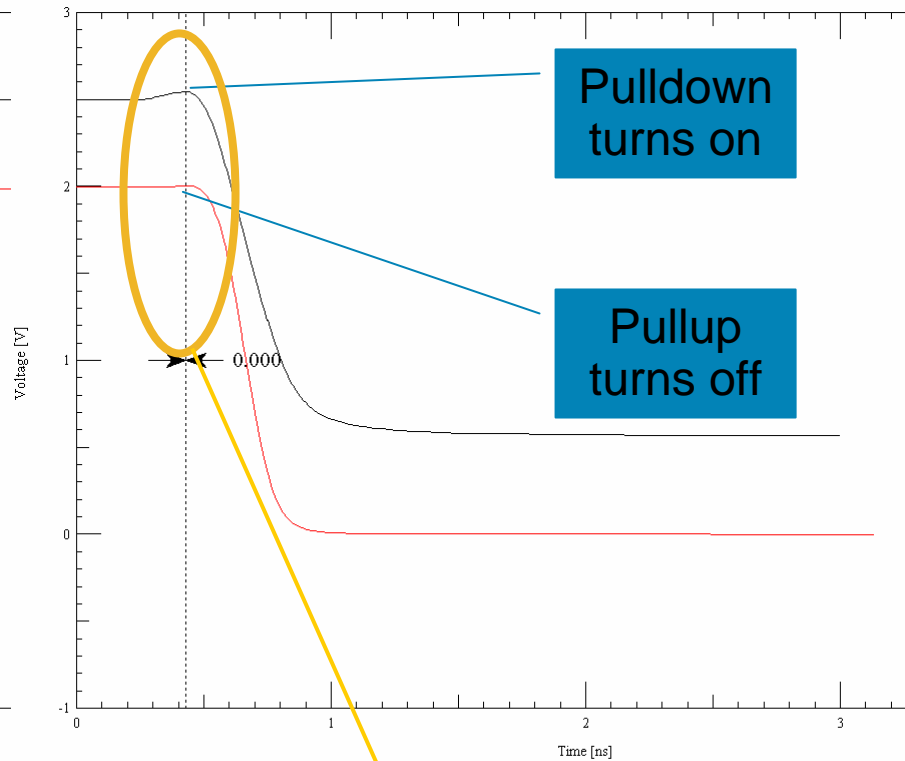
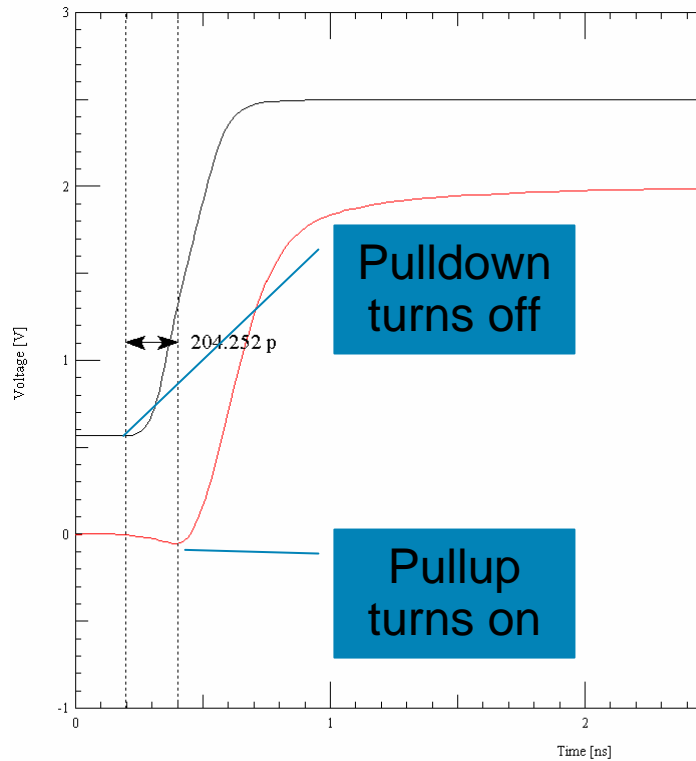
# Offset IBIS Waveforms (normal)



— R\_fixture=50, V\_fixture=2.5    — R\_fix

— R\_fixture=50, V\_fixture=2.5    — R\_fixture=50, V\_fixture=0

# Aligned IBIS Waveform (abnormal)

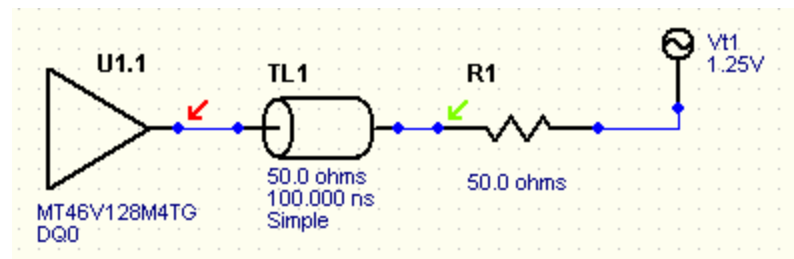


Note: waveform manually shifted

Changes voltage at same time, regardless of fixture voltage!

# Simulation Test Circuit

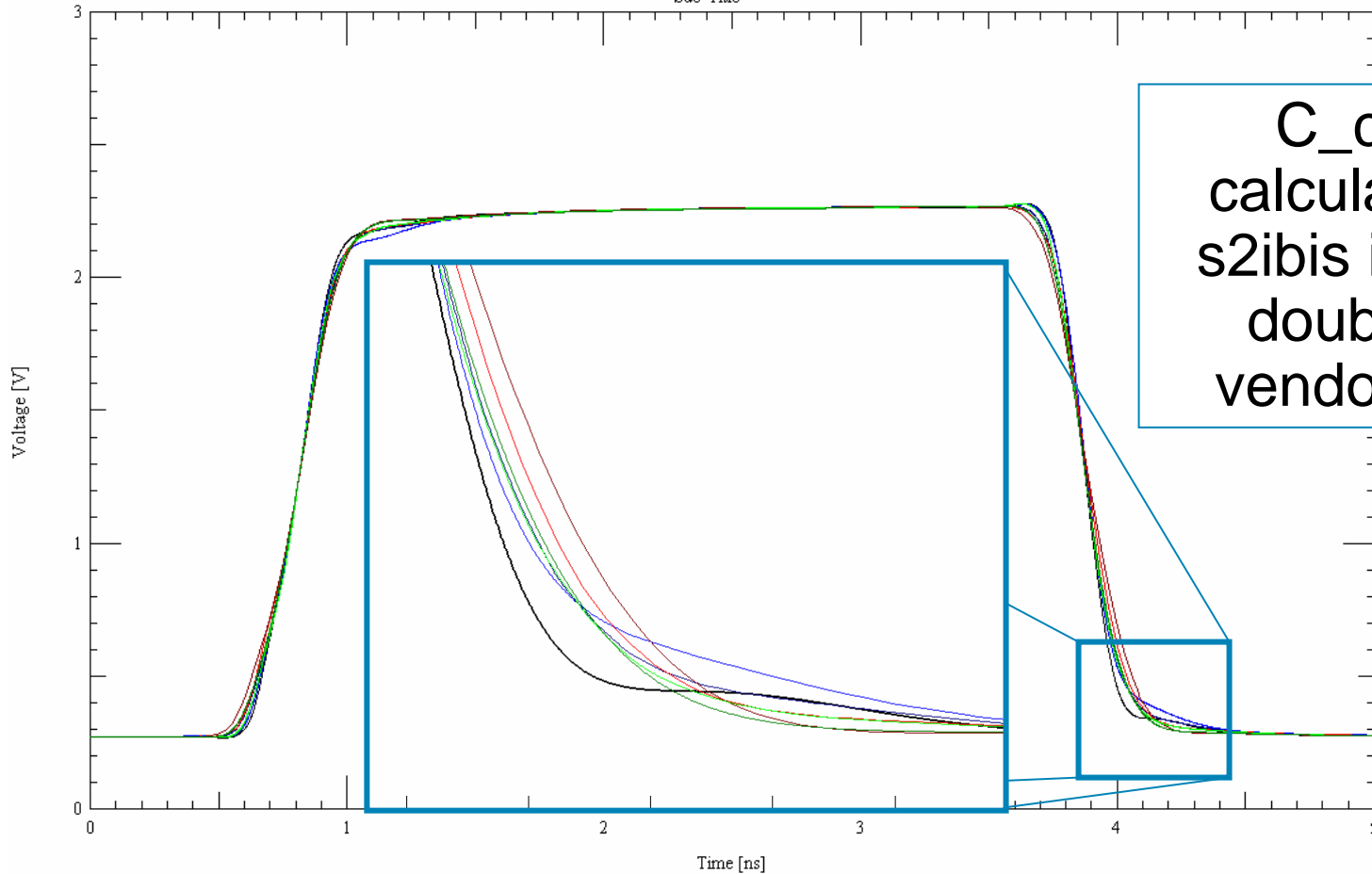
- 2.5V 167MHz buffer
  - Vendor IBIS model, 0 ERRORS, 0 WARNINGS
  - Vendor silicon SPICE model
- Package  $R=70.4m$   $L=5.3e-9$   $C=1.08e-12$
- 50 ohm T-line terminated to mid-voltage VTT
- Tested with 3 IBIS simulators + Silicon SPICE
- Voltage measured at buffer pad
- Power/ground currents measured in 2 simulators
- Test cases:
  1. Buffer with normal waveforms
  2. Falling waveforms aligned
  3. No waveforms at all



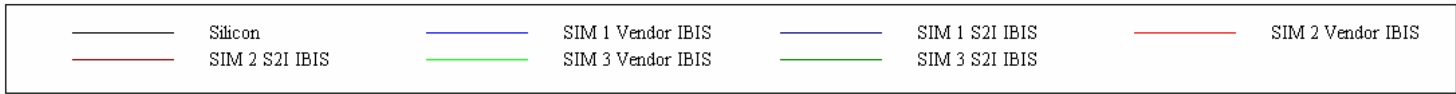
# Baseline: Vendor IBIS, S2IBIS, and Silicon

Silicon vs. Vendor IBIS & S2IBIS - 3 IBIS Simulators

Sub-Title

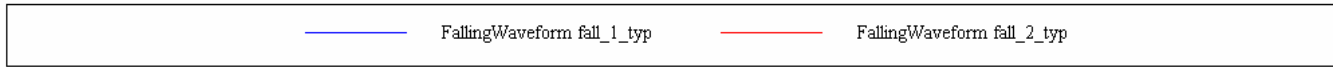
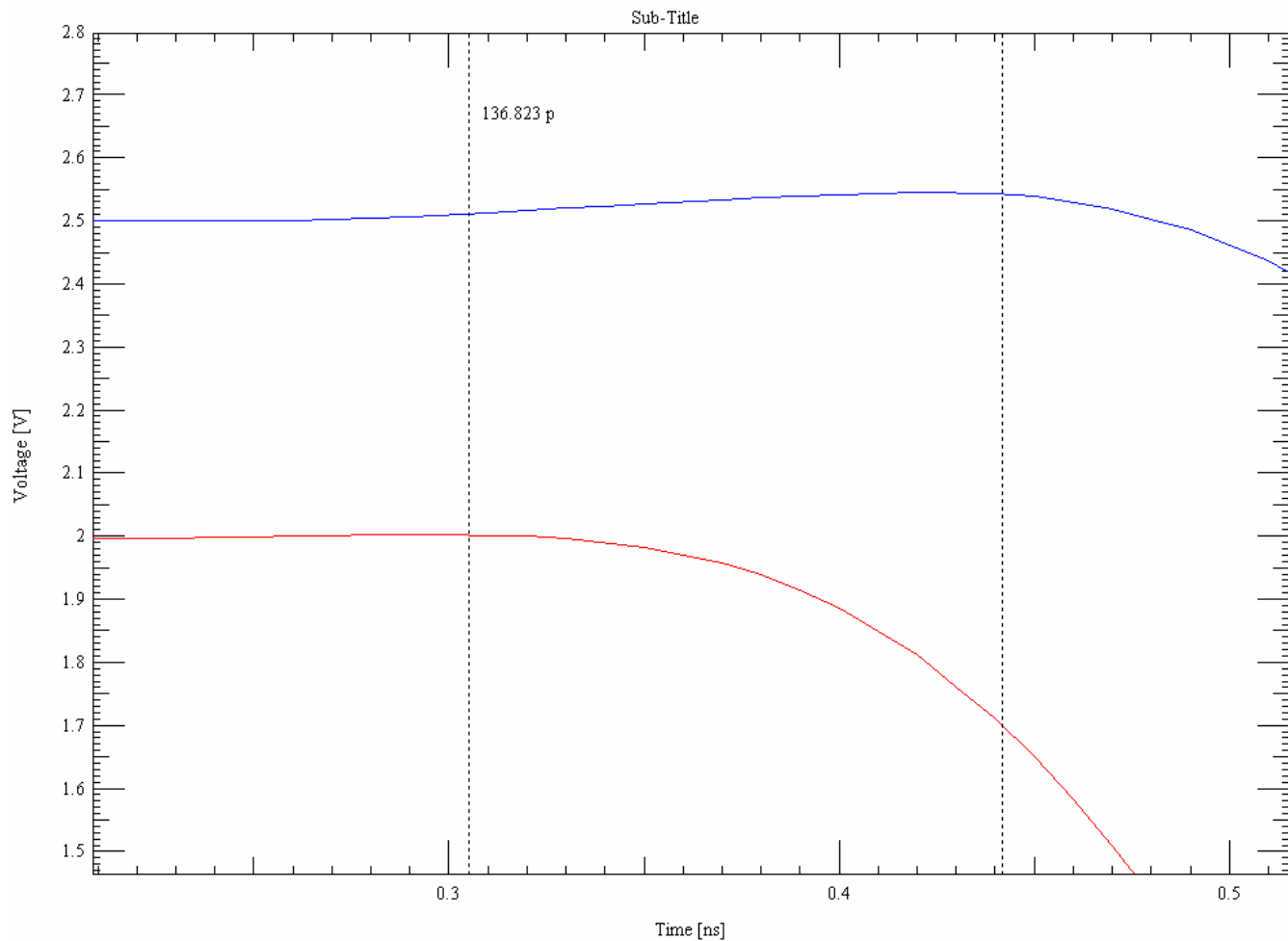


C\_comp  
calculated for  
s2ibis is about  
double the  
vendor value



# Vendor IBIS Fall Waves Offset (Normal)

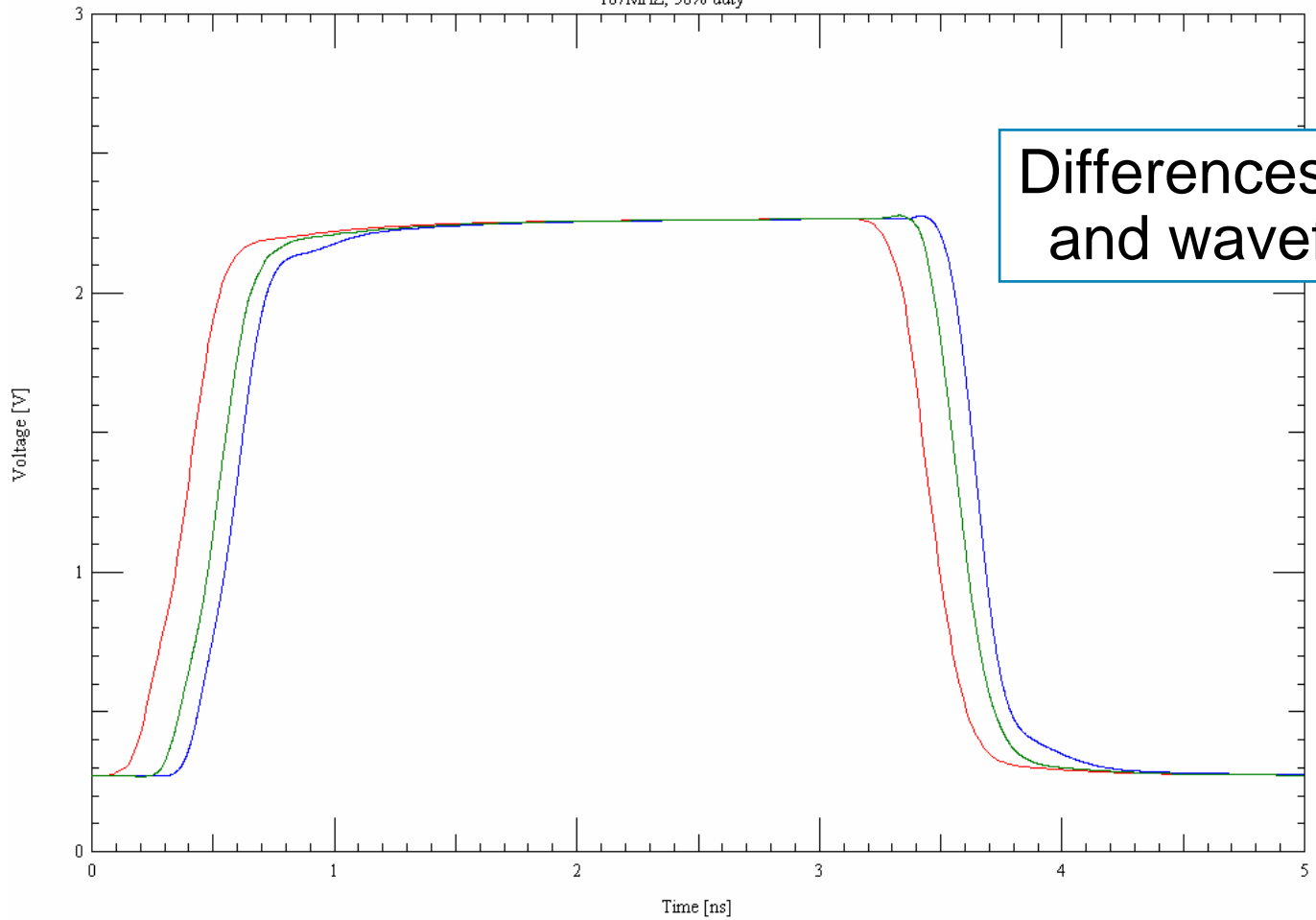
Falling Waveform Time Offset - normal



# Vendor IBIS Waveform Case - 3 Simulators

IBIS Simulator Comparison - normal waveforms

167MHz, 50% duty



Differences in trigger time and waveform trimming

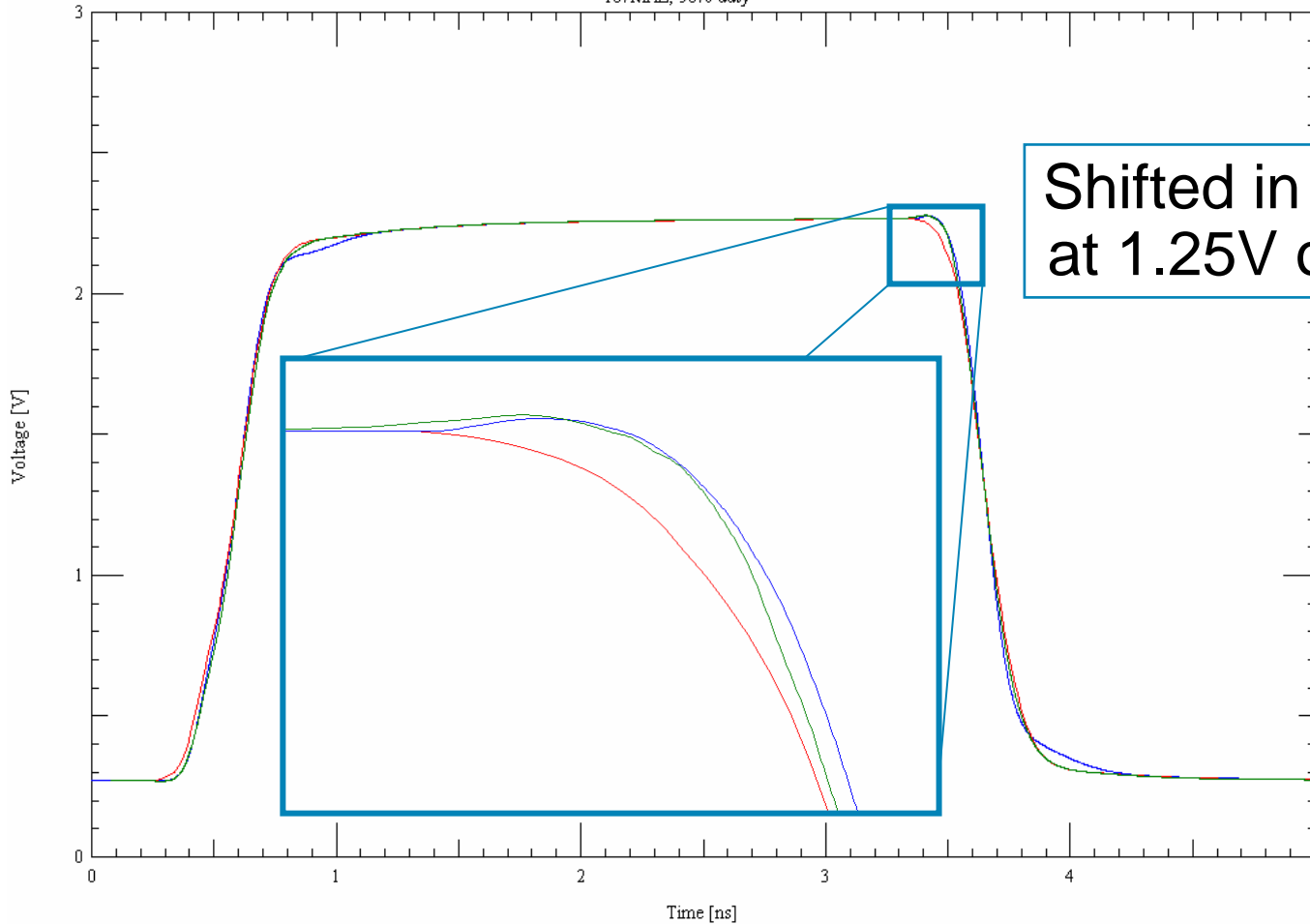
IBIS\_SIM\_1 IBIS\_SIM\_2 IBIS\_SIM\_3



# Vendor IBIS Waveform Case – Lined Up

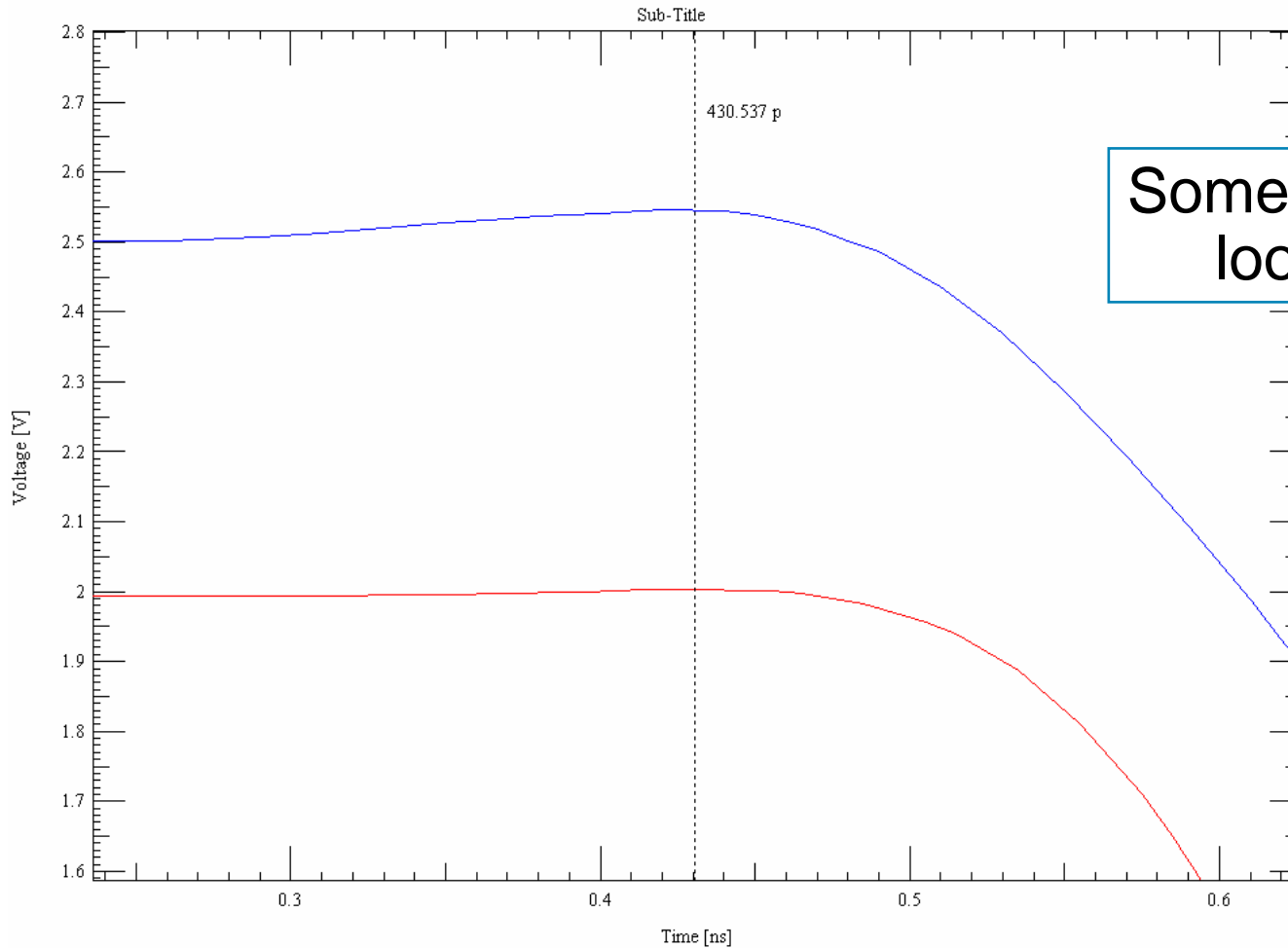
IBIS Simulator Comparison - normal waveforms, lined up

167MHz, 50% duty

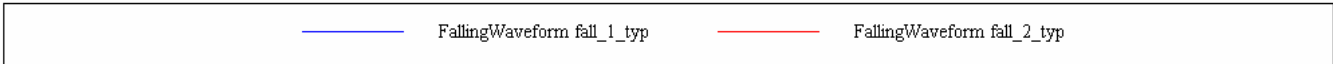


# IBIS Fall Waves Manually Aligned

Falling Waveform Time Offset - incorrect

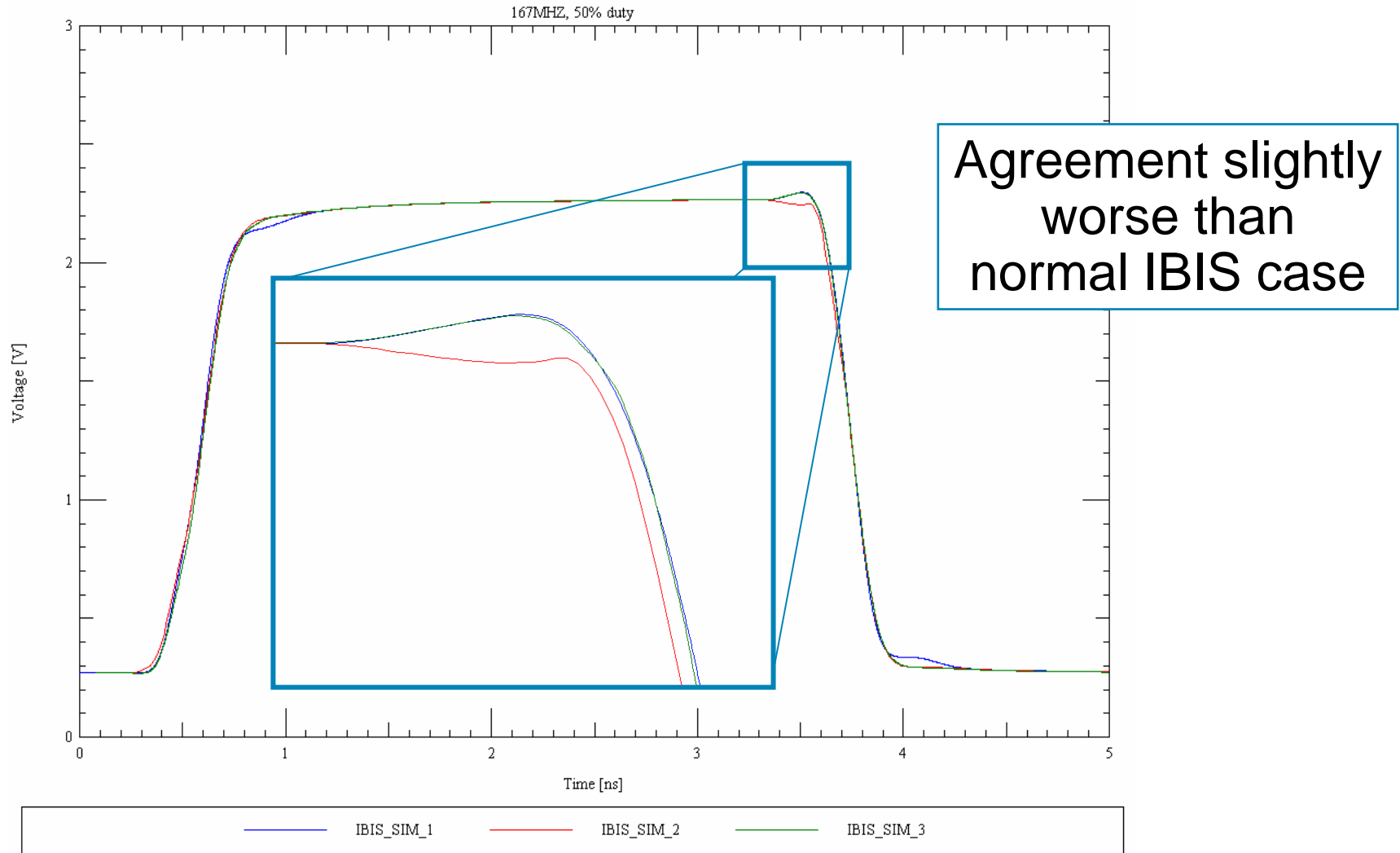


Some IBIS models look like this



# Aligned IBIS Waveform Case – Lined Up

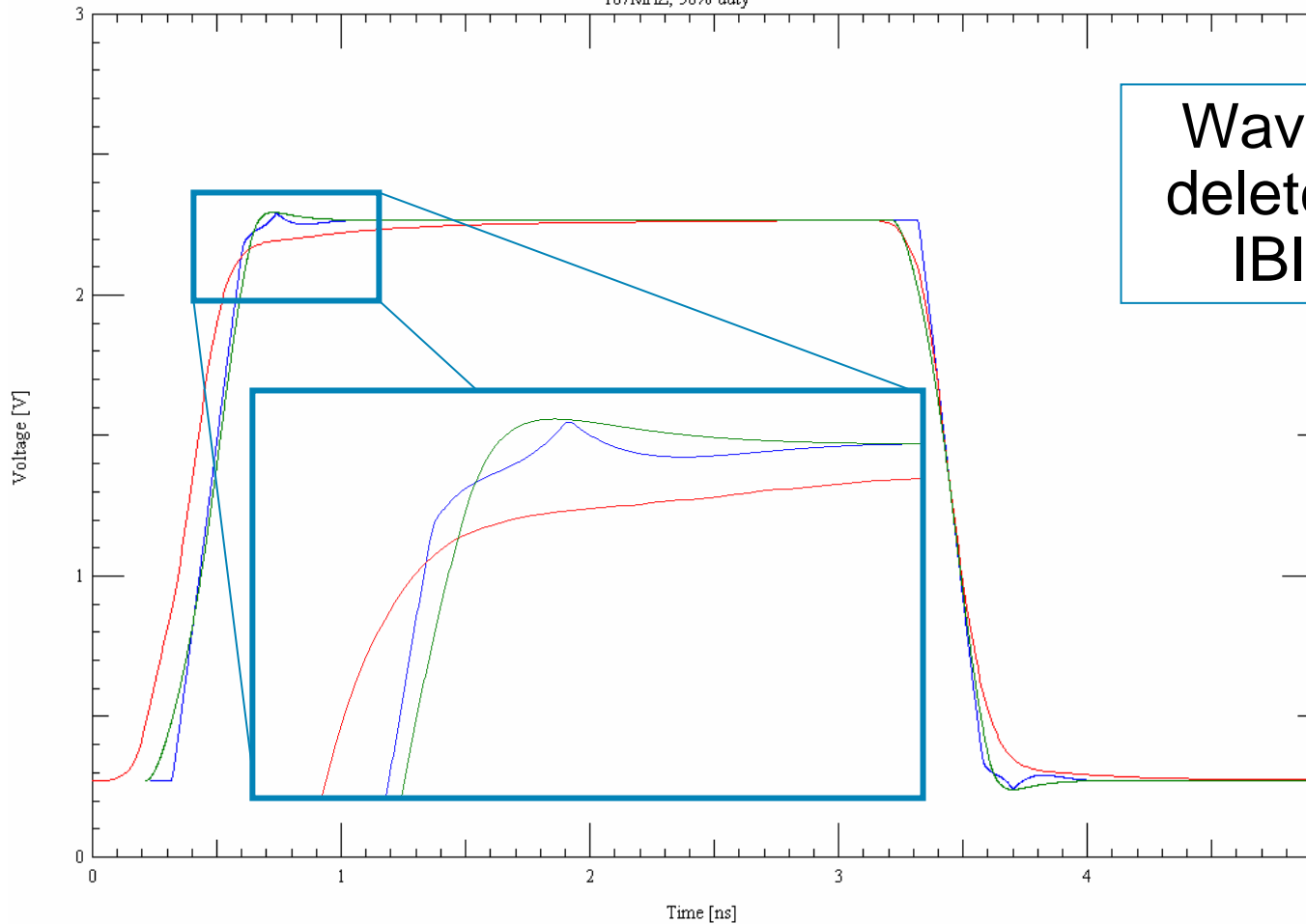
IBIS Simulator Comparison - aligned falling waveforms, lined up



# No IBIS Waveform Case – Lined Up

IBIS Simulator Comparison - no waveforms, lined up

167MHz, 50% duty

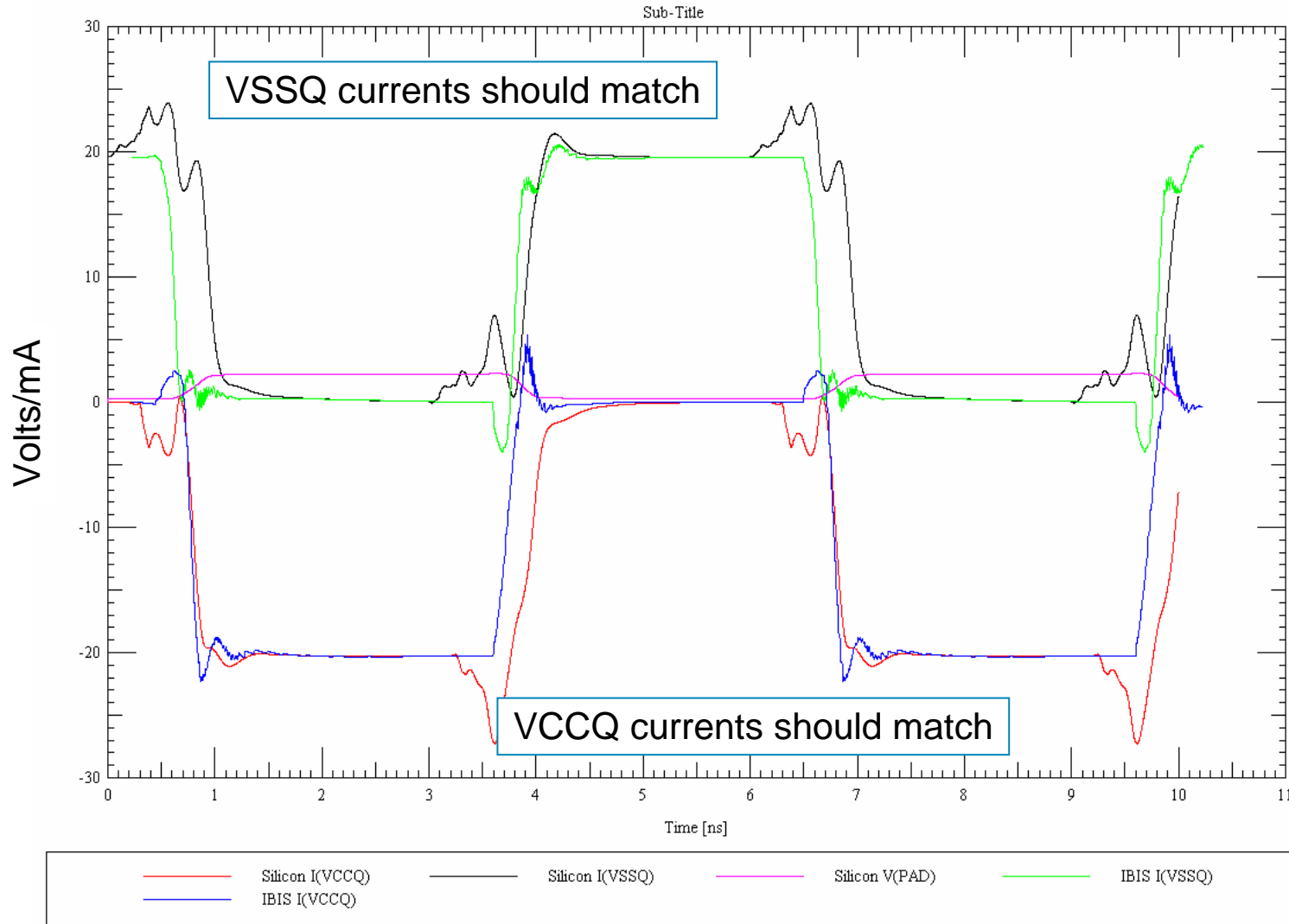


Waveforms  
deleted from  
IBIS file

IBIS\_SIM\_1 IBIS\_SIM\_2 IBIS\_SIM\_3

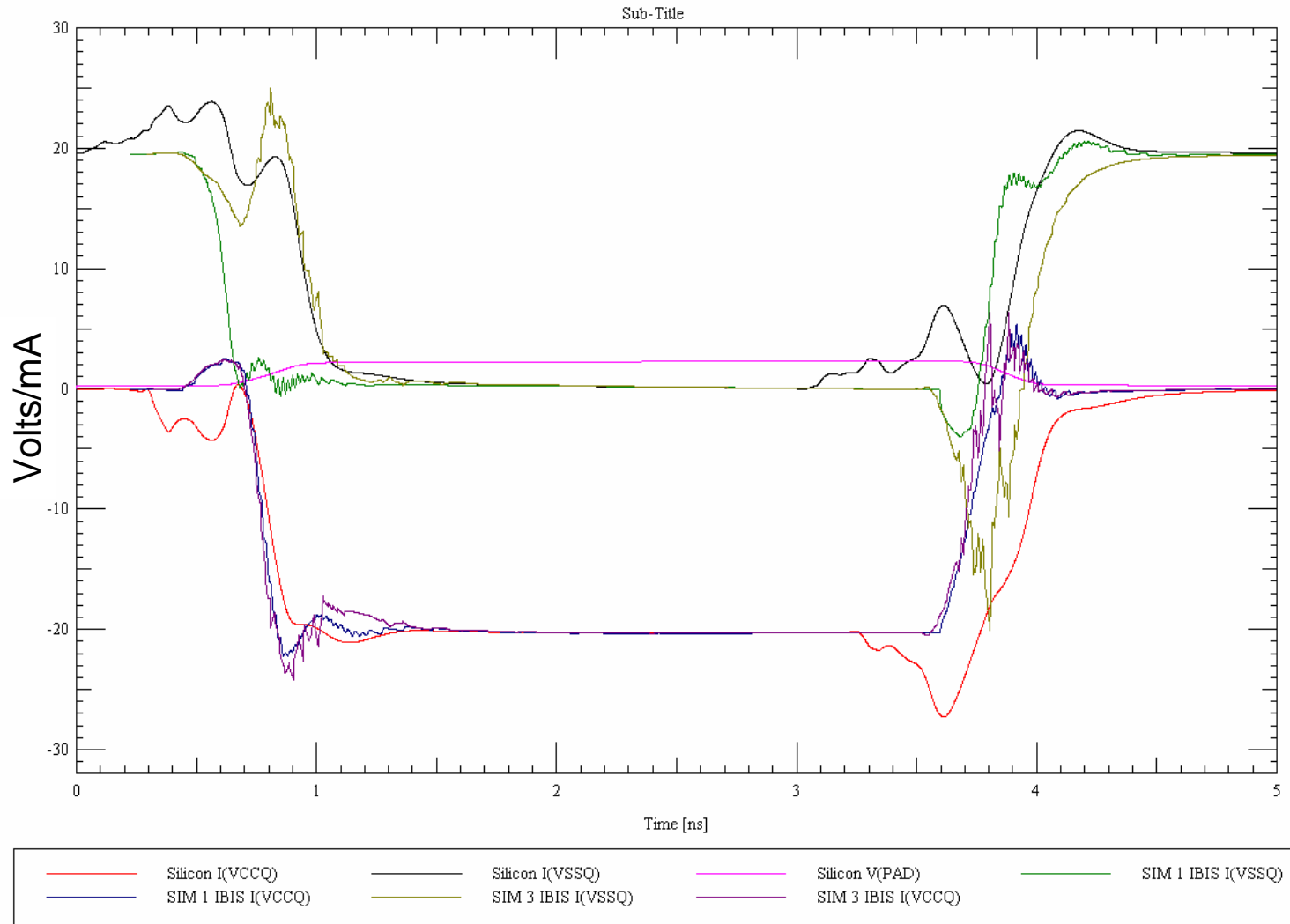
# Normal IBIS Waveform Case - Currents

VCCQ and VSSQ Currents - Silicon vs. IBIS Simulator 1 - Normal IBIS



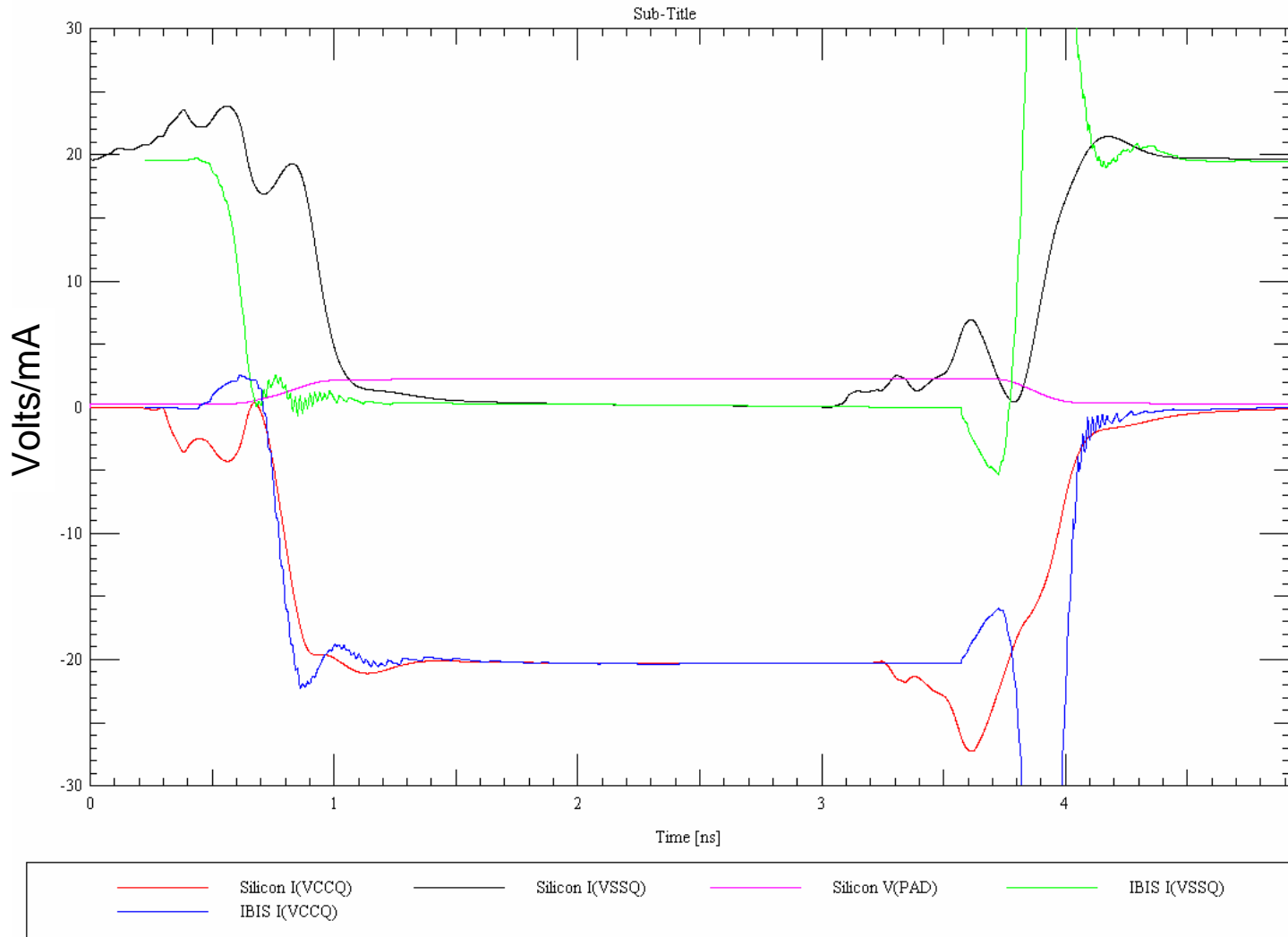
# Normal IBIS Waveforms - 2 IBIS Simulators

VCCQ and VSSQ Currents - Silicon vs. IBIS Simulators 1 + 3 - Vendor IBIS



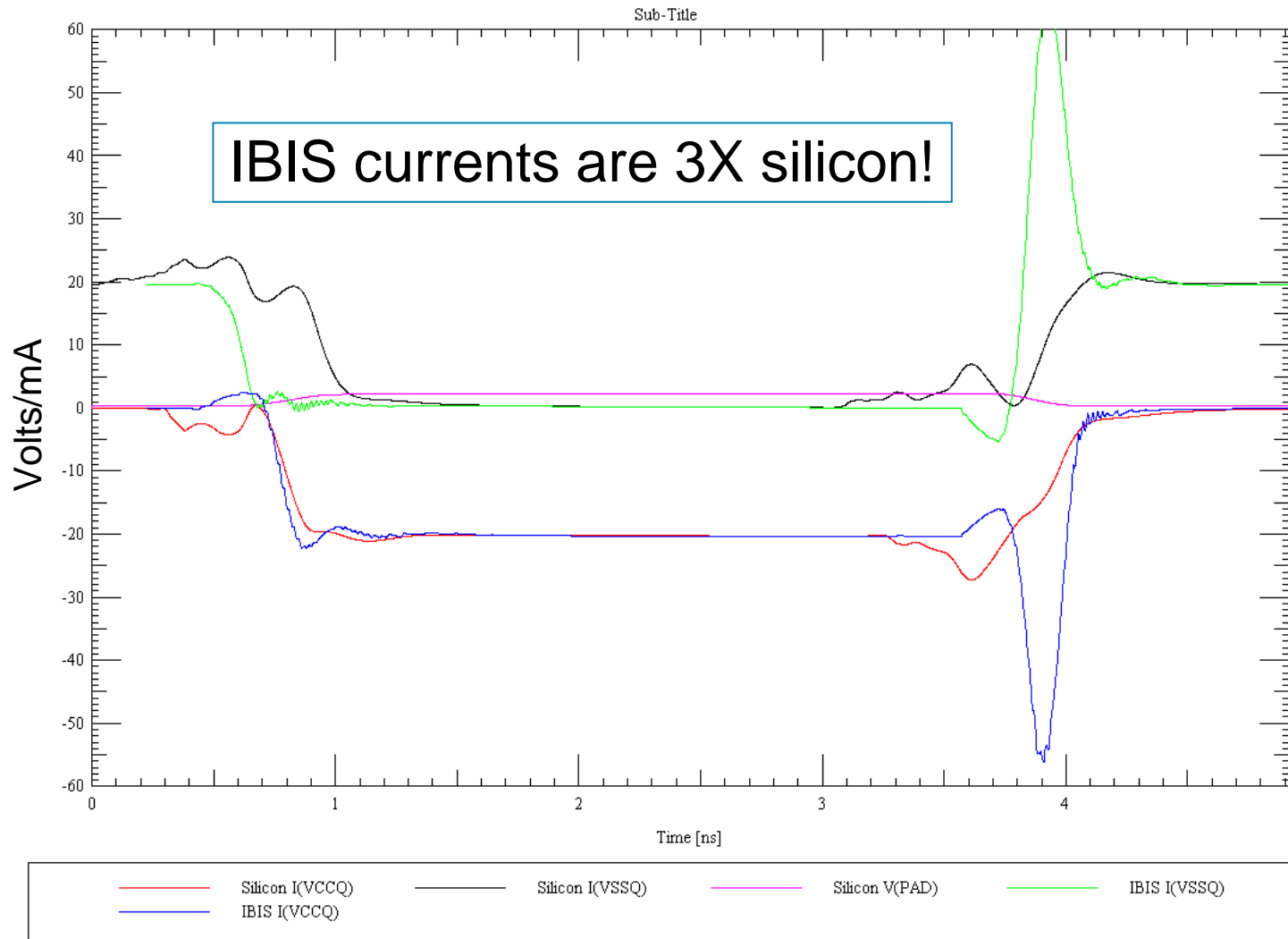
# Aligned IBIS Waveform Case - Currents

VCCQ and VSSQ Currents - Silicon vs. IBIS Simulator 1 - Fall Aligned IBIS



# Aligned IBIS Waveform Case - Currents

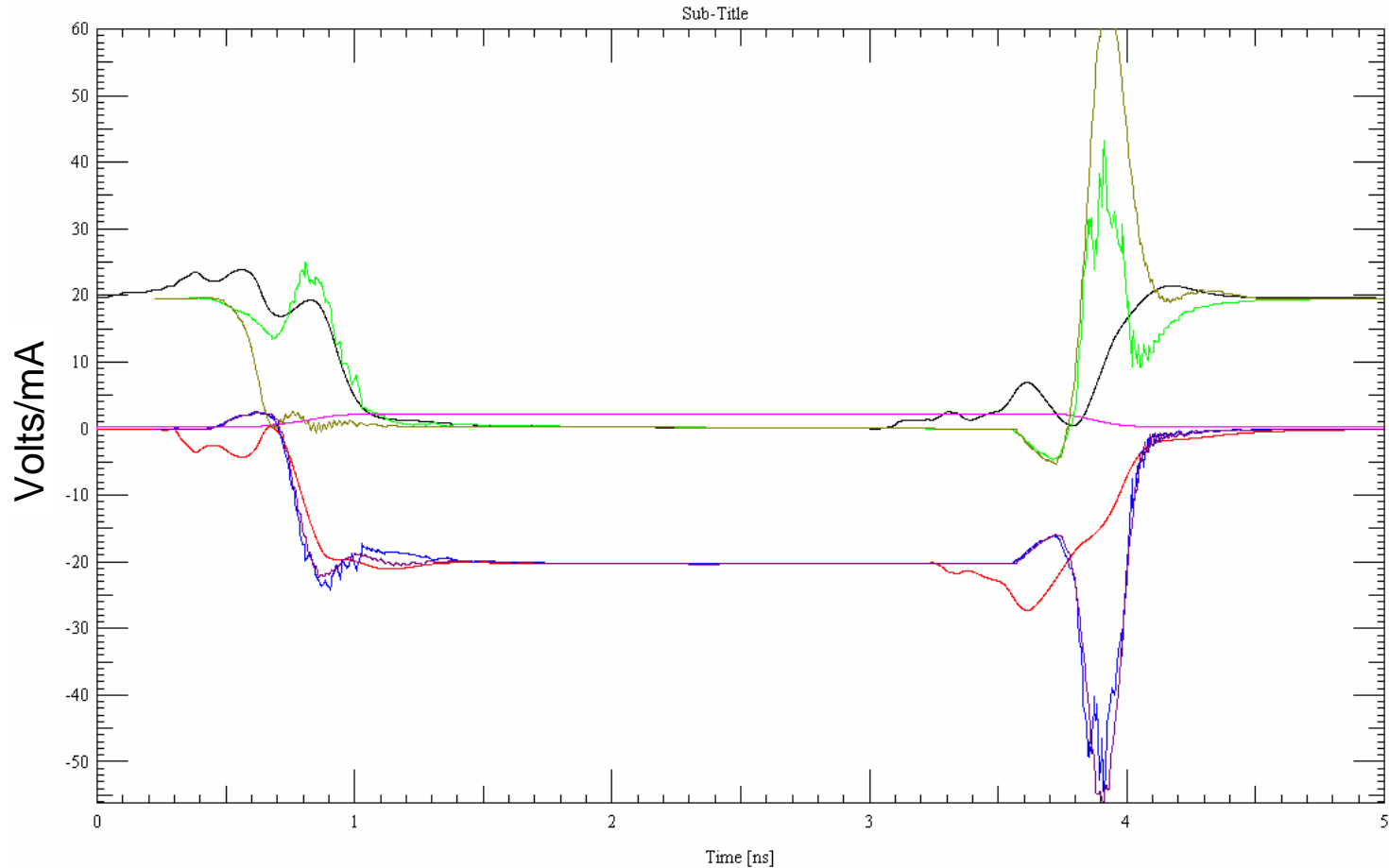
VCCQ and VSSQ Currents - Silicon vs. IBIS Simulator 1 - Fall Aligned IBIS





# Aligned IBIS Waveforms – 2 IBIS Simulators

VCCQ and VSSQ Currents - Silicon vs. IBIS Simulators 1 + 3 - Fall Aligned IBIS



— Silicon I(VCCQ)	— Silicon I(VSSQ)	— Silicon V(PAD)
— SIM 3 IBIS I(VSSQ)	— SIM 3 IBIS I(VCCQ)	— SIM 1 IBIS I(VSSQ)
— SIM 1 IBIS V(VCCQ)		

# Conclusions

- IBIS simulators differ slightly in **voltage** simulation (*at least for one off-the-shelf IBIS model*).
- IBIS simulators differ in how they handle pullup/pulldown turn-on/turn-off timing, and therefore power/ground currents, even with **correctly timed** IBIS waveform data.
  - BIRD 95 has been accepted to address this.
  - Kumar was right.
- IBIS simulators differ even more in how they handle pullup/pulldown turn-on/turn-off timing when IBIS waveforms have **incorrect time offset**.
- In the latter case the voltage waveform difference between simulators becomes only slightly worse.

