EIA IBIS Open Forum Summit Minutes

Meeting Date: **February 1, 2007**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2007 PARTICIPANTS

Actel	(Prabhu Mohan)
Agere	(Nirav Patel)
Agilent	Radek Biernacki*
AMD	Nam Nguyen, Tadashi Arai*
Ansoft Corporation	(Michael Brenneman)
Apache Design Solutions	(Ji Zheng)
Applied Simulation Technology	(Fred Balistreri)
Cadence Design Systems	Lance Wang*, C. Kumar*, Hemant Shaw*
Cisco Systems	Syed Huq*, Tram Bui*, AbdulRahman Rafiq*, Huyen Pham*, Darja Padilla*, Mike LaBonte* Paul Ruddy*, Gurpreet Hundal*, Luis Boluna* Ehsan Kabir*, Jehyoung Lee*, Susmita Mutsuddy* Eddie Wu*
Fluent	(Chetan Desai)
Freescale	Jon Burnett*
Green Streak Programs	Lynne Green
Hitachi ULSI Systems	Kazuyoshi Shoji*
Huawei Technologies	ChunXing Huang*, Bob He*
Integrated Circuit Systems (ICS)	(Dan Clementi)
Intel Corporation	Michael Mirmak*, Arpad Muranyi*
LSI Logic	Frank Gasparik, Kim Helliwell*, Dinh Tran*, Praveen Soora*
Mentor Graphics	John Angulo*, Ian Dodd*
Micron Technology	Randy Wolff*, Pavani Jella*
NEC Electronics Corporation	Hock Seow*, Huy Tran*
Panasonic	(Atsuji Ito)
Samtec	(Corey Kimble)
Siemens AG	Eckhard Lenski
Signal Integrity Software	Barry Katz*, Douglas Burns*, Mike Steinberger*, Walter Katz*, Todd Westerhoff*
Sigrity	Sam Chitwood*, Sandy Dung*
Silego	(Joe Froniewski)
STMicroelectronics	Antonio Girardi, Giacomo Bernardi Roberto Izzi
Synopsys	Ted Mido*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino*

Texas Instruments	Otis Gorley, Richard Ward*
Toshiba	(Yasumasa Kondo)
Xilinx	Bruce Bandeli*
ZTE	(Shunlin Zhu)
Zuken	(Michael Schaeder)

OTHER PARTICIPANTS IN 2007

74ze Engineering	Linc Jepson*
Altera	Hui Liu*, Zhe Lin*, Ravindra Gali*, Salman Jiva*
Applied Telisis, Inc. (ATI)	Vladimar Mandrusov*
ChipX	Jay Hidy*, Oren Dvir*
Cybernet Systems	Kazuhiki Kusunoki*
Enterasys	Robert Haller*
Extreme Networks	Kevin Ko*
GEIA	(Chris Denham)
Hewlett Packard	Shafiq Rahman*
Ericsson	Anders Ekholm*, Ole Segtum*
Force10 Networks	Robert Badal*
IBM	Michael Sorna*, Adge Hawes*
Leventhal Design	Roy Leventhal
National Instruments	Lee Maixman*
Netlogic	Eric Hsu*
NESA	Edward Sayre*
Nuova Systems	Zhiping Yang*, Lin Shen*
NXP	H N Sudarshan*
Optimal Corporation	Marc Kowalski*
Renesas Technology	Takuji Komeda*
Samsung	Sang-Soo Park*
Sedona International	Joe Socha*
Sun Microelectronics	Leon Yang*
Tiburon Design Automation	Patirick Challacn*
White Electronics Designs	John Perez*
Xyratex	Paul Levin*, Joseph Chan*

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Telephone Number	Bridge #	Passcode
February 16, 2007	1-916-356-2663	2	462-8469

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven

days of the corresponding meeting. When calling into the meeting, provide the bridge number and passcode at the automated prompts. If asked by an operator, please request to join the IBIS Open Forum hosted by Michael Mirmak. For international dial-in numbers, please contact Michael Mirmak.

NOTE: "AR" = Action Required.

INTRODUCTIONS AND MEETING QUORUM

The IBIS Open Forum Summit was held in Santa Clara, California at the Hyatt hotel during the 2007 DesignCon Conference. About 77 people representing 42 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/ibis/summits/feb07/

Michael Mirmak opened the meeting by thanking the cosponsors, IEC, the organizers of DesignCon, and Cisco for sponsoring the lunch. Michael asked attendees to indicate if they were model users, tool vendors, or model makers. There were 15 users, 7 tool vendors, and 16 model makers present at the start of the meeting. Michael also introduced the officers. Michael asked about any opens or discussion topics. There were none at this time.

IBIS CHAIR'S REPORT AND ISSUES SUMMARY

Michael Mirmak, Intel Corp.

Michael began by summarizing events for 2006 and upcoming events for 2007. He also mentioned the status of parser development and finances. He displayed a chart with membership trends showing recent increases. He summarized the main tasks of the IBIS task groups including the Ad Hoc Interconnect, Advanced Technology Modeling, Model Review, and Quality groups. Michael listed the BIRD queue for inclusion in IBIS 5.0. He asked the questions of “Are we making progress?” and “Are we missing something?” He noted that we are moving from a circuit view to modeling at a system level. He noted that the average platform signal is 830 MHz in North America, and in two years it will be 1.4 GHz. He argued that this technology still falls between the modeling level of IBIS 3.2/4.0 and “Future IBIS.” He proposed that we should increase our focus on cookbooks, templates and tools for the “middle group” of builders and users. Mike Steinberger of SiSoft encouraged IBIS to focus on education of the SI community.

STUDY OF IBIS WAVEFORM TIME OFFSETS

Mike Labonte, Cisco Systems, Inc.

Mike began with a little background on the relationship between turn-on and turn-off times of the pullup and pulldown transistors in a buffer. He showed four sets of V-T waveforms with normal offset and four sets with abnormal alignment. Mike ran a simulation with three IBIS simulators and a silicon Spice simulator. He ran test cases of the IBIS model with normal V-T waveforms, falling waveforms aligned in time, and no waveforms at all. He showed that with the misaligned waveforms, there was slightly worse agreement between the three simulators than with the

normal models. With no V-T waveforms, there were significant differences between how the three simulators handled the transition regions outside of the 20% to 80% switching regions. Mike then showed the differences in VSSQ and VCCQ currents between the three simulators. Mike summarized that the biggest difference was noticed in the I-T results between the simulators.

Michael Mirmak commented that perhaps the difference in the simulator results was not in how they handle the data they have, but in how they handle the data they don't have such as frequency dependent C_comp, I-T data, etc.

INITIAL TIME DELAY ISSUE IN IBIS VT CURVES

Lance Wang, Cadence

Lance wanted to investigate the difference between IBIS models and transistor level models when the switching frequencies increase. Lance simulated with a test topology of 50 ohms to ground using a test stimulus of 5 ps. He used one Spice and two IBIS simulators. There were perfect matching results between all three with just one rising or one falling edge transition. He then simulated with different bit widths using full V-T waveforms, cutting off initial delay from V-T waveforms and not using any waveforms. There was poor agreement between IBIS and Spice at short bit periods and good agreement at longer bit periods. Cutting off the initial delay of the V-T waveforms had little effect.

Todd Westerhoff commented that he agreed that the initial delay effects causing the model to be valid only for slower bit periods is correct, but that the problem limiting the model is only the time it takes for the model to reach steady state. Some discussion ensued regarding overclocking of IBIS models and the time correlation between the various corners of V-T waveforms. It was agreed that removing the initial delay of V-T waveforms was useful in allowing the model to switch at faster frequencies.

IBIS QUALITY COMMITTEE REPORT

Kim Helliwell, LSI Logic

Kim showed a sample from the IBIS Quality specification and the IBIS Quality checklist. He then talked about the old classification scheme for levels of quality from 0 to 3. He then detailed several issues with this classification scheme. He introduced a new classification scheme that combines levels 0 to 4 with appended letters indicating further qualifications and listed advantages of the new scheme. Kim mentioned parser BUGs related to non-monotonic warnings and the parser permitting Vmeas levels not between Vinh and Vinl values. He detailed the checks required for each level.

Lance Wang asked about whether we should specify the particular simulator used for simulation correlation. Kim mentioned that this would need to be discussed further. Randy Wolff asked about the ability to release models with errors related to parsers by documentation of the error with the new "X" qualification. Kim recommended releasing versions of the model that don't include the errors.

X

Bob Ross, Teraspeed Consulting Group

Bob's presentation is related to the exceptions in IBIS models that are documented. These exceptions are real. Bob showed a model where there was a shutdown circuit in the power clamp region that causes warnings in ibischk4. One choice was to remove the glitch; the other was to leave it in. In either case, it should be documented with an X in the quality report. He then showed an example where pulldown I-V tables do not cross through 0 current at 0 volts. He then detailed the BUG93 problem. Bob concluded that there are lots of exceptions that can occur, and it is important to document them all.

ADAPTIVE DFE MODELING USING IBIS 4.2/VHDL-AMS

Luis Boluna, Ehsan Kabir, Susmita Mutsuddy, AbdulRahman Rafiq, Cisco Systems Inc.

Luis Boluna presented for the group. Luis started with a summary of past VHDL-AMS projects. He said that DFE is a complex feature to model, and they are addressing this challenge with IBIS 4.2. A Decision Feedback Equalizer (DFE) is a digital equalizer designed to remove primarily ISI. He showed that there are many ways to architect a DFE. Luis detailed the Least Mean Square (LMS) algorithm. He then showed some of the VHDL-AMS code to implement this algorithm. Luis showed results of the AMS simulation for a 2 tap and 4 tap DFE. He noted that the model can be improved, but the concept of modeling a DFE in VHDL-AMS is verified. The Cisco team is expanding to now cover SerDes modeling, simulation, and measurement. He also noted that Matlab and VHDL-AMS correlated very well for the DFE model.

STATISTICAL EYE ANALYSIS IMPLEMENTED IN VHDL-AMS

Arpad Muranyi, Intel Corp.

Arpad started with background on his work modeling Peak Distortion Analysis (PDA) with VHDL-AMS models. He noted that numerous statistical methods have been developed to model SerDes drivers and receivers, and the challenge is to bring these algorithms to SI tools in a standardized format (IBIS). He is promoting the use of AMS modeling by showing how statistical eye and BER algorithms can be implemented in AMS, specifically VHDL-AMS. He detailed his simulation setup including generation of a channel giving a reasonable pulse response. He then gave an overview of the operation of the model including the flow of the simulation's top-level circuits and functions. He then showed results of the pulse response simulations and generated statistical eye contours. He summarized that this experiment implemented only the basic equations of statistical eye analysis not including cross talk and jitter. Future work may include implementation in Verilog-A(MS) and also implementation of the algorithm in the frequency domain.

IBIS MODELING OF USB BUFFERS

Sudarshan Honnudike, NXP Semiconductors

Sudarshan introduced his topic as his desire to share his experiences with learning IBIS and modeling a USB buffer. He modeled low speed and full speed modes of operation. The driver is made of two parallel single ended buffers. The receiver has two parallel single ended buffers and a differential receiver. He explained that a valid input signal is defined with both single ended and differential [Receiver Thresholds] levels. However, this is not possible in a single model. He proposed adding a new type of [Model] that requires both single ended and differential thresholds. He also expressed interest in reducing duplication of tables in an IBIS model by allowing I-V tables to reference a name corresponding to a [Model] that includes the table of interest. He went on to explain how USB has two modes of operation: upstream and

downstream. The only difference between these modes for modeling is a different test load (Rref, Cref, Vref). He requested the IBIS community look into allowing a single model to include multiple timing test load values.

Walter Katz commented that he sees this issue of duplication with models and switching levels information often, and he would also like to see a way to simplify the models. Sudarshan then clarified the operation of the USB interface in single ended and differential modes.

OPENS/DISCUSSIONS

Todd Westerhoff commented that people have a hard time using the tools on the market. He encouraged any efforts we want to undertake as a community to explain to users what they really need in order to solve each problem including SI and timing.

Walter Katz expressed interest in putting more information into IBIS models to handle derating of timing like the kind you find in DDR2 and DDR3 memory technologies. Arpad mentioned that this had been done with AMS models. Todd Westerhoff made the comment that he did not like people referring to use of AMS to model things, when in reality you have Verilog-AMS and VHDL-AMS that are incompatible. Discussion ensued about the role of AMS in advancing modeling. One issue brought up was the need for EDA tools to support both VHDL-AMS and Verilog-AMS so that model makers don't have to provide models in both formats. Ian Dodd expressed that Verilog-A is the lowest common denominator that all the EDA vendors could look to provide. Arpad mentioned that his work for SerDes modeling could be implemented in Verilog-A, but it would not run as fast as when using the full digital simulator.

IBIS ADVANCED TECHNOLOGY MODELING GROUP (IBIS-ATM) STATUS REPORT

Todd Westerhoff, SiSoft

Todd mentioned that the ATM group was originally the Macromodel group. The ATM group's current goal is to define a transmitter/receiver modeling standard for SerDes channel analysis that encompasses equalization and clock recovery. Todd referenced Arpad Muranyi's recent work on modeling peak distortion analysis. The group recently investigated the ability to support parameter passing to [External Model] Spice. Synopsys declined to allow their syntax for HSPICE to be made publicly available, but the committee could still adopt the syntax for parameter passing if a proposal (BIRD) is brought forward. The group has been discussing in detail a proposal from Cadence on API. The group is also discussing how you simulate in both a circuit simulation format as well as doing signal-processing analysis. There is also a lot of discussion about how to distribute the models. Todd mentioned terminology presentations that are available. The group will be discussing more terminology and reviewing Cadence's proposal further.

Mike explained the difference of semi-analytical versus statistical approaches to channel analysis. Ian Dodd mentioned that time domain and statistical techniques are complementary. The point was made that the group was not supporting one technique over another, just proposing how to get all the information necessary into the EDA tools so that the tools can use whatever technique they want to.

CONCLUDING ITEMS

Michael Mirmak thanked Cisco for providing the lunch. He also mentioned the upcoming IBIS

Open Forum meeting as well as the DATE summit meeting.

NEXT MEETING

The next IBIS Open Forum teleconference will be held February 16, 2007 from 8:00am to 10:00am US Pacific Time.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda-stds.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda-stds.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda-stds.org)
IBIS Users' Group Reflector (ibis-users@eda-stds.org)
State your request.

ibis-info@eda-stds.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/
http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm_bugs/
http://www.eda-stds.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

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GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	December 8, 2006	January 5, 2007	January 26, 2007	February 1, 2007
Advanced Micro Devices	Producer	Active			√	√
Agere Systems	User	Inactive				
Agilent Technologies	User	Inactive				√
Ansoft	User	Inactive				
Apache Design Solutions	User	Inactive				
Applied Simulation Technology	User	Inactive				
Cadence Design Systems	User	Active	√		√	√
Cisco Systems	User	Active	√	√	√	√
Fluent	Producer	Inactive				
Freescale Semiconductor	Producer	Inactive				√
Green Streak Programs	General Interest	Inactive	√		√	
Hitachi ULSI Systems	Producer	Inactive				√
Huawei Technologies	User	Inactive				√
Integrated Circuit Systems	Producer	Inactive				
Intel Corp.	Producer	Active	√	√	√	√
LSI Logic	Producer	Inactive		√		√
Mentor Graphics	User	Active	√	√	√	√
Micron Technology	Producer	Active	√	√	√	√
NEC Electronics Corp.	Producer	Inactive				√
Panasonic	Producer	Inactive				
Samtec	Producer	Inactive				
Siemens AG	Producer	Inactive	√		√	
Signal Integrity Software	User	Inactive				√
Sigrity	User	Active			√	√
Silego	Producer	Inactive				
STMicroelectronics	Producer	Inactive			√	
Synopsys	User	Inactive				√
Teraspeed Consulting Group	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Active			√	√
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive	√			√
ZTE	User	Inactive				
Zuken GmbH	User	Inactive				

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.