Initial Time Delay Issue in IBIS VT Curves

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Motivation

- The results from Spice Transistor-level models and IBIS models sometimes are different:
    - What:
        - IBIS model is generated from Spice Transistor-level model
        - It contains an initial delay
    - When:
        - When stimulus switching frequency gets higher, the timing of rising and falling edges are very different than Spice model simulation result. It is not showing "ISI" facts as the results from Spice model simulations.
   - Why?
        - Let's find out

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Test Topology

- Driver model
  - Using both Transistor-Level Spice model and IBIS model which generated from Transistor-level model

- 50 Ohm to Ground (One of the VT curve set conditions / Ramp data conditions)

- 5ps rising/falling edges in stimulus

- Focus on the output node of Driver

- Used 1 Spice and 2 IBIS simulators

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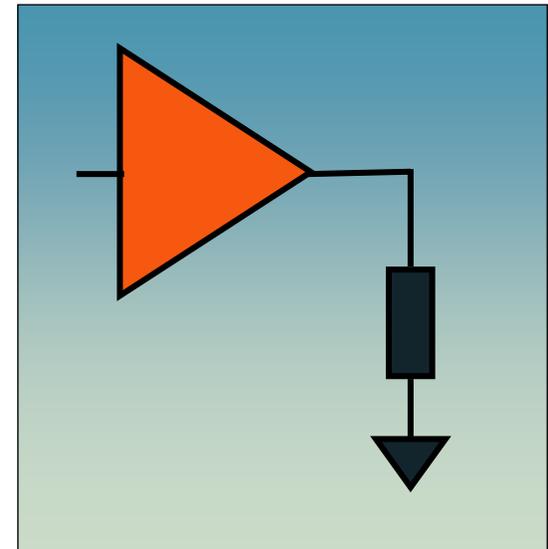
Driver Model:
Transistor-level Spice model vs. IBIS model

- Perfect matching results on Rising and Falling between all three simulators

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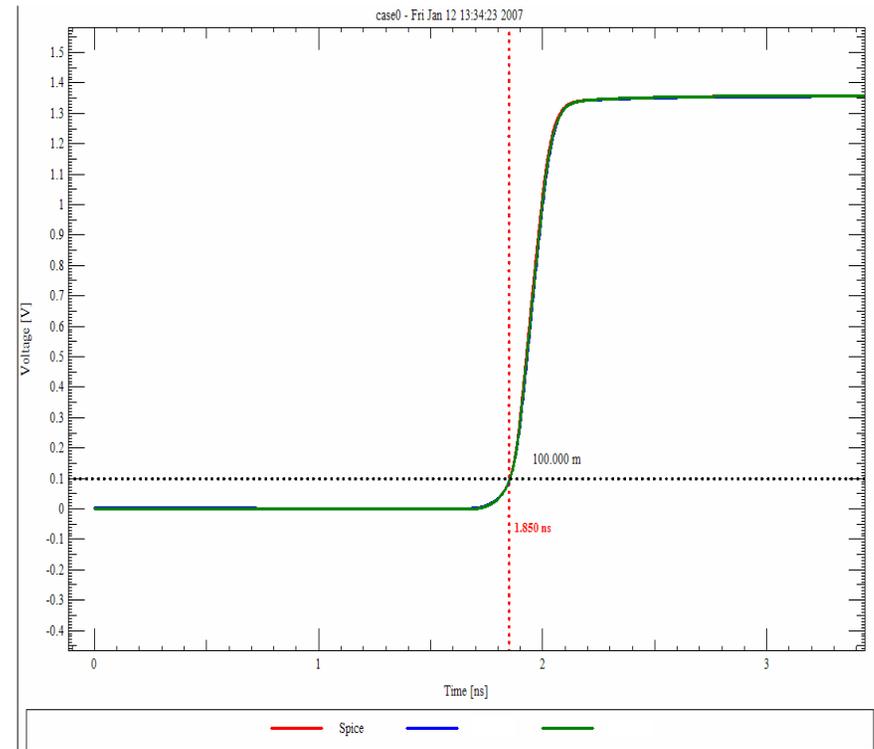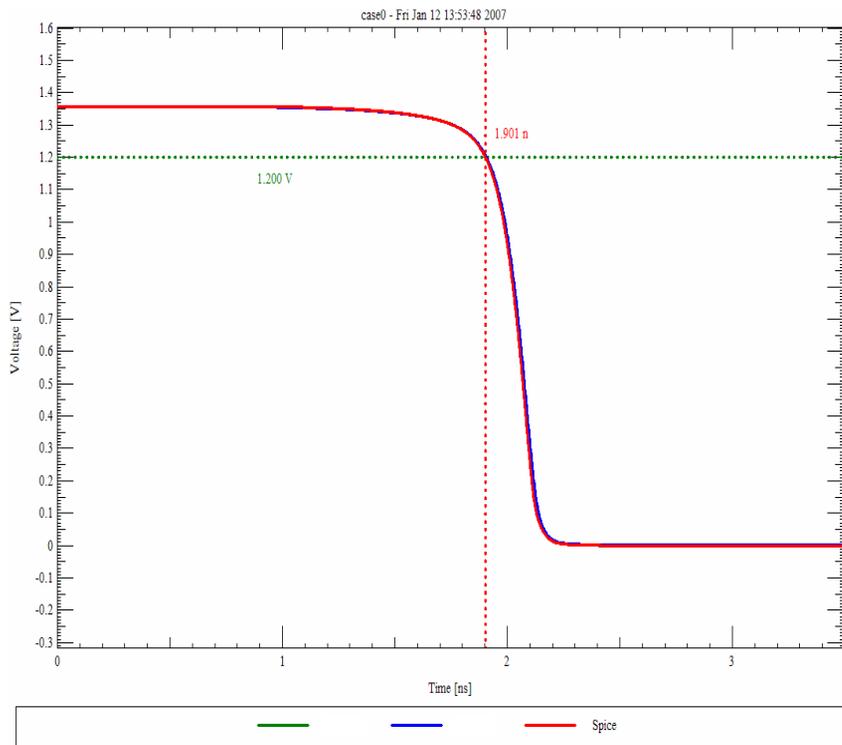
Using this model in different speeds (BPS)

- Using 2ns, 4ns and 6ns bit width
  - With full VT waveforms
  - Cut off 1ns delay from VT waveforms
  - Not use VT waveforms
- Using 1ns, 2.5ns, 5ns, 7.5ns and 10ns bit width
  - With full VT waveforms
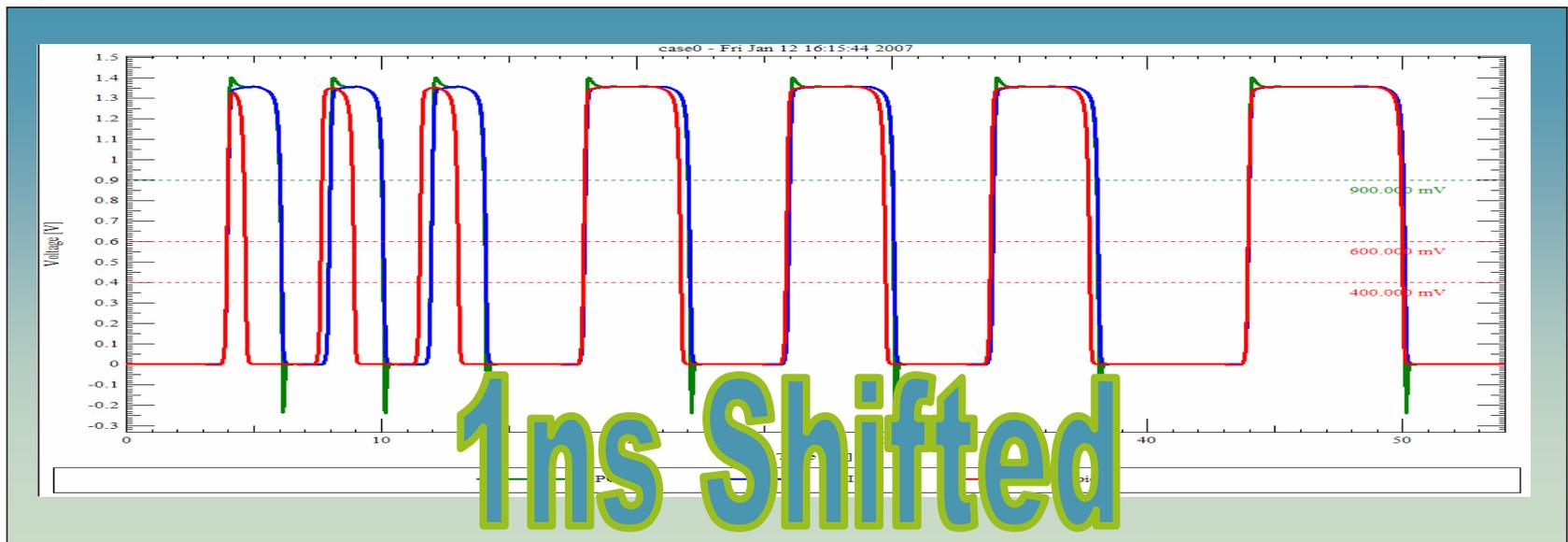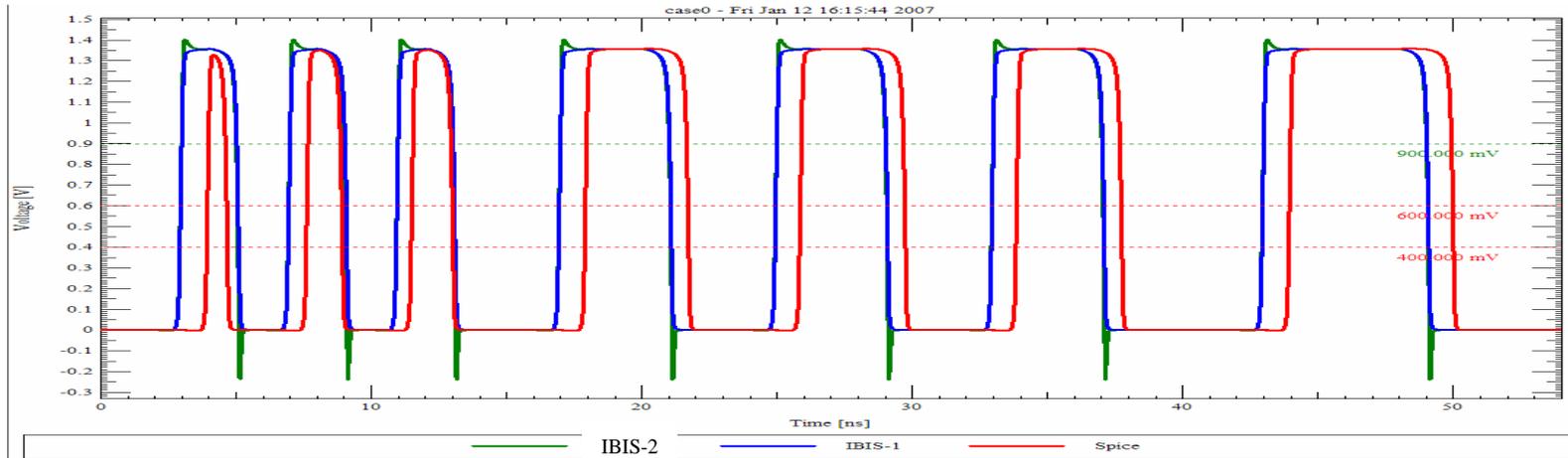 - Cut off 1ns delay from VT waveforms
  - Not use VT waveforms

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With full VT waveforms
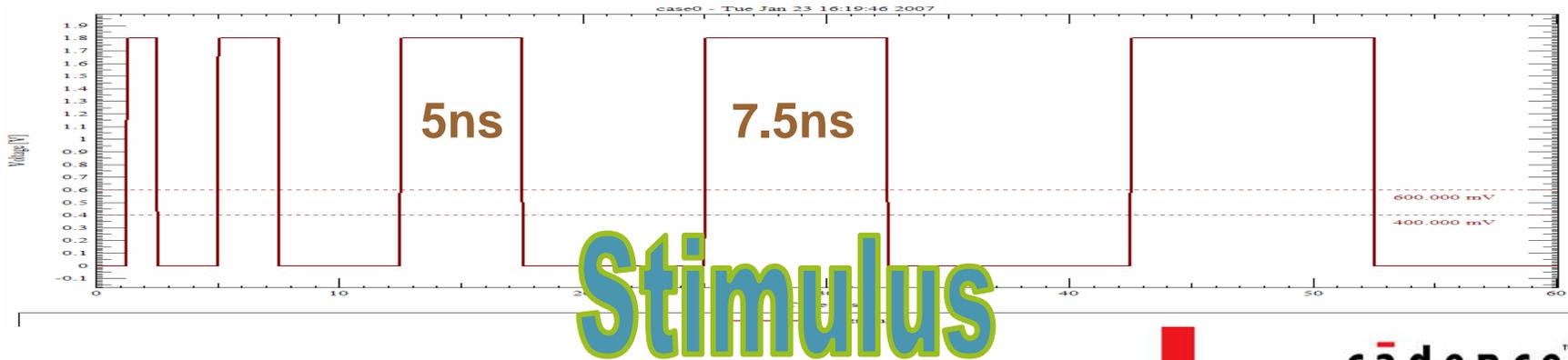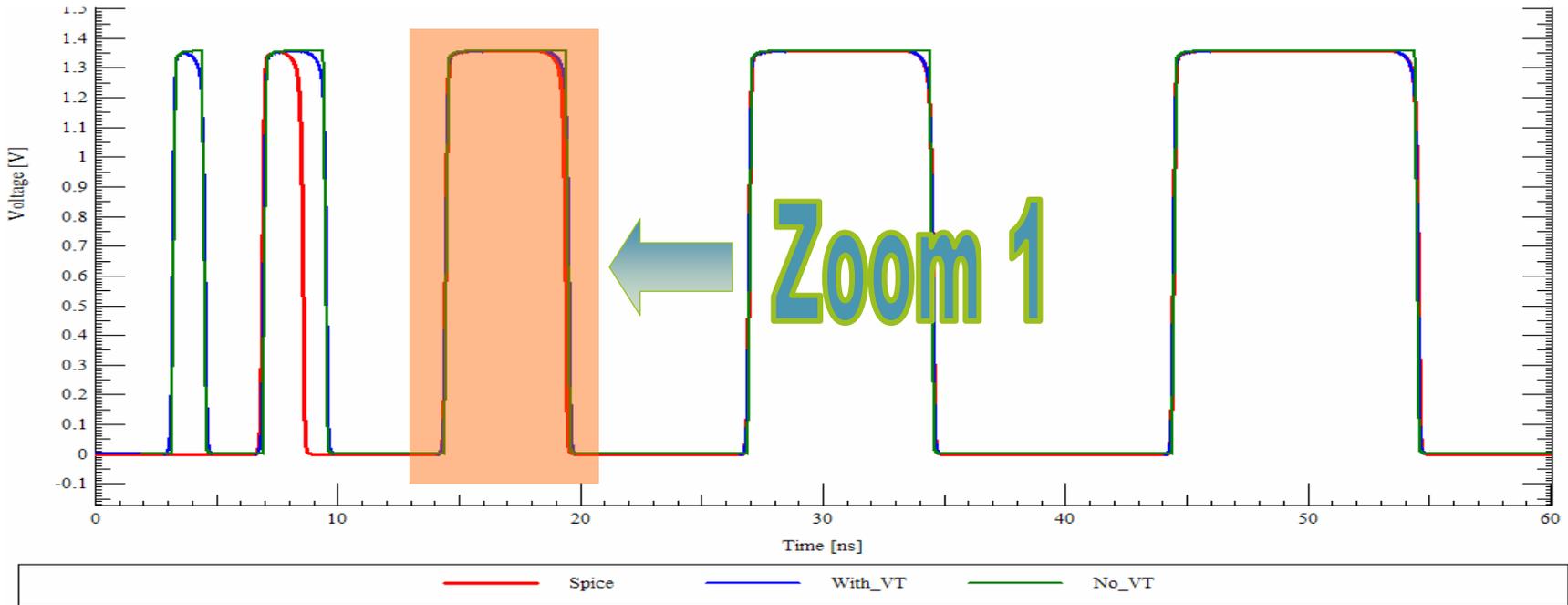## - Stimulus patterns "010101001100110011000111000"

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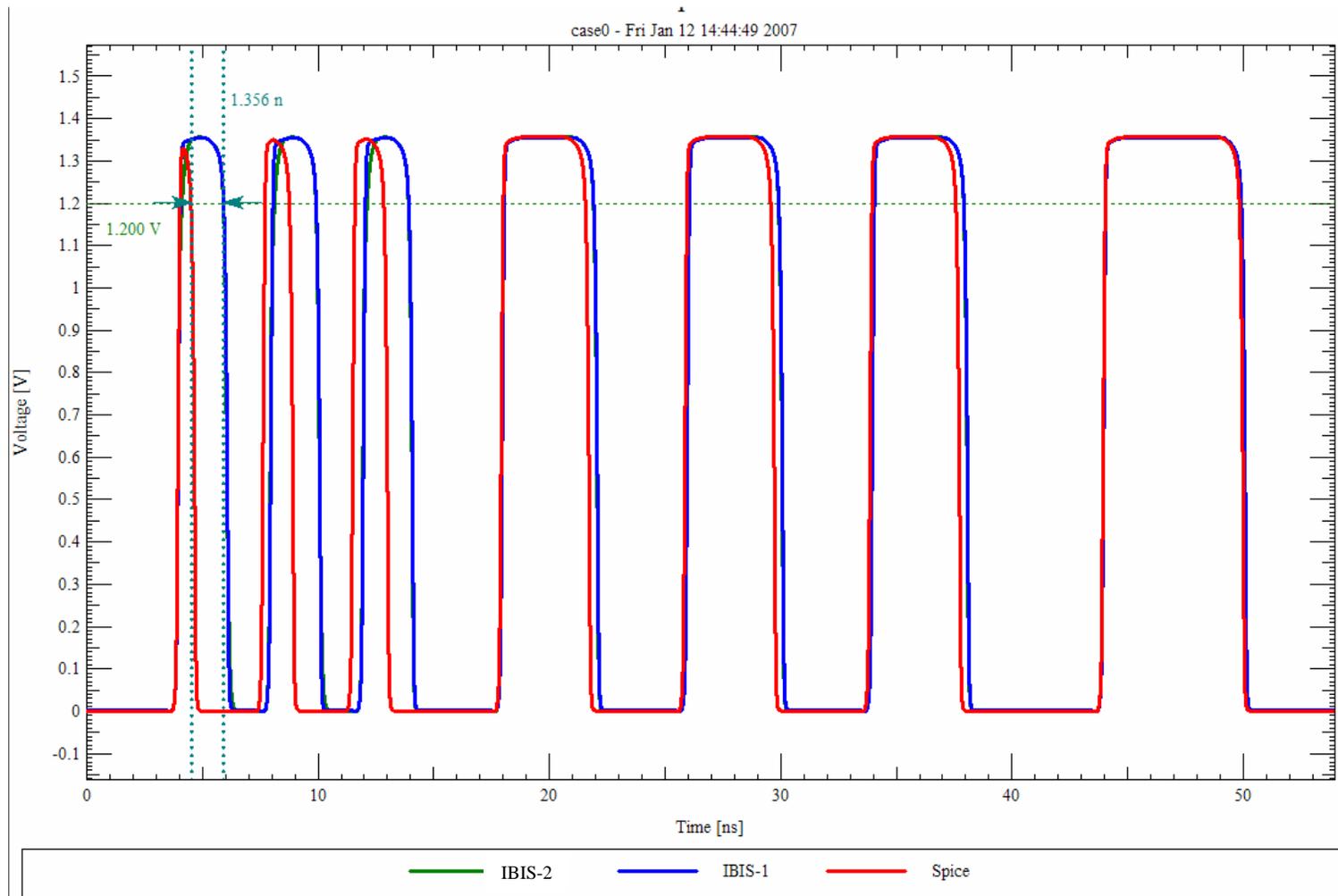
With cut off 1ns delay VT waveforms
- Stimulus patterns "010101001100110011000111000"
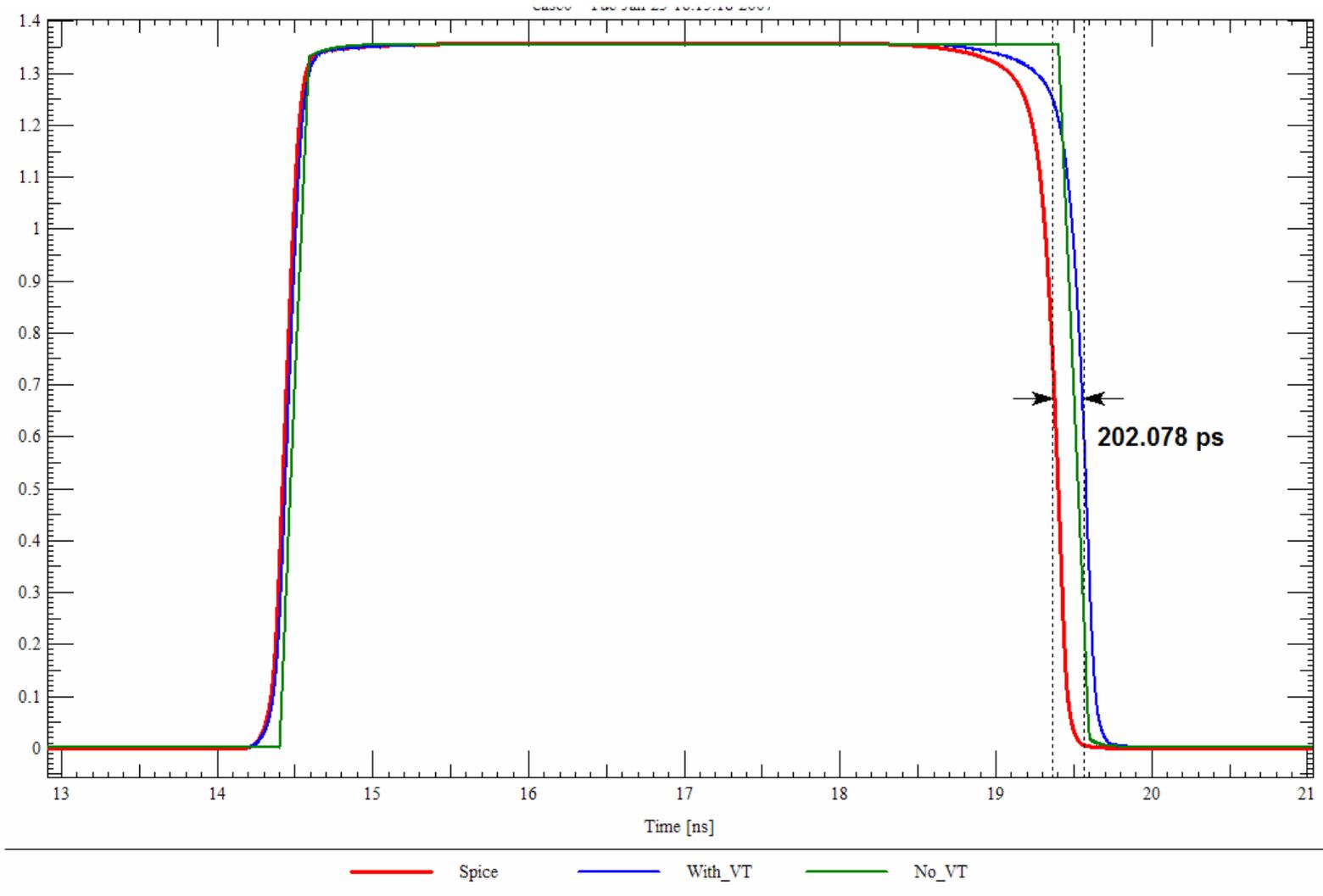
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IBIS Simulator-1
- Spice vs. with_VT vs. no_VT

IBIS Simulator-1 (5ns bit width)
- Spice vs. with_VT vs. no_VT (Zoom-1)

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IBIS Simulator-1
- Spice vs. with_VT vs. no_VT

IBIS Simulator-1 (7.5ns bit width)
- Spice vs. with_VT vs. no_VT (Zoom-2)

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IBIS Simulator-2
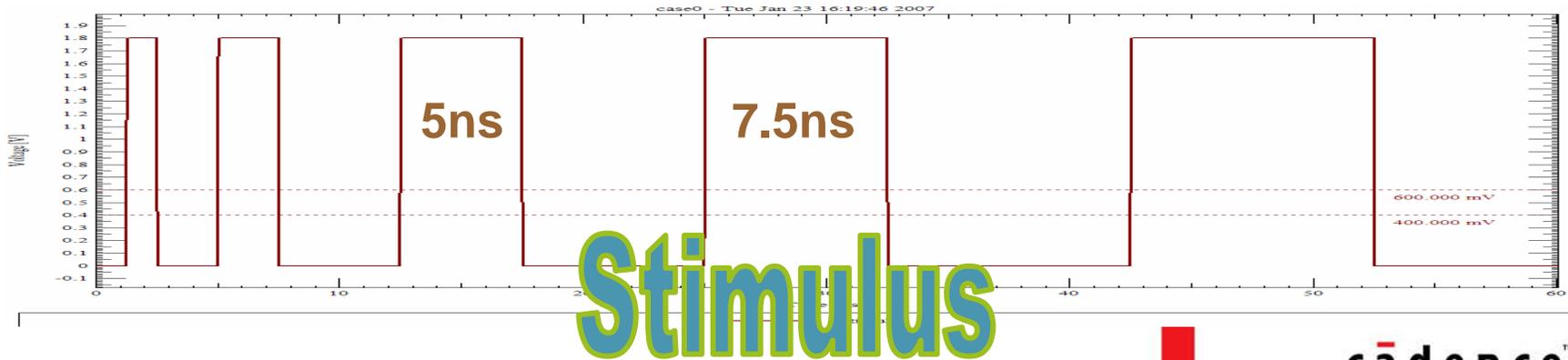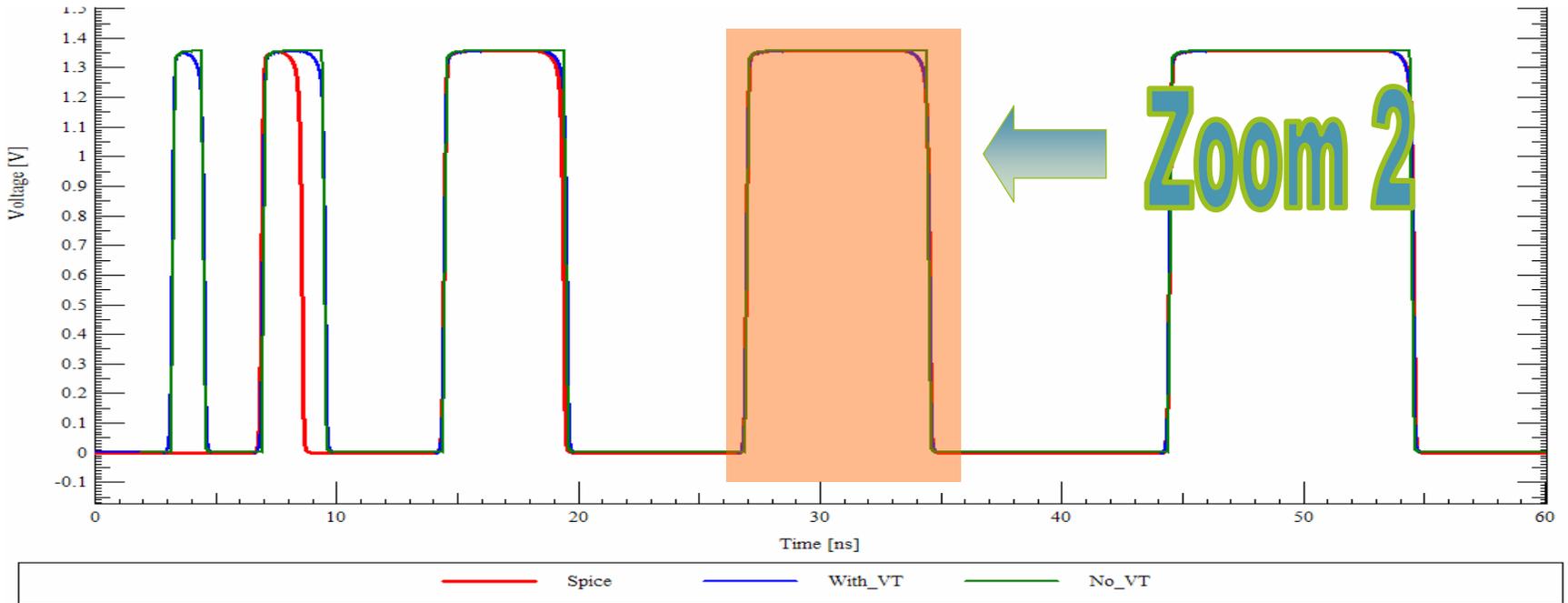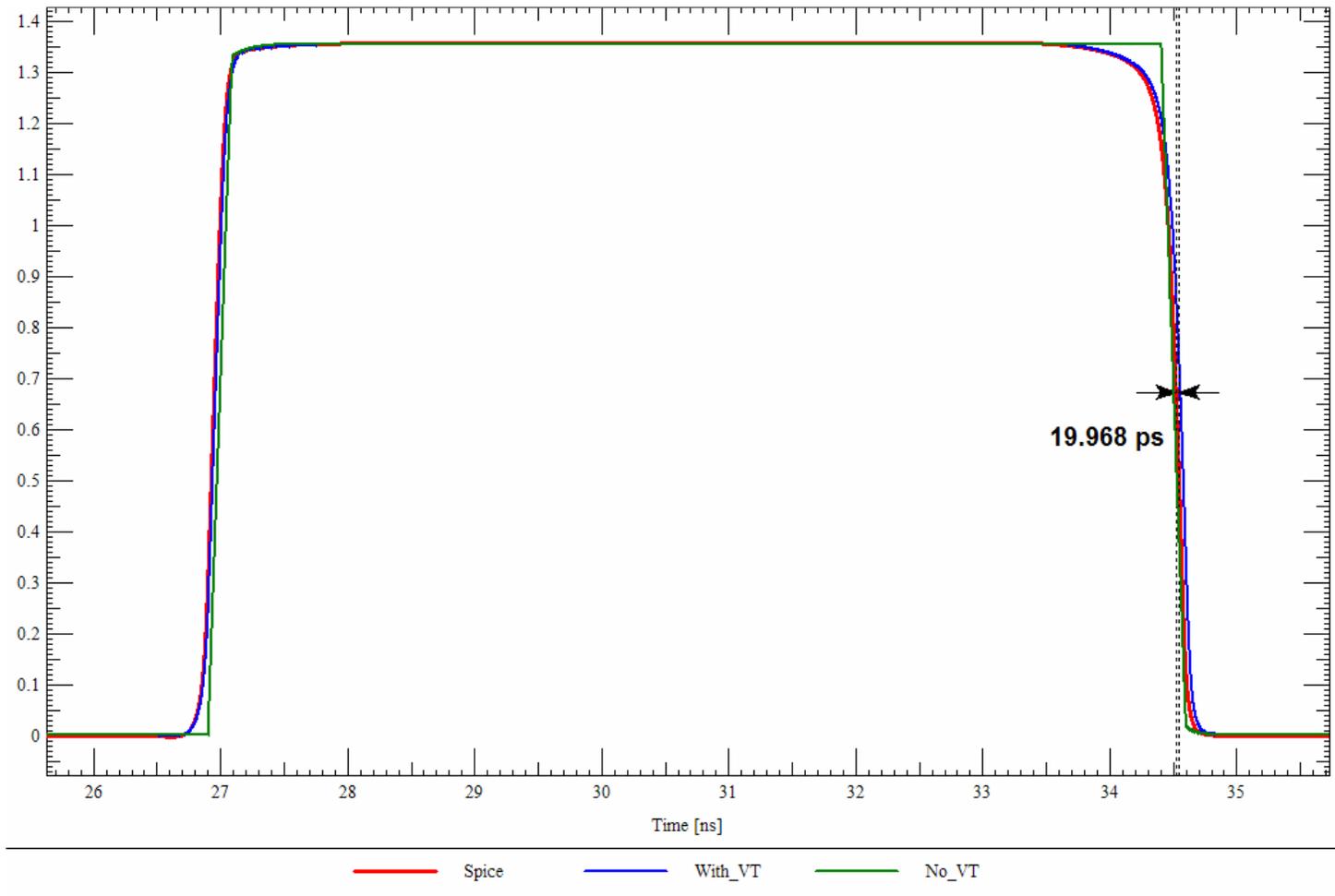# - Spice vs. with_VT vs. no_VT
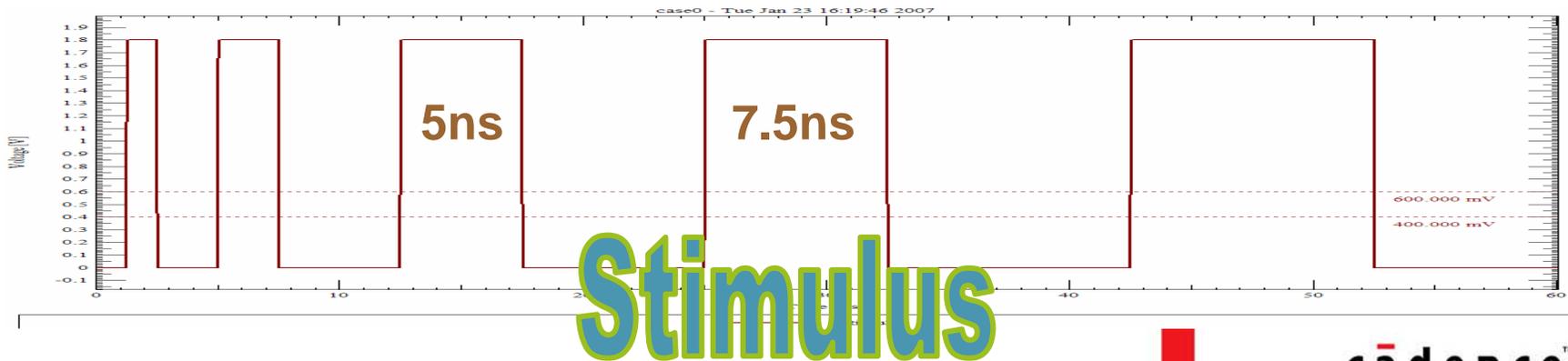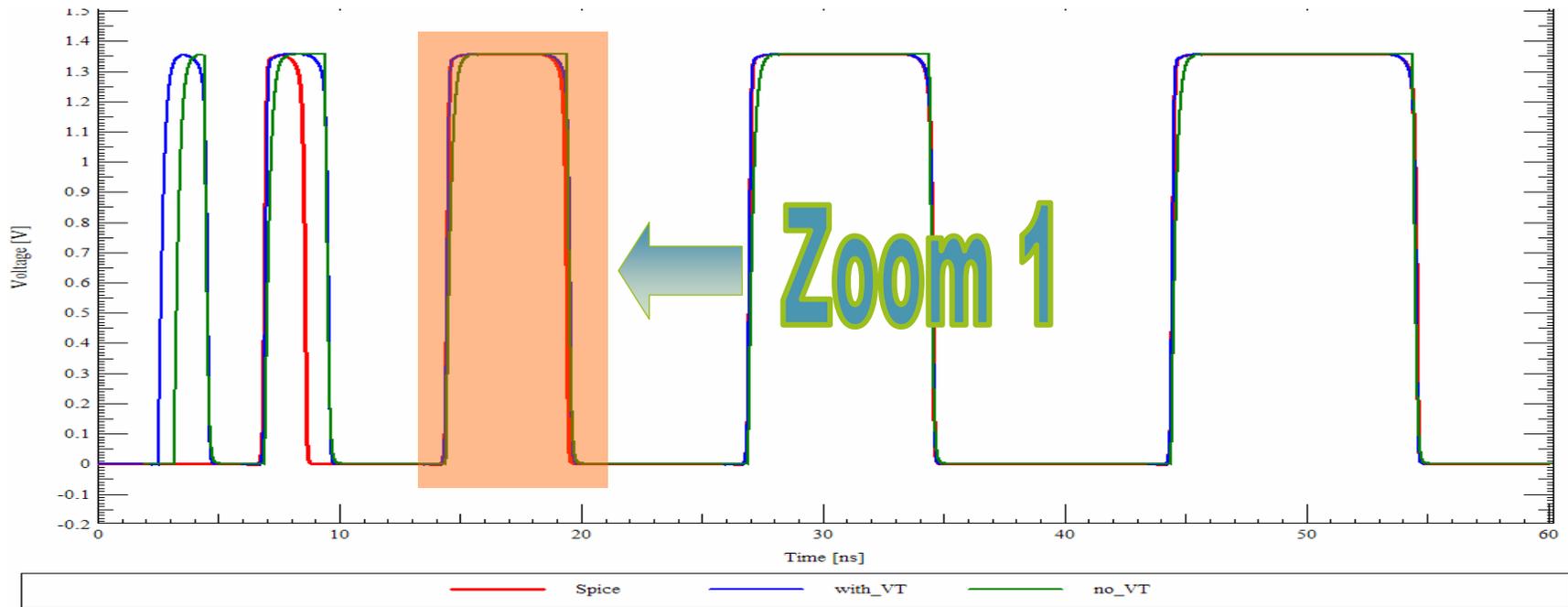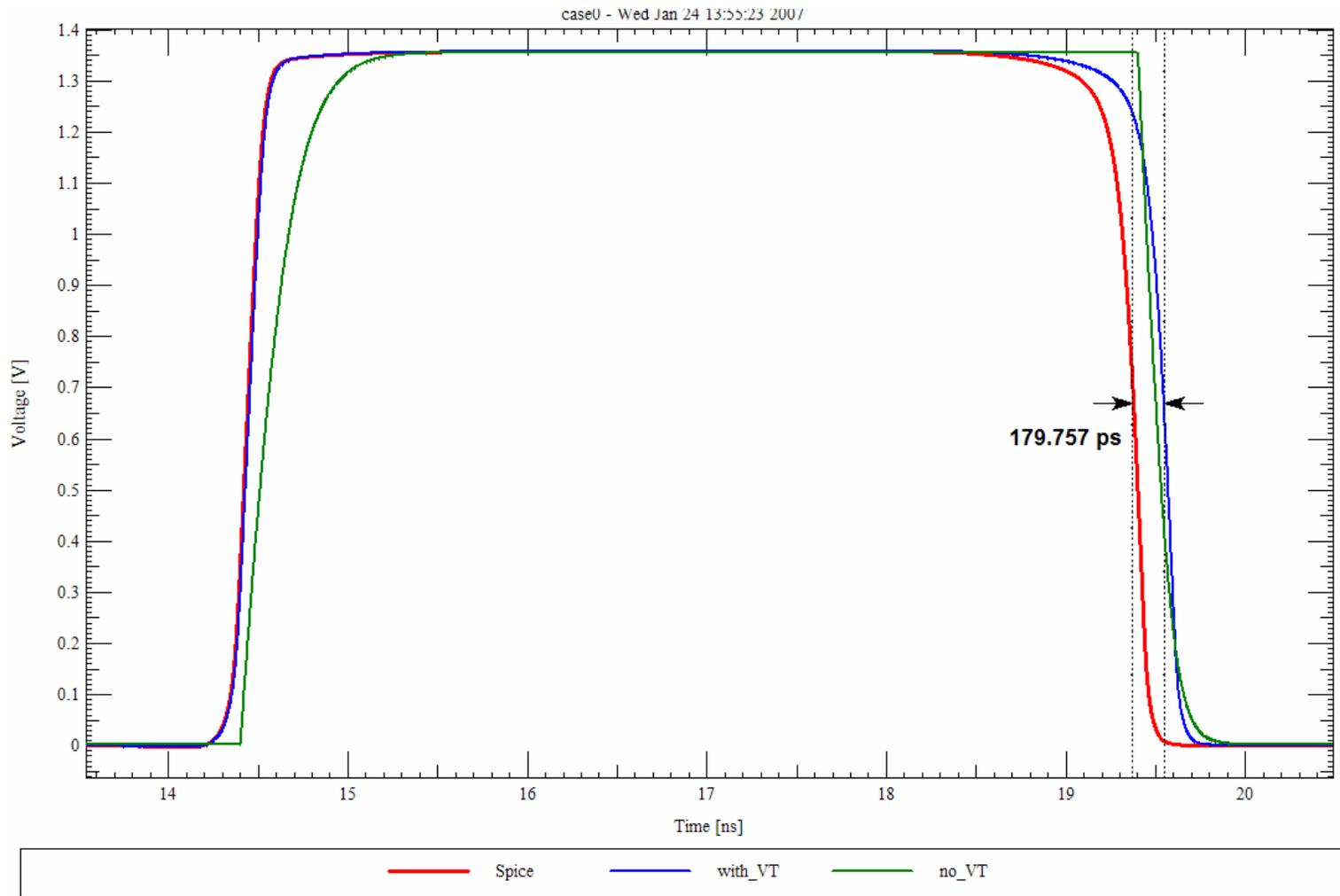
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IBIS Simulator-2 (5ns bit width)
- Spice vs. with_VT vs. no_VT (Zoom-1)

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IBIS Simulator-2
- Spice vs. with_VT vs. no_VT

Zoom 2

| Spice | with_VT | no_VT |

5ns   7.5ns

600.000 mV
400.000 mV

Stimulus

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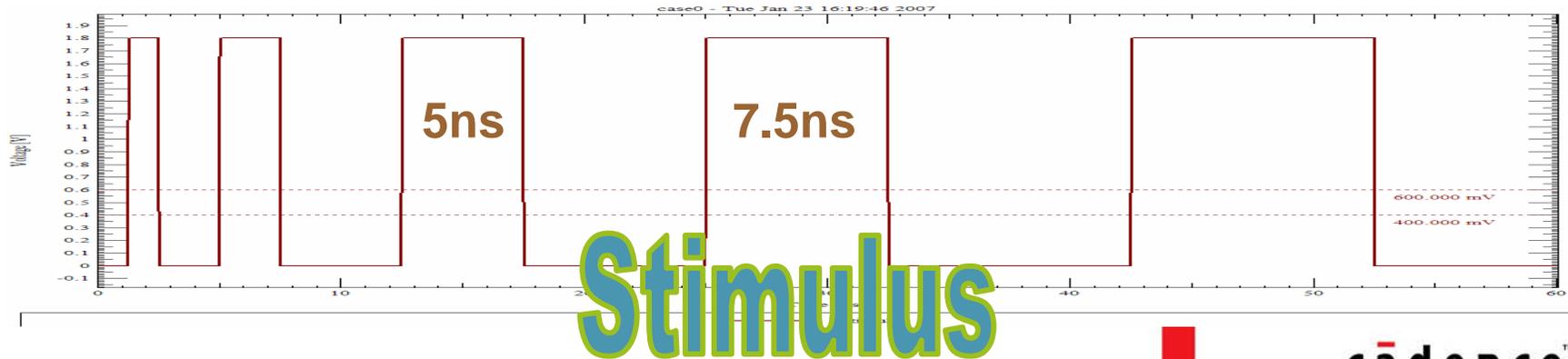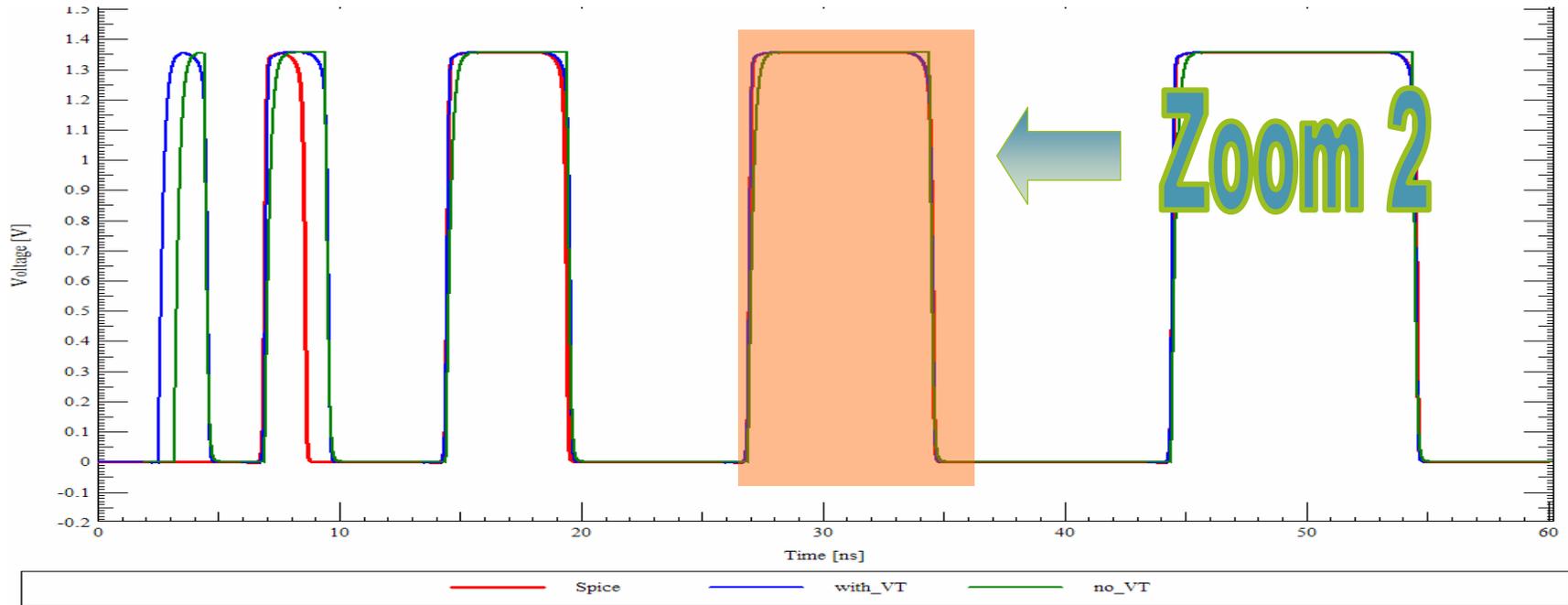
IBIS Simulator-2 (7.5ns bit width) - Spice vs. with_VT vs. no_VT (Zoom-2)

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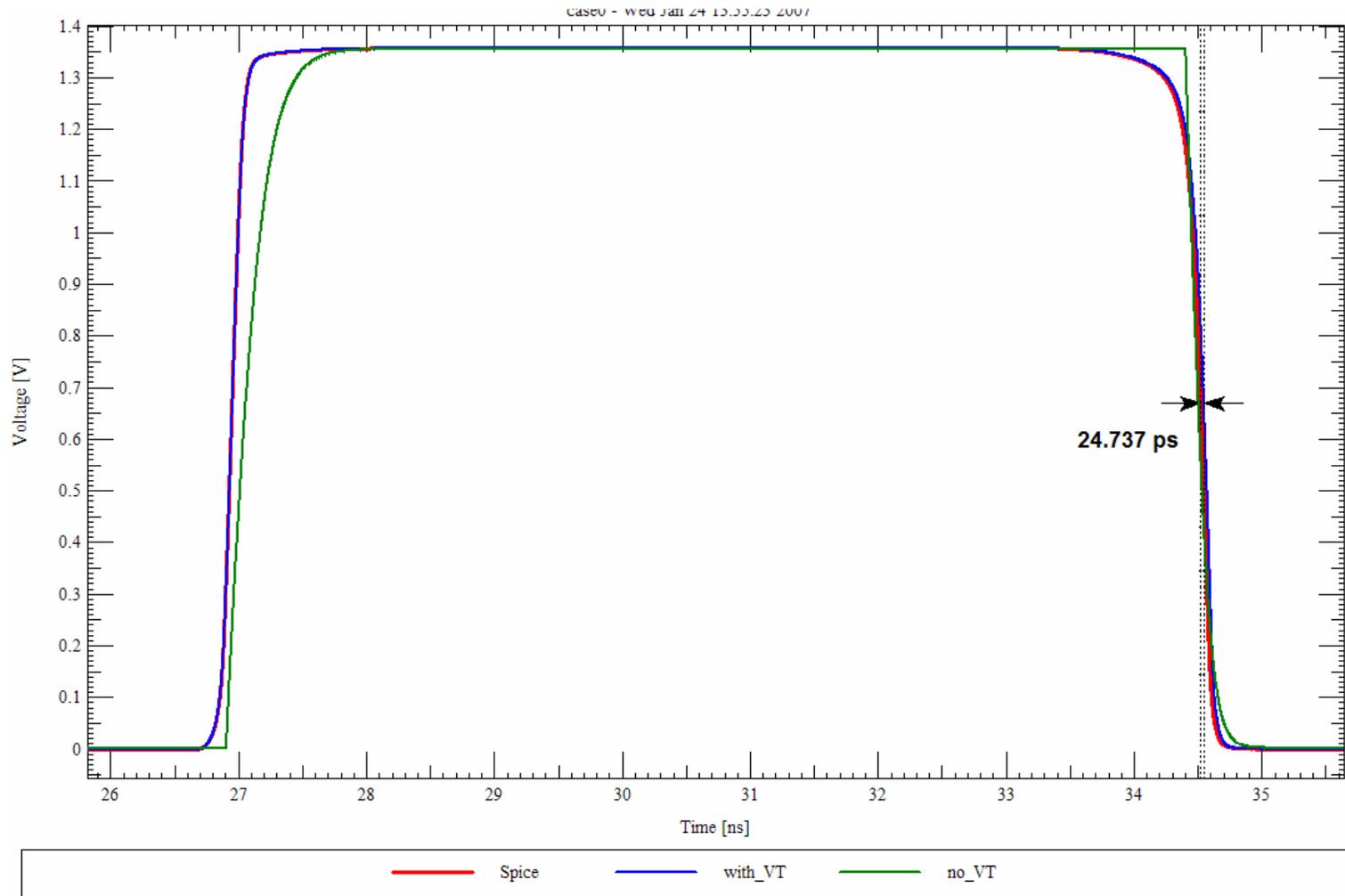
Summary of the results

- There is about 1.6ns "initial" delay in the VT waveform
  - 10pf C-comp, 50 Ohm load
  - dV/dT: 0.8V/115ps
- There are huge differences between Spice and IBIS simulations for this driver when bit width is shorter than 2.5ns; There are perfect matches between Spice and IBIS simulations for this driver when bit width is longer than 10ns
- With 5ns bit width, there is 202ps / 179ps (12.6% / 11.2% over 1.6ns delay) difference between Spice and IBIS simulations for this driver
- With 7.5ns bit width, there is only 20ps / 25ps (1.25% / 1.56% over 1.6ns delay) difference between Spice and IBIS simulations for this driver

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Analysis

- Need to have enough charge/discharge period for Die Capacitance when there is a long "initial" delay in the IBIS VT curves (relatively with rising/falling slew rate)
  - 2.5ns bit width / 1.6ns = 1.56 times (unacceptable results)
  - 5ns bit width / 1.6ns = 3.125 times (acceptable threshold, about 10%)
  - 7.5ns bit width / 1.6ns = 4.68 times (acceptable, about 1%)
- How long (bit width) is safe?
  - Less than 2 x "initial delay" is "Dangerous"
  - Between 2.5 to 3.5 x "initial delay" is on the threshold
  - Greater than 4 x "initial delay" is safe
- NOTE: This is "initial delay" not buffer delay or Tco.

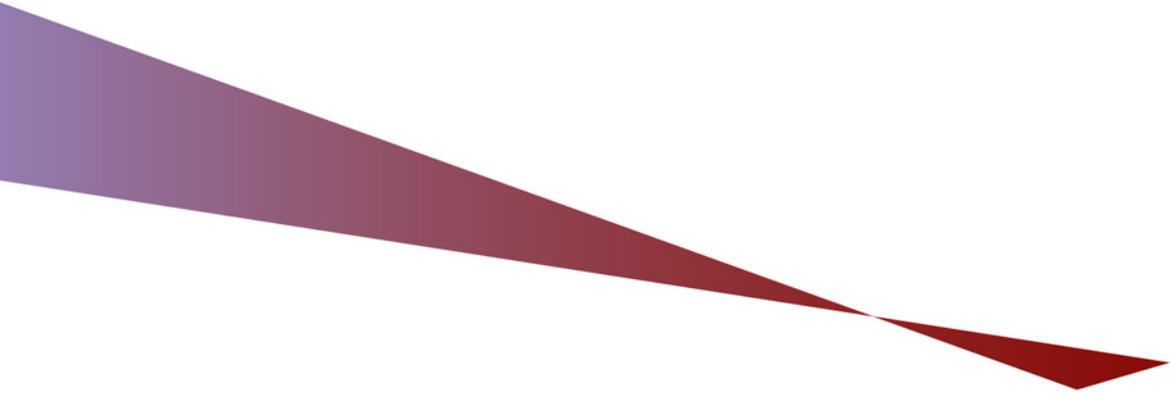cādence™

Conclusions and next step

- Conclusions
  - Be aware to use IBIS buffer models with a long "initial delay" in the VT curves for the "faster" bit-rate system simulations
  - It does mainly affect the accuracy of timing results as well as ISI facts
  - There is no "short-cut" in IBIS now to solve this issue
- Next Step
  - Need to compare the results with the real measurements
    - Need to make sure Spice transistor-level model simulation is correct vs. lab measurement
  - Find out the solutions
    - Detect issues (how to validate)
    - Enhancement for IBIS

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Questions and Comments?

Thank You!

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