Multi-Mode Modeling

Bob Ross
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Configurable Buffers in IBIS

- **Current methods in IBIS**
  - [Model Selector] (general usage – all voltages, modes, technologies, conditions)
  - [Alternate Package Models]
  - [Series Switch Groups] (and [On], [Off] models)
  - [Add Submodel] (for specific state (e.g., Non-driving mode only)

- **Tool/user select based on ALL choices documented**
  - State selection (e.g., for I/O Driving or Non-driving operation)
  - EBD format – multiple buffers on net
  - Algorithmic Model Executable (Windows, Unix, Linux, etc.)
  - Multi-lingual language selection (VHDL-AMS, SPICE, Verilog_A(MS), etc.)
  - Syntax with levels of override for higher level functionality (technical and levels of specification)
Missing Configurability

• Examples
  – Differential/single-ended reconfiguration
  – 3-state vs. I/O distinction if both exist in device (not really needed)
  – 3-state on/off toggle dynamic characterization when “enable” is switched (not really needed)

• Can offer separate [Component]s for hard coded configurations

• EDA tools can hard override the configuration

• Example of one configurable buffer given
Real Output Clock(s) Example

CMOS (3.3V, 2.5V, 1.8V, 1.5V plus slew rates [Model Selector]s)  In Sync. Mode Selector MUXs

LVPECL, LVDS [Model Selector]s

(Complimentary CMOS possible, but not in this device)
Four [Component] Choices

[Component] CLOCKS_SS
[Component] CLOCKS_SD
[Component] CLOCKS_DS
[Component] CLOCKS_DD

8 Single-ended (S) pins (1-8) or 4 Differential (D) pin-pairs (1,2 3,4 5,6 7,8)

Model Selectors in Sync. with Differential Pin assignments (next two slides)
## [Model Selector] Choices for [Pin]s

<table>
<thead>
<tr>
<th>PIN</th>
<th>S</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>clk_1  { CMOS_A</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>clk_2  { CMOS_A</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>clk_3  { CMOS_A</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>clk_4  { CMOS_A</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>clk_5  { CMOS_B</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>clk_6  { CMOS_B</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>clk_7  { CMOS_B</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>clk_8  { CMOS_B</td>
<td></td>
</tr>
</tbody>
</table>
Four Distinct [Diff Pin] Assignments

[Diff Pin]
1 2  
Both or Neither for Bank A
3 4  
5 6  
Both or Neither for Bank B
7 8  
[Model Selector] CMOS_A
...  
[Model Selector] CMOS_B
...  
[Model Selector] Diff_A
...  
[Model Selector] Diff_B
...
Issues Under Consideration

• Differential Mode (vdiff location problem)
  – “vdiff” – can be different for PECL and LVDS if these were Input models
  – (Not a problem here for Output only clocks)
• IBIS Limitation
  – No selection mechanism for re-configuration of single-ended (matched pairs) to differential
  – Originally an ECL option for early devices
  – Must use different [Component]s for hard-coded choices
Observations

• Configurability makes a strong case for moving differential parameters into the [Model] scope directly along with single-ended parameters
  – Already done for [Receiver Thresholds]
  – Ugly but solves dual mode problem for some technologies (DDR, USB, ECL, Configurable)

• Consider offering a single-ended/differential selection option
  – Another mechanism for EDA tools to control
  – Helps limit the choices
  – But selectors and S/D modes must be in sync.